

MOSFET – Dual N-Channel and Dual P-Channel, POWERTRENCH[®], GreenBridge[™] Series of High-Efficiency Bridge Rectifiers

N-Channel: 100 V, 6 A, 110 mΩ
P-Channel: -80 V, -6 A, 190 mΩ

FDMQ8203

General Description

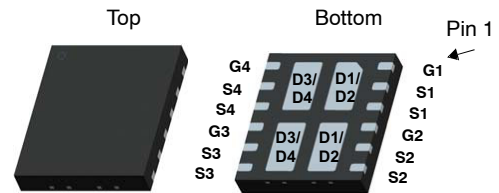
This quad mosfet solution provides ten-fold improvement in power dissipation over diode bridge.

Features

- Q1/Q4: N-Channel
 - ♦ Max $R_{DS(on)}$ = 110 mΩ at $V_{GS} = 10$ V, $I_D = 3$ A
 - ♦ Max $R_{DS(on)}$ = 175 mΩ at $V_{GS} = 6$ V, $I_D = 2.4$ A
- Q2/Q3: P-Channel
 - ♦ Max $R_{DS(on)}$ = 190 mΩ at $V_{GS} = -10$ V, $I_D = -2.3$ A
 - ♦ Max $R_{DS(on)}$ = 235 mΩ at $V_{GS} = -4.5$ V, $I_D = -2.1$ A

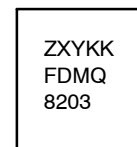
Applications

- High-Efficiency Bridge Rectifiers
- Substantial Efficiency Benefit in PD Solutions
- These Device is Pb-Free, Halide Free and is RoHS Compliant



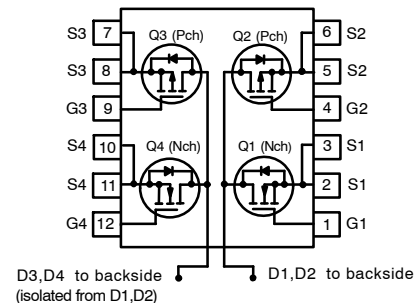
WDFN12 5x4.5, 0.8P
CASE 511CS

MARKING DIAGRAM



FDMQ8203 = Specific Device Code
 Z = Assembly Plant Code
 XY = Date Code
 KK = Lot Run Traceability Code

N-Channel / P-Channel



ORDERING INFORMATION

Device	Package	Shipping [†]
FDMQ8203	MLP 4.5x5 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDMQ8203

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Q1/Q4	Q2/Q3	Unit
V _{DS}	Drain to Source Voltage		100	−80	V
V _{GS}	Gate to Source Voltage		±20	±20	V
I _D	Drain Current	– Continuous (Package Limited) T _C = 25°C	6	−6	A
		– Continuous (Silicon Limited) T _C = 25°C	10	−10	
		– Continuous T _A = 25°C (Note 1a)	3.4	−2.6	
		– Pulsed	12	−10	
P _D	Power Dissipation for Single Operation	T _C = 25°C	22	37	W
	Power Dissipation for Dual Operation	T _A = 25°C (Note 1a)	2.5		
T _J , T _{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	160	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
--------	-----------	----------------	------	-----	-----	-----	------

OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 I _D = -250 μA, V _{GS} = 0	Q1/Q4 Q2/Q3	100 -80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1/Q4 Q2/Q3	- -	72 -79	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V V _{DS} = -64 V, V _{GS} = 0 V	Q1/Q4 Q2/Q3	- -	-	1 -1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	Q1/Q4 Q2/Q3	- -	-	±100 ±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = -250 μA	Q1/Q4 Q2/Q3	2 -1	3 -1.6	4 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1/Q4 Q2/Q3	- -	-8 5	-	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3 A V _{GS} = 6 V, I _D = 2.4 A V _{GS} = 10 V, I _D = 3 A, T _J = 125°C	Q1/Q4	- - -	85 118 147	110 175 191	mΩ
		V _{GS} = -10 V, I _D = -2.3 A V _{GS} = -4.5 V, I _D = -2.1 A V _{GS} = -10 V, I _D = -2.3 A, T _J = 125°C	Q2/Q3	- - -	161 188 273	190 235 323	
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 3 A V _{DS} = -10 V, I _D = -2.3 A	Q1/Q4 Q2/Q3	- -	6 6	- -	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1/Q4 V _{DD} = 50 V, V _{GS} = 0 V, f = 1.0 MHz Q2/Q3 V _{DS} = -40 V, V _{GS} = 0 V, f = 1.0 MHz Q1/Q4 Q2/Q3	Q1/Q4 Q2/Q3	- -	158 639	210 850	pF
C _{oss}	Output Capacitance		Q1/Q4 Q2/Q3	- -	41 46	55 65	pF
C _{rss}	Reverse Transfer Capacitance		Q1/Q4 Q2/Q3	- -	2.6 24	5 40	pF

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition		Type	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 2)								
t _{d(on)}	Turn-On Delay Time	Q1/Q4 V _{DD} = 50 V, I _D = 3 A, V _{GS} = 10 V, R _{GEN} = 6 Ω Q2/Q3 V _{DD} = -40 V, I _D = -2.3 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		Q1/Q4	–	3.8	10	ns
t _r	Rise Time			Q2/Q3	–	4.7	10	ns
t _{d(off)}	Turn-Off Delay Time			Q1/Q4	–	1.3	10	ns
t _f	Fall Time			Q2/Q3	–	2.8	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V V _{GS} = 0 V to -10 V	Q1/Q4: V _{DD} = 50 V, I _D = 3 A Q2/Q3 V _{DD} = -40 V, I _D = -2.3 A	Q1/Q4	–	2.9	5	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to 5 V V _{GS} = 0 V to -4.5 V		Q2/Q3	–	13	19	nC
Q _{gs}	Gate-Source Gate Charge			Q1/Q4	–	1.6	3	nC
Q _{gd}	Gate to Drain “Miller” Charge			Q2/Q3	–	6.4	10	nC
				Q1/Q4	–	0.8	–	nC
				Q2/Q3	–	1.6	–	nC
				Q1/Q4	–	0.8	–	nC
				Q2/Q3	–	2.6	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drine Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$, $I_S = -2.3\text{ A}$ (Note 2)	Q1/Q4 Q2/Q3	– –	0.86 –0.82	1.3 –1.3	V
t_{rr}	Reverse Recovery Time	Q1/Q4: $I_F = 3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ Q2/Q3: $I_F = -2.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q1/Q4 Q2/Q3	– –	32 26	52 42	ns
Q_{rr}	Reverse Recovery Charge		Q1/Q4 Q2/Q3	– –	21 26	34 42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 50°C/W when mounted on a 1 in² pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.



- 160°C/W when mounted on a minimum pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS (N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

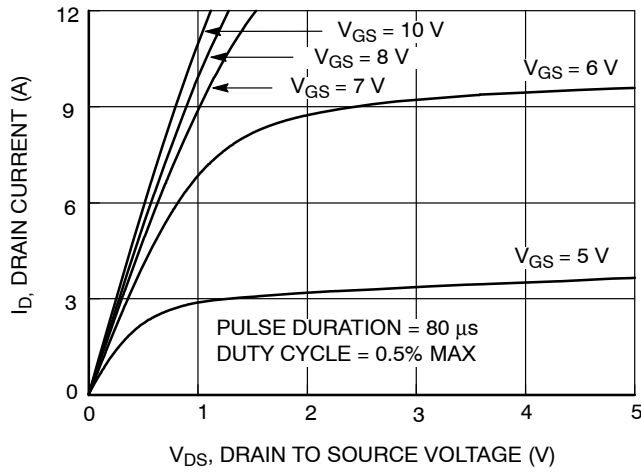


Figure 1. On Region Characteristics

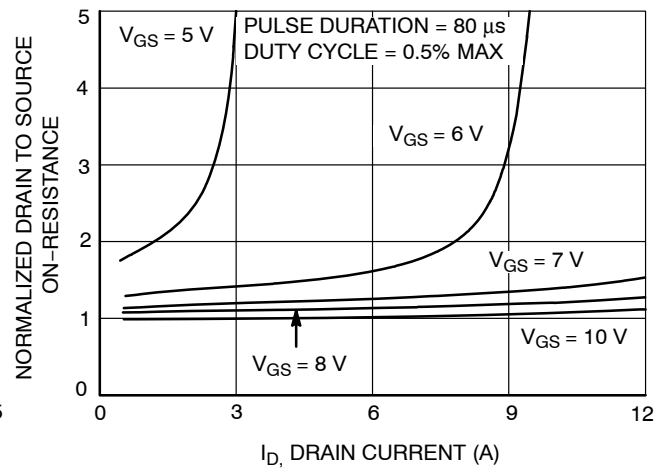


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

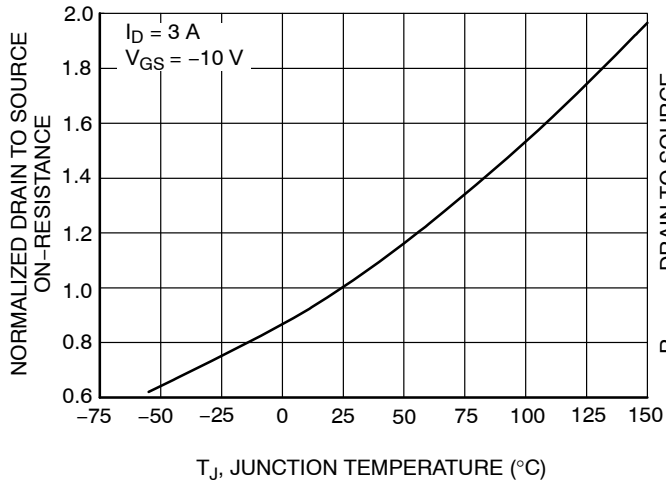


Figure 3. Normalized On Resistance vs Junction Temperature

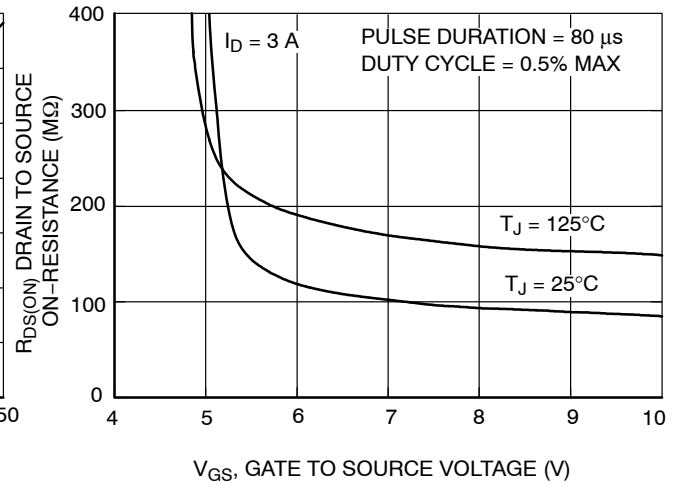


Figure 4. On-Resistance vs Gate to Source Voltage

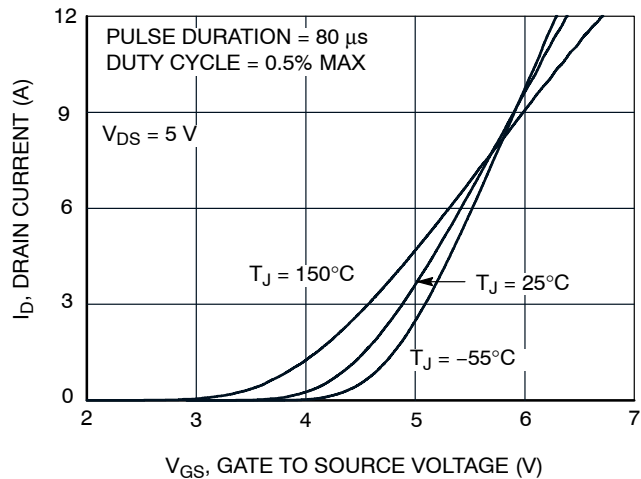


Figure 5. Transfer Characteristics

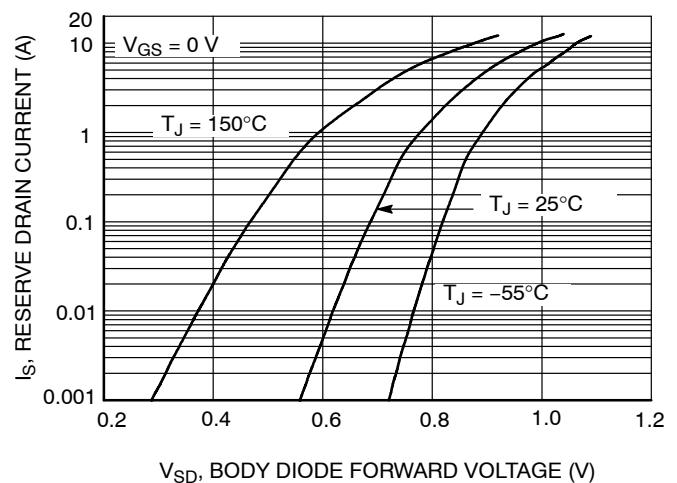


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

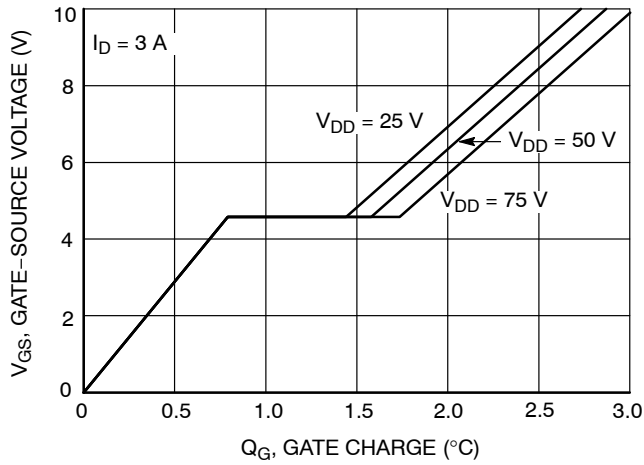


Figure 7. Gate Charge Characteristics

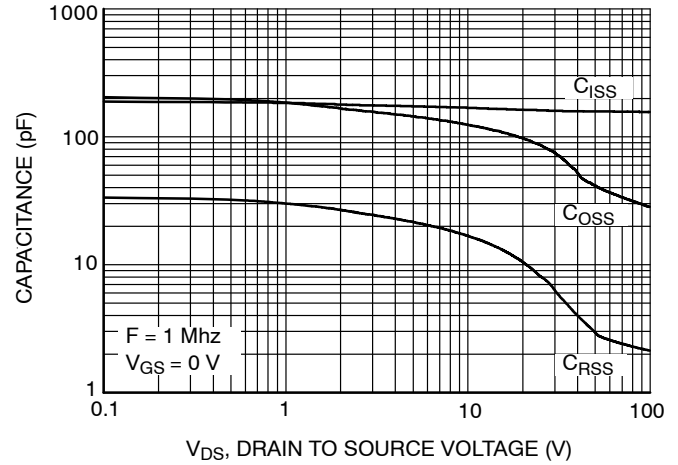


Figure 8. Capacitance vs Drain to Source Voltage

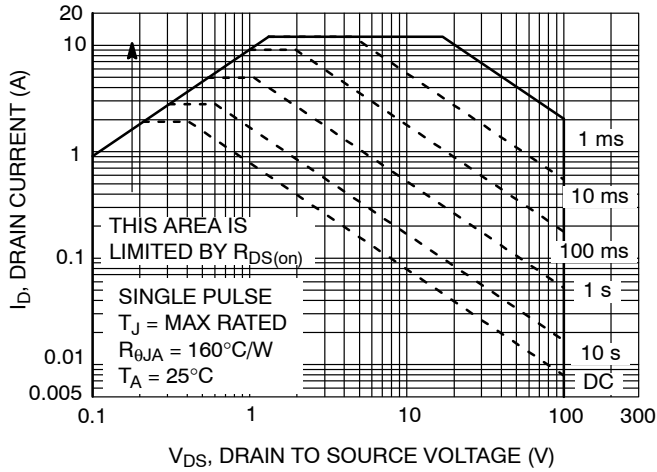


Figure 9. Forward Bias Safe Operating Area

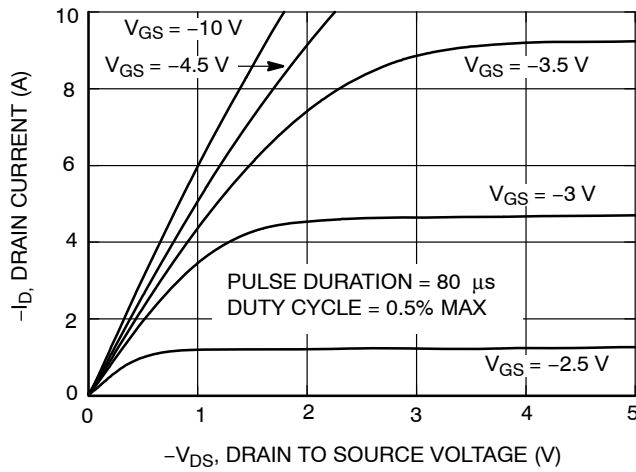
TYPICAL CHARACTERISTICS (P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Figure 10. On-Region Characteristics

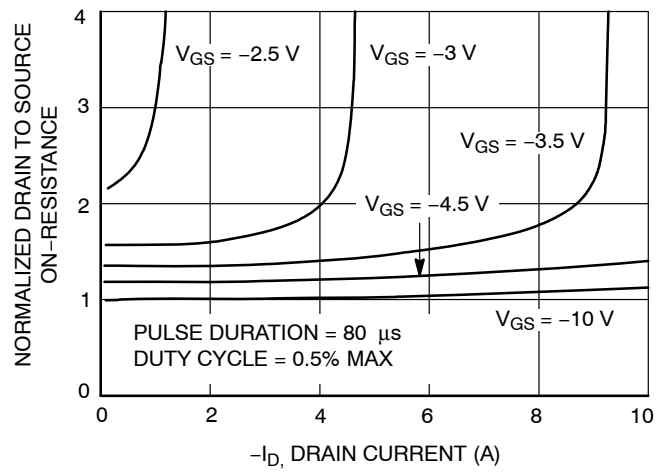


Figure 11. Normalized On-Resistance vs Drain Current and Gate Voltage

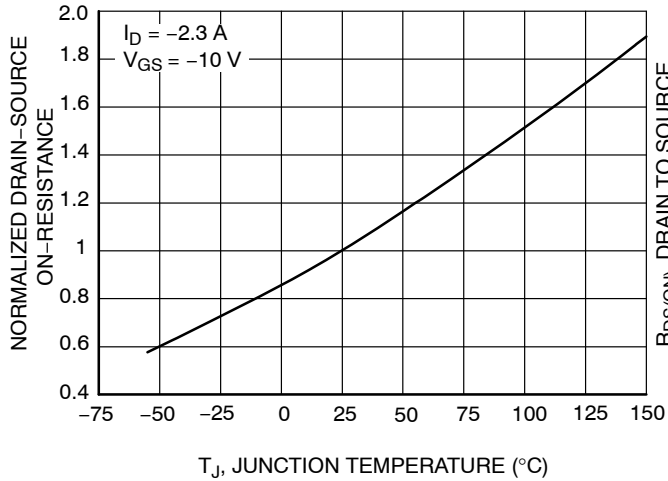


Figure 12. Normalized On-Resistance vs Junction Temperature

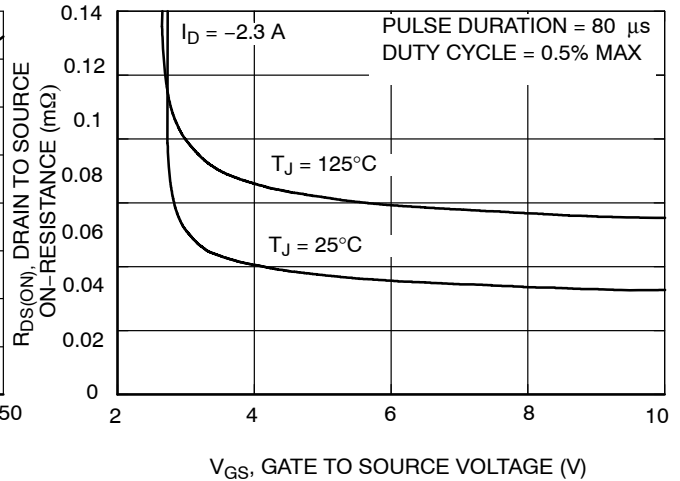


Figure 13. On-Resistance vs Gate to Source Voltage

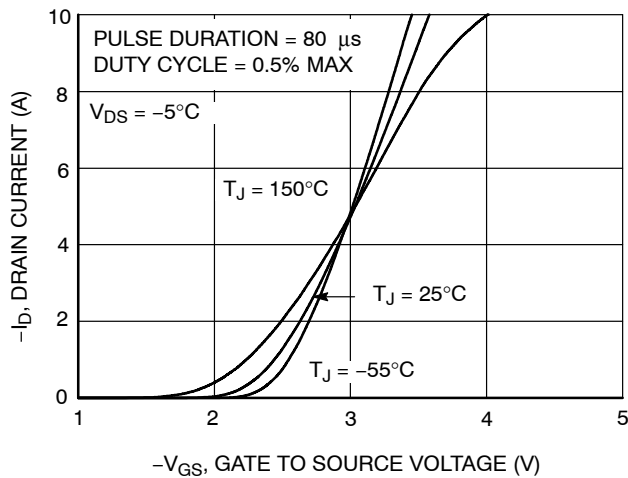


Figure 14. Transfer Characteristics

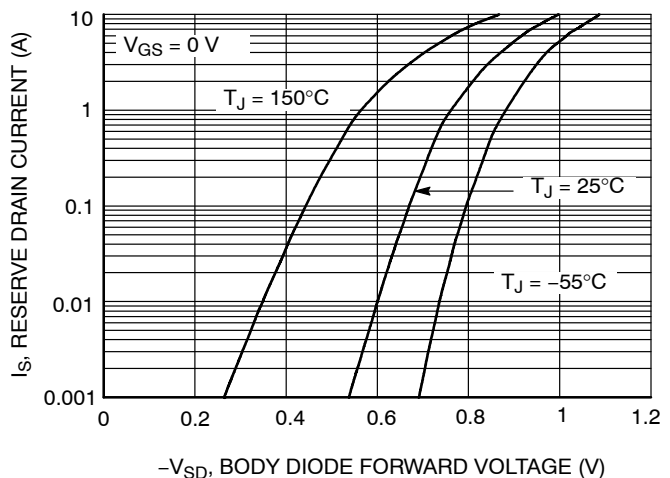


Figure 15. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q1 P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

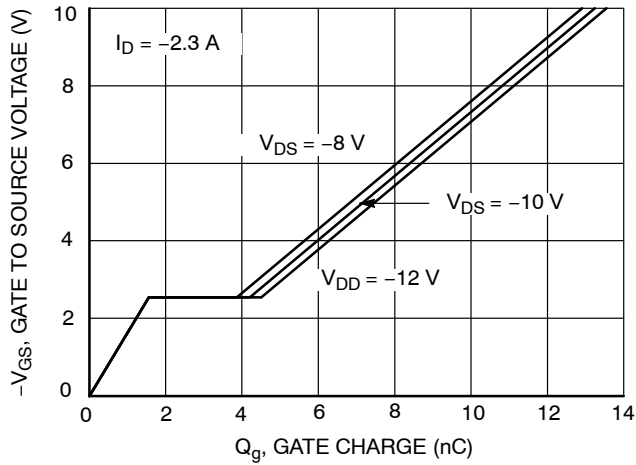


Figure 16. Gate Charge Characteristics

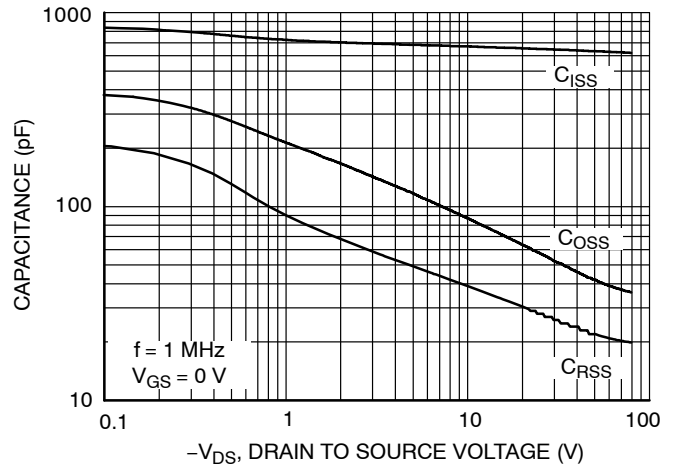


Figure 17. Capacitance vs Drain to Source Voltage

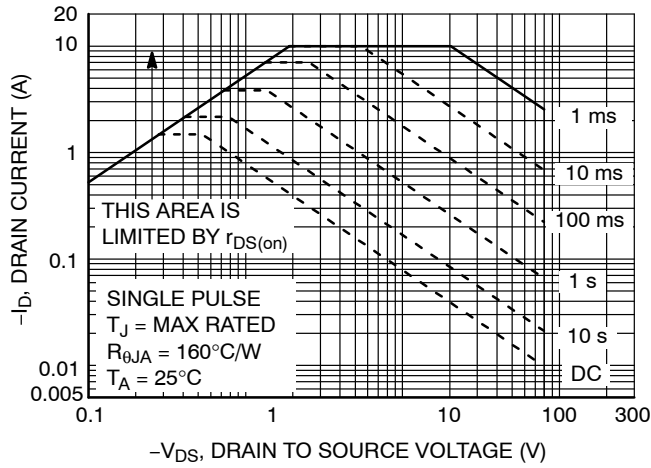


Figure 18. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

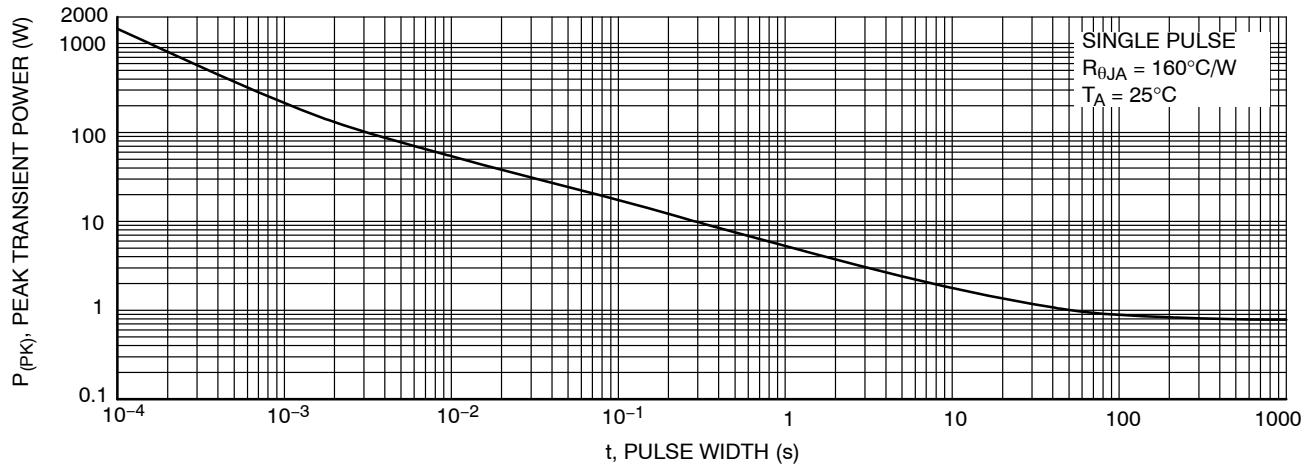


Figure 19. Single Pulse Maximum Power Dissipation

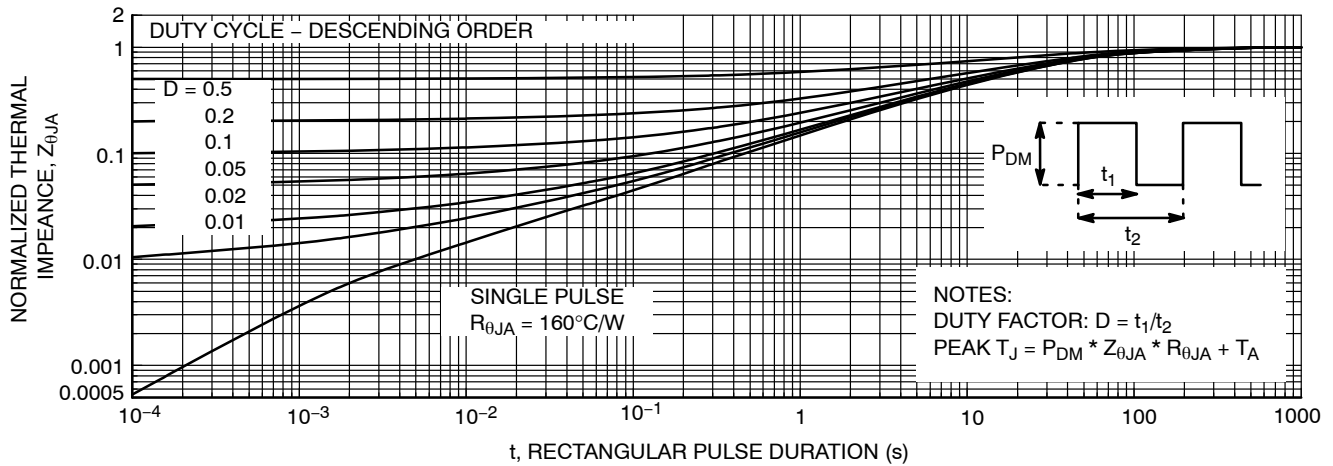


Figure 20. Junction-to-Ambient Transient Thermal Response Curve

POWERTRENCH is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

GreenBridge is trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

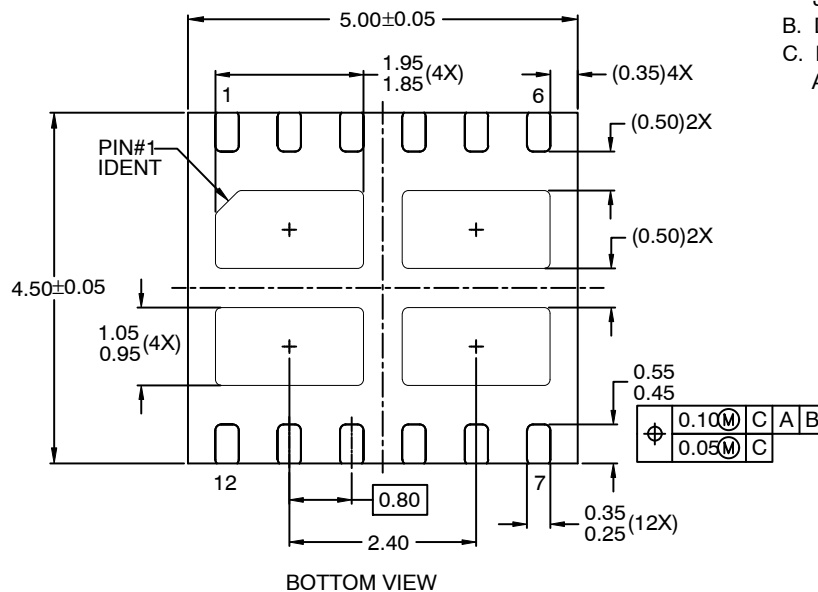
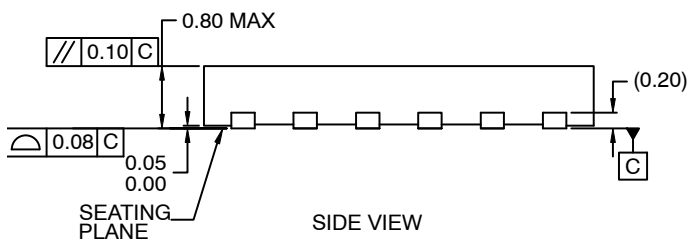
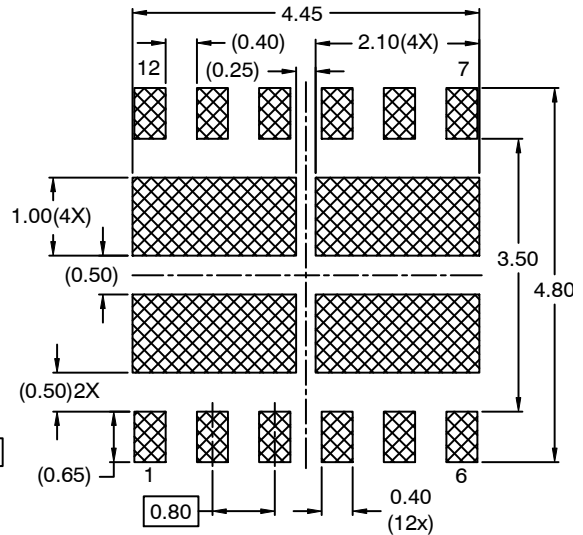
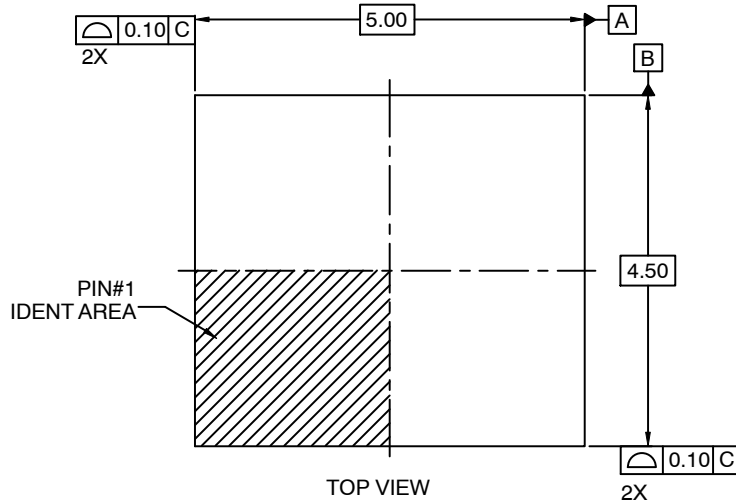
PACKAGE DIMENSIONS

ON Semiconductor®

ON

WDFN12 5x4.5, 0.8P
CASE 511CS
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

DOCUMENT NUMBER:	98AON13607G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN12 5X4.5, 0.8P	PAGE 1 OF 1

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales