MP6605E

4-Channel, Low-Side Driver IC with Serial Interface

DESCRIPTION

The MP6605E is a 4-channel, low-side driver IC with a serial interface. It integrates low-side MOSFET (LS-FET) switches and high-side (HS) clamp diodes to drive inductive loads. This device is well-suited for unipolar stepper motors and solenoid drives.

The MP6605E operates from a supply voltage up to 60V, and it can deliver an output current (I_{OUT}) up to 1.5A, depending on the PCB design and thermal conditions. The maximum voltage on the motor driver output pins is 60V.

Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The MP6605E is available in a QFN-24 (4mmx4mm) package.

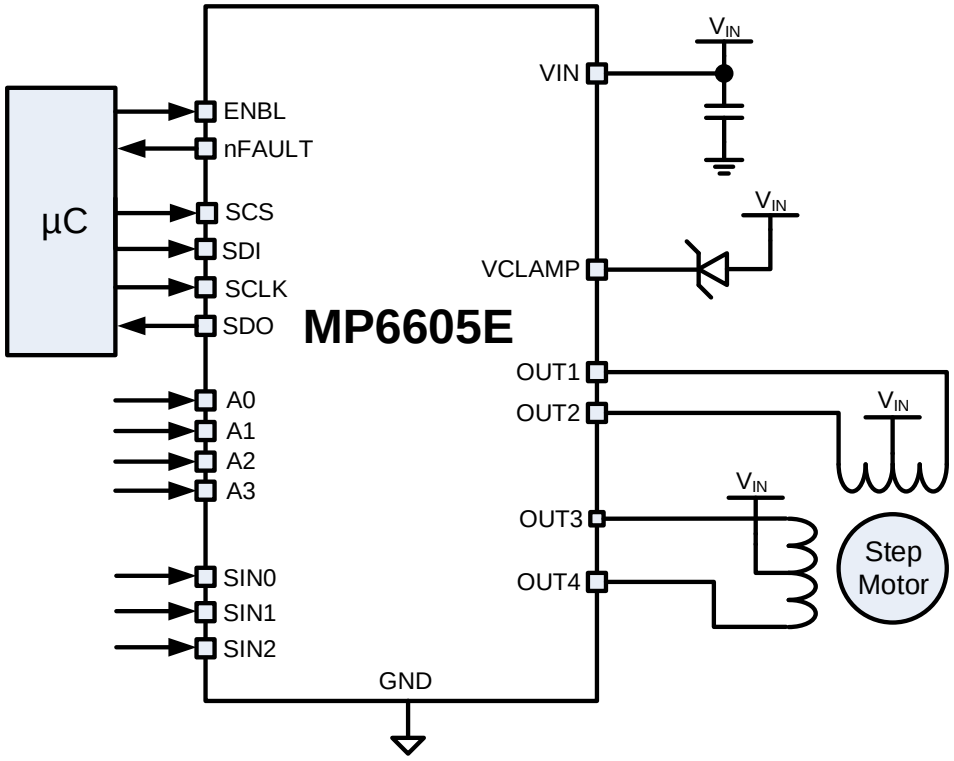
FEATURES

- Wide 4.5V to 60V Input Voltage (V_{IN}) Range
- 60V Maximum Winding Clamp Voltage (V_{CLAMP})
- Four Low-Side MOSFETs (LS-FETs) and Clamp Diodes
- 350mΩ MOSFET On Resistance
- 1.5A Maximum Output Current (I_{OUT}) while One LS-FET is On, or 700mA Maximum I_{OUT} while Four LS-FETs are On
- Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO) Protection
- Over-Temperature Protection (OTP)
- Fault Indication Output
- No Control Power Supply Required
- Simple Logic Interface with Schmitt Triggers
- 3.3V and 5V Compatible Logic Supply
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- Unipolar Stepper Motors
- Solenoid Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6605EGR*	QFN-24 (4mmx4mm)	*See Below*	1

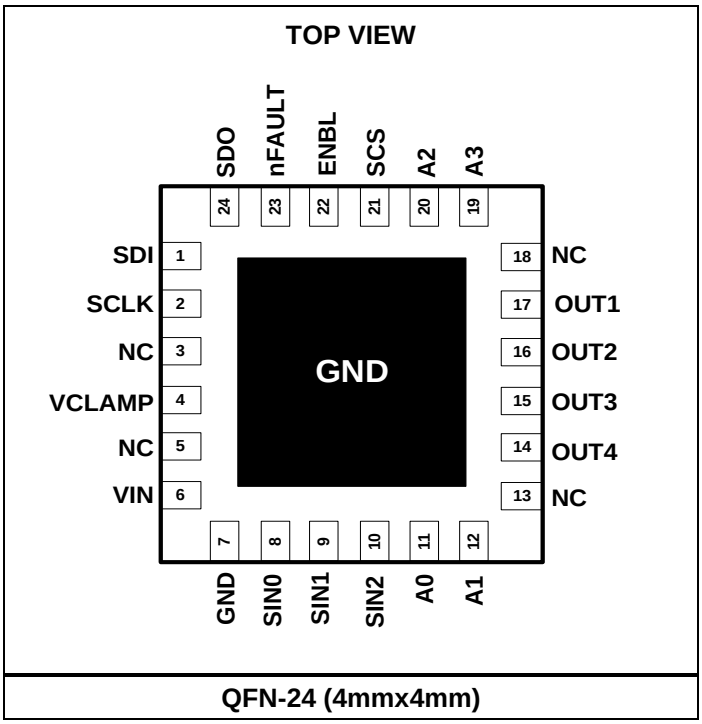
* For Tape & Reel, add suffix -Z (e.g. MP6605EGR-Z).

TOP MARKING

MPSYWW
M6605E
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6605E: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
6	VIN	**Input supply voltage.** Decouple the VIN pin with a minimum 100nF ceramic capacitor connected to GND. Additional bulk capacitance may be required.
7, EP	GND	**Power ground.**
4	VCLAMP	**High-side clamp.** Connect the VCLAMP pin to VIN with a TVS or Zener diode to clamp the leakage inductance spike.
21	SCS	**Serial chip selection input.** Drive the SCS pin active high to enable serial data transfer. SCS is connected to an internal pull-down resistor.
1	SDI	**Serial data input.** The SDI pin has an internal pull-down resistor.
2	SCLK	**Serial clock input.** The SCLK pin has an internal pull-down resistor.
24	SDO	**Serial data output.** The SDO pin is an open-drain output that requires an external pull-up resistor if it is used.
11	A0	**Address setting input.** Connect the A0~A3 pins to ground or leave them open to configure the serial interface address. These pins are connected to an internal supply voltage (about 6V) with an internal pull-up resistor.
12	A1	
20	A2	
19	A3	
8	SIN0	**Sensor input 0.** The SIN0 pin has an internal pull-down resistor.
9	SIN1	**Sensor input 1.** The SIN1 pin has an internal pull-down resistor.
10	SIN2	**Sensor input 2.** The SIN2 pin has an internal pull-down resistor.
22	ENBL	**Enable input.** Drive the ENBL pin to logic low to disable the outputs; drive ENBL to logic high to enable the outputs. The state of ENBL does not affect the serial interface. ENBL has an internal pull-down resistor.
23	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output that requires an external pull-up resistor when it is used. If a fault condition occurs, then nFAULT is driven low.
17	OUT1	**Output terminal 1.**
16	OUT2	**Output terminal 2.**
15	OUT3	**Output terminal 3.**
14	OUT4	**Output terminal 4.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +65V
OUTx voltage (V_{OUTx}) ..... -0.7V to+ 65V
Clamp voltage (V_{CLAMP}) ..... -0.7V to +65V
A0, A1, A2, A3 ..... -0.3V to +9V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 2.9W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human body model (HBM) …….. ±2kV
Charged device model (CDM) …… ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 60V
Output voltage (V_{OUTx})..... 0V to 60V
Maximum output current for LS-FETs (I_{LSX})…….. ……. 1.5A
Maximum output current for HS diodes (I_{HSX}) …….. 1.5A at duty cycle <20%
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)……..42.....9.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{CLAMP} = 36V, T_A = 25°C, unless otherwise noted.

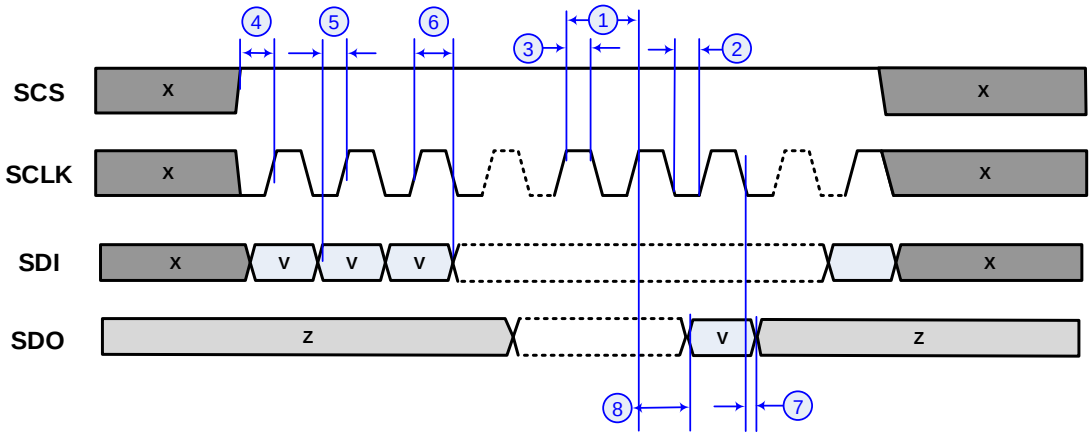
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5	12 or 24	60	V
Clamp voltage	V_{CLAMP}		V_{IN}		60	V
Quiescent current	I_Q	V_{IN} = 24V, ENBL = 1, with no load		1.2	5	mA
Internal MOSFETs						
Output on resistance	$R_{DS(ON)}$	V_{IN} = 24V, I_{OUT} = 700mA, T_J = 25°C		350	500	mΩ
High-side diode forward voltage	V_{FWD_HS}	I_{OUT} = 700mA			1.1	V
Body diode forward voltage	V_{FWD_LS}	I_{OUT} = 700mA			1.1	V
Control Logic						
Input logic low threshold	V_{IL}				0.7	V
Input logic high threshold	V_{IH}		2.3			V
Input logic hysteresis	ΔV_{IH}			560		mV
Logic input current	$I_{IN(H)}$	V_{IH} = 5V			20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V			5	µA
Internal pull-up current (A0~A3)	I_{PU}	To V_{PU}		40		µA
Internal pull-up voltage (A0~A3)	V_{PU}				8.1	V
nFAULT, SDO Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
Under-voltage lockout (UVLO) rising threshold	V_{IN_RISE}			3.4	4.5	V
Over-current (OC) trip level	I_{OCP}		1.5	4		A
OC deglitch time	t_{OCP}			3.5		µs
OC retry time	t_{OCR}			2.5		mS
Thermal shutdown (5)	T_{TSD}			155		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			25		°C
Output enable time (5)	t_{EN}			3.3		µs

Note:

5) Guaranteed by design.

TIMING CHARACTERISTICS (6)

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.



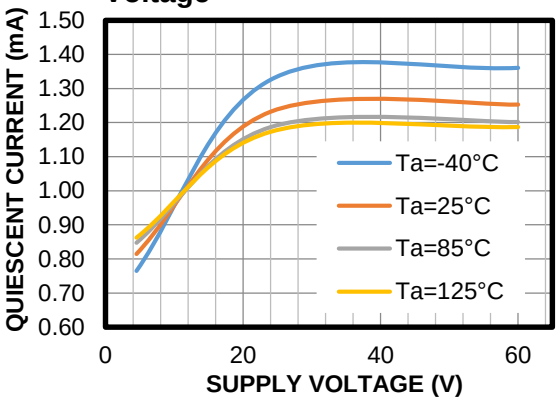
Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK cycle time	t1		250			ns
SCLK frequency			0.1		4	MHz
SCLK high time	t2		50			ns
SCLK low time	t3		50			ns
SCLK rising/falling time					50	ns
Set-up time SCS high to SCLK rising	t4		30			ns
Set-up time SDI valid to SCLK rising	t5		15			ns
Holding time SCLK rising to SDI invalid	t6		10			ns
Holding time SCLK rising to SDO invalid	t7		40			ns
Delay time SCLK falling to SDO valid	t8	C_L < 100pF			10	ns

Note:

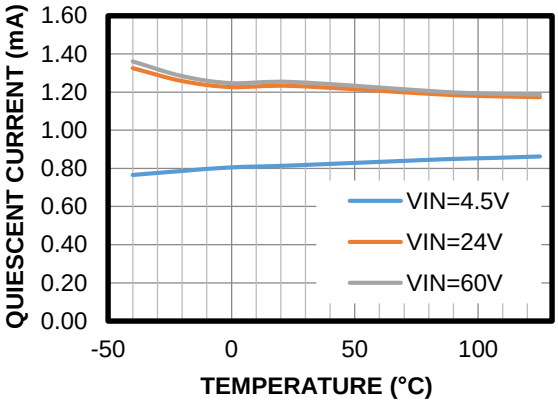
6) Not subject to production testing. Specified by design.

TYPICAL CHARACTERISTICS

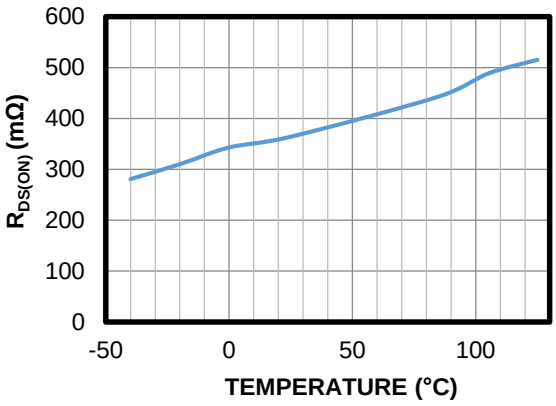
Quiescent Current vs. Supply Voltage



Quiescent Current vs. Temperature



$R_{DS(ON)}$ vs. Temperature

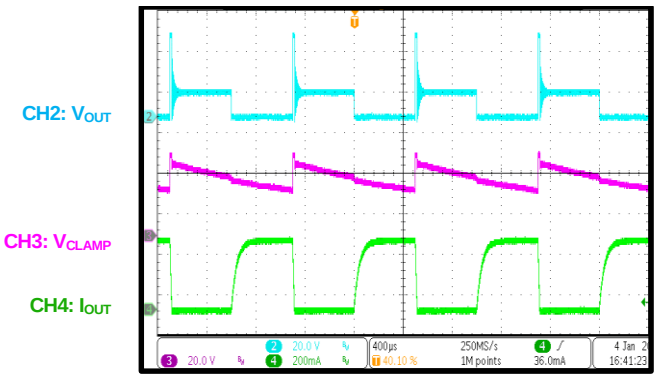


TYPICAL PERFORMANCE CHARACTERISTICS

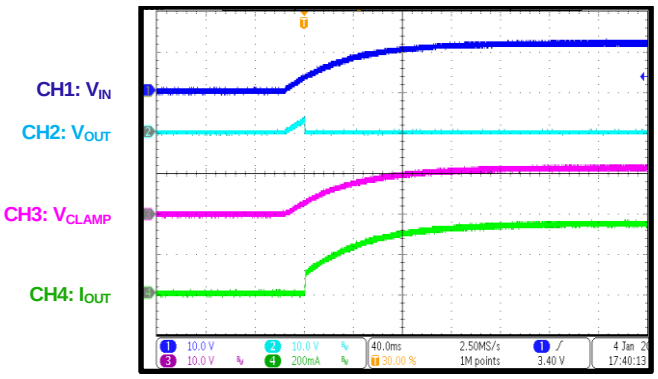
V_{IN} = 12V, V_{CLAMP} = 24V, VCLAMP connected to VIN with 24V TVS diode, I_{OUT} = 700mA, T_A = 25°C, resistor + inductor load: R = 33Ω, L = 1.5mH/channel, unless otherwise noted.

Normal Operation

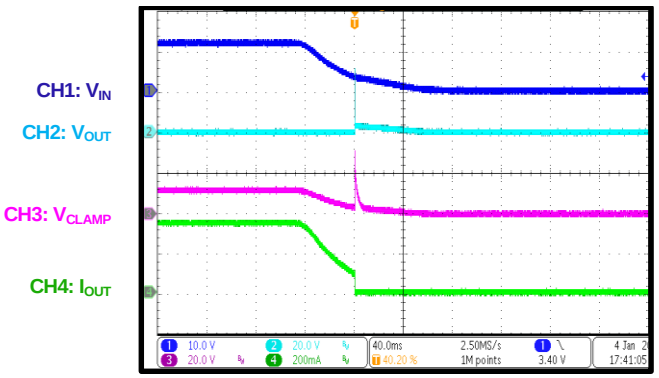
f_{SW} = 1kHz



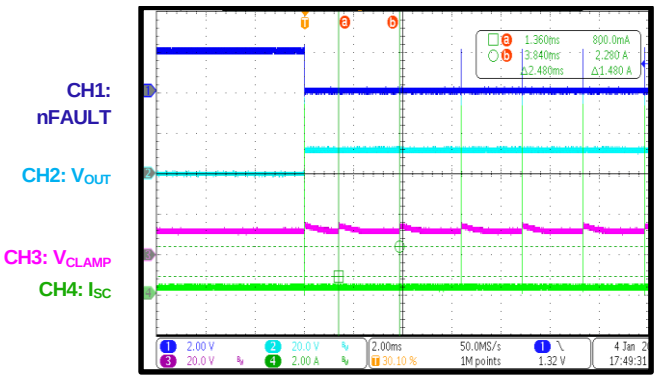
Start-Up through VIN



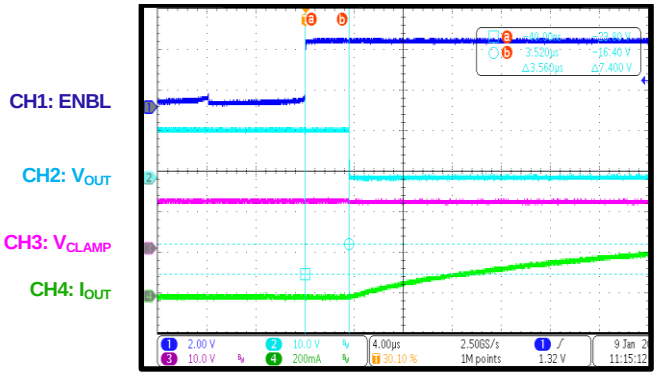
Shutdown through VIN



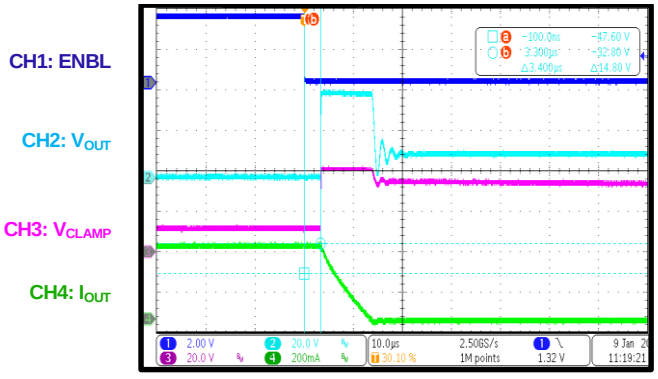
SCP



Chip Enabled



Chip Disabled



FUNCTIONAL BLOCK DIAGRAM

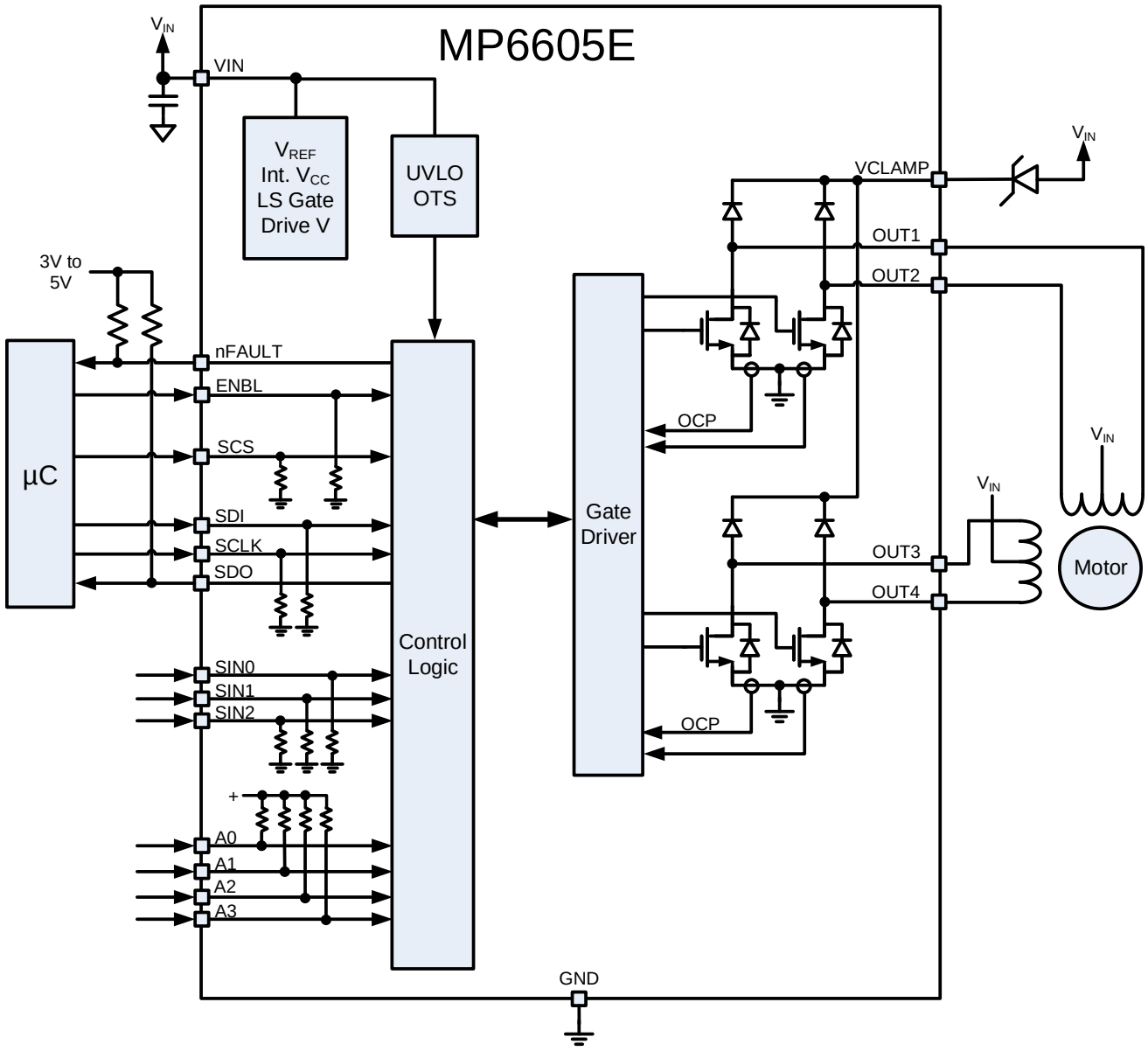


Figure 1: Functional Block Diagram

OPERATION

The MP6605E is a 4-channel, low-side driver IC that integrates four N-channel power MOSFETs and four clamp diodes with 1.5A of current capability per channel. The MP6605E operates across a wide 4.5V to 60V supply voltage range.

The MP6605E is designed to drive inductive loads, including unipolar stepper motors and solenoids.

Unipolar Stepper Operation

A unipolar stepper motor has two windings. These windings are driven by currents that are 90° out of phase. Each winding has a center tap that is connected to the power source. The current is driven through the winding in a push-pull fashion, meaning that the device alternately pulls one side of the winding to ground, then it pulls the other side. This reverses the current, which then reverses the magnetic field.

After a MOSFET turns off, current continues to flow through the other side of the winding due to the inductance of the winding. The current flows from ground through the opposite MOSFET body diode and to the power supply.

Leakage Inductance Clamp (VCLAMP)

Because the two halves of the winding are not perfectly coupled in a unipolar stepper motor, there is leakage inductance. When a MOSFET turns off, the voltage rises up to two times the supply for a short period. This leakage inductance spike must be clamped to prevent over-voltage damage on the MOSFETs.

If a switch turns off when driving a solenoid connected to the VIN pin, current must continue to flow until the magnetic field decays.

These currents flow through internal diodes at each output to a common VCLAMP pin. Generally, the VCLAMP pin is connected to a transient voltage suppressor that limits the voltage on the output pins to a maximum of 60V, regardless of the VIN pin's voltage.

If the outputs do not need to exceed the VIN pin's supply, connect VCLAMP to VIN.

ENBL Operation

The ENBL pin controls the output drivers. When ENBL is high, the outputs are enabled, and the signals on the serial interface are recognized. When ENBL is low, the outputs are disabled, but the serial interface remains operational. ENBL has an internal pull-down resistor.

Address Input Pins

The four address input pins (A0~A3) are intended to either be connected to ground or floating. These pins are connected to an internal voltage (about 6V) via an internal pull-up resistor. This means that these pins require special consideration when they are driven by a logic output.

Logic Input Pins

The remaining logic input pins have Schmitt trigger inputs with a hysteresis. These pins are compatible with 3V or 5V logic.

Fault Reporting

The MP6605C provides an nFAULT pin that reports if a fault condition (such as over-current protection (OCP), over-voltage protection (OVP), or over-temperature protection (OTP)) occurs. nFAULT is an open-drain output that is driven low when a fault condition occurs. If the fault condition is removed, nFAULT is pulled high by an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the MOSFETs by disabling the gate driver. If the device exceeds the OC limit threshold for longer than the OC deglitch time, all of the MOSFETs are disabled, and nFAULT is driven low. The driver automatically re-enables itself after about 2.5ms.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, the outputs are disabled, and nFAULT is driven low. Normal operation resumes automatically when the die temperature falls to a safe level.

Serial Interface Operation

A serial interface sends data to the MP6605E outputs, and it also reads back the state of the three sensor inputs. The serial interface implements a simple protocol, in which a slave address and command are embedded. The protocol uses 3 bytes.

The first byte is a wake up byte of 0xFEh. During this time, the SDO pin is held in high impedance.

The second byte contains the 4-bit device address, followed by the data to output to OUT4:OUT1. During this time, the SDO pin is held in high impedance.

The third byte is a stop byte (0x7Eh) to indicate the end of the command. During the third byte, the input address is output, followed by the input pin values of SIN2:SIN0. Figure 2 shows the device's address operation.

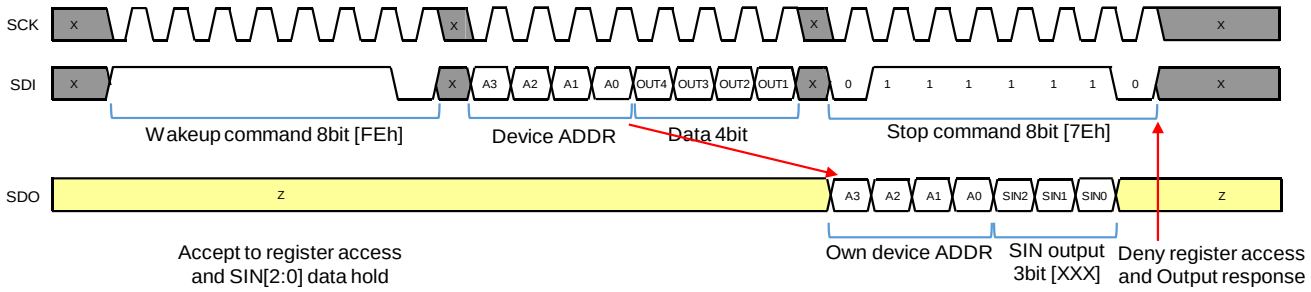


Figure 2: Device Address Operation

An address of "0000" is a broadcast address, and all devices respond to this address. Figure 3 shows the broadcast address operation.

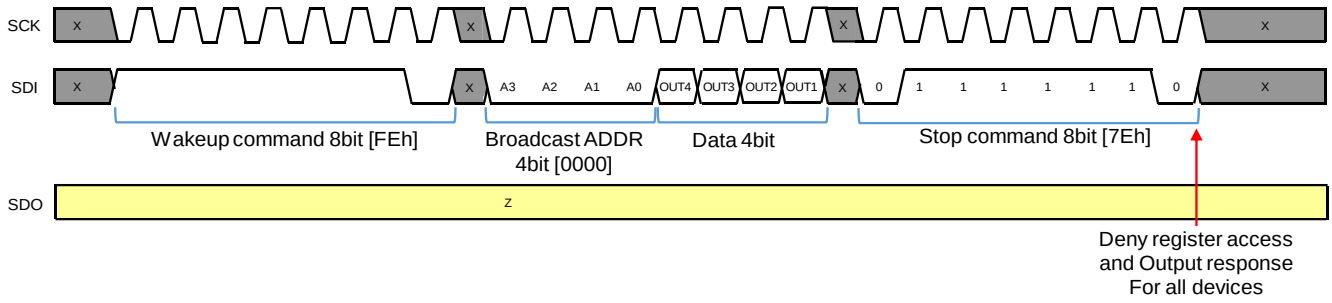


Figure 3: Broadcast Address Operation

Figure 4 on page 13 shows how multiple devices can be addressed sequentially.

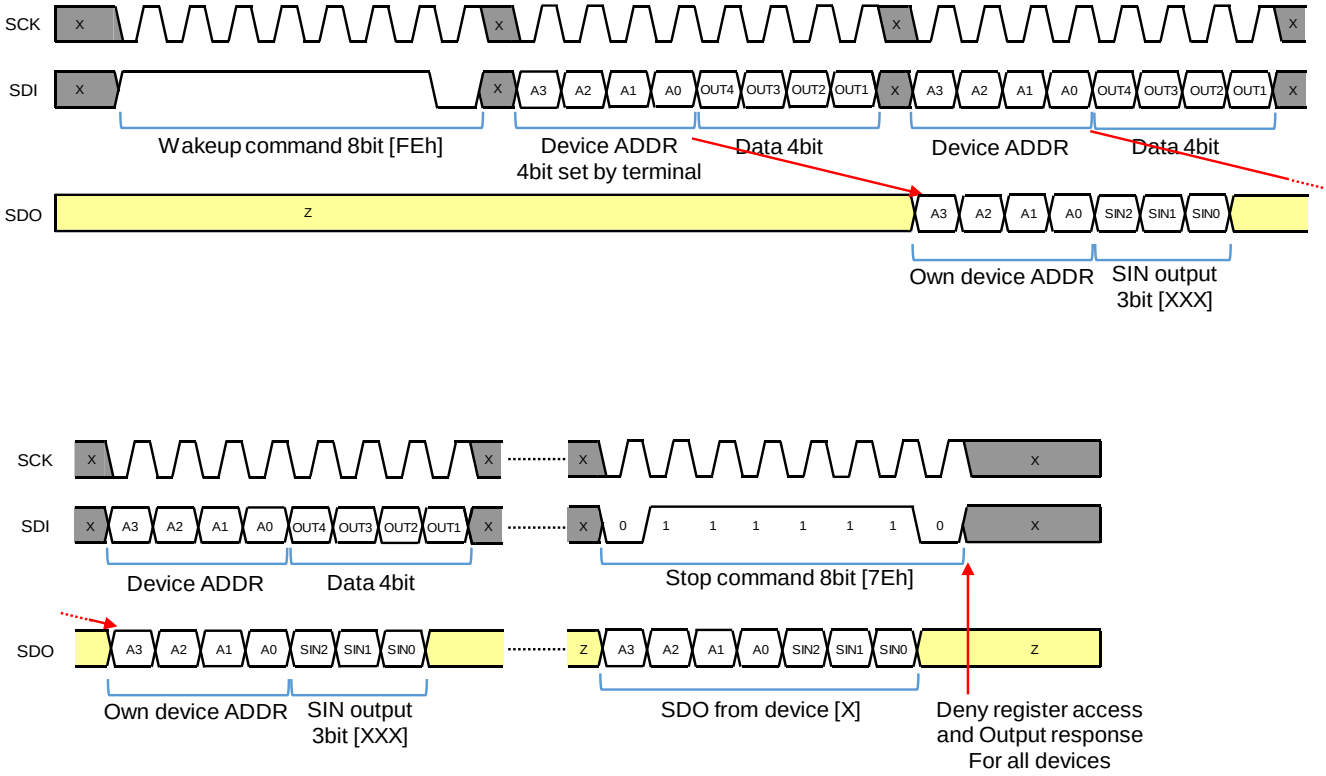


Figure 4: Addressing Multiple Devices

Certain values of ADDR and DATA are prohibited. For example, ADDR and DATA cannot be 0xFEh (the wake-up command) or 0x7Eh (the stop command). Note that ADDR = 0x0h is reserved for the broadcast address.

If the wake-up sequence is received at any time, regardless of the interface state, then the serial interface is reset to the state where it expects a new address / data packet.

APPLICATION INFORMATION

Selecting the External Components

A 100nF, X7R ceramic bypass capacitor must be placed at the VIN pin. An additional, 4.7µF minimum ceramic capacitor should be placed nearby. If the device is located far from the power source, additional electrolytic bulk capacitance may be needed.

When the current is turned off, the VCLAMP pin dissipates the energy in an inductive load. Depending on the application, VCLAMP can be connected directly to VIN, or it can be connected to VIN with a TVS diode.

Connecting VCLAMP to VIN is equivalent to connecting a diode from each output to VIN. The TVS diode allows the voltage on the output pins to exceed V_{IN} until the TVS diode breaks down. This increased voltage allows the current through the load to decay faster, which is generally required for high-speed operation with unipolar stepper motors.

The TVS diode's breakdown voltage should be selected such that the VCLAMP pin remains below its maximum ratings. Note that the TVS diode's breakdown voltage may be higher than expected as this voltage is rated at low currents.

For VIN supply voltages up to 24V, it is recommended to use a 24V TVS diode. This ensures that the VCLAMP pin voltage stays within its limits.

PCB Layout Guidelines

Efficient PCB layout is vital for stable operation. For the best results, refer for Figure 5 and follow the guidelines below:

1. Place the bypass capacitors near the IC.
2. If used, place the VCLAMP TVS diode near the IC.
3. Place thermal vias under the exposed pad to help move heat from the device to a plane on an inner layer, or on the back side of the PCB.

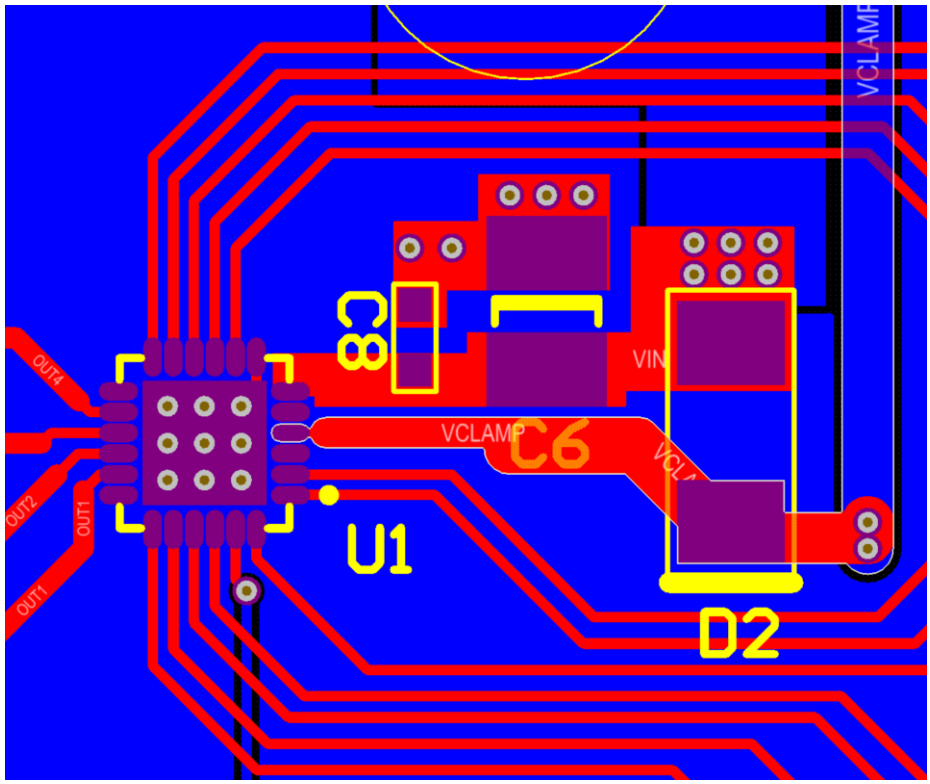


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

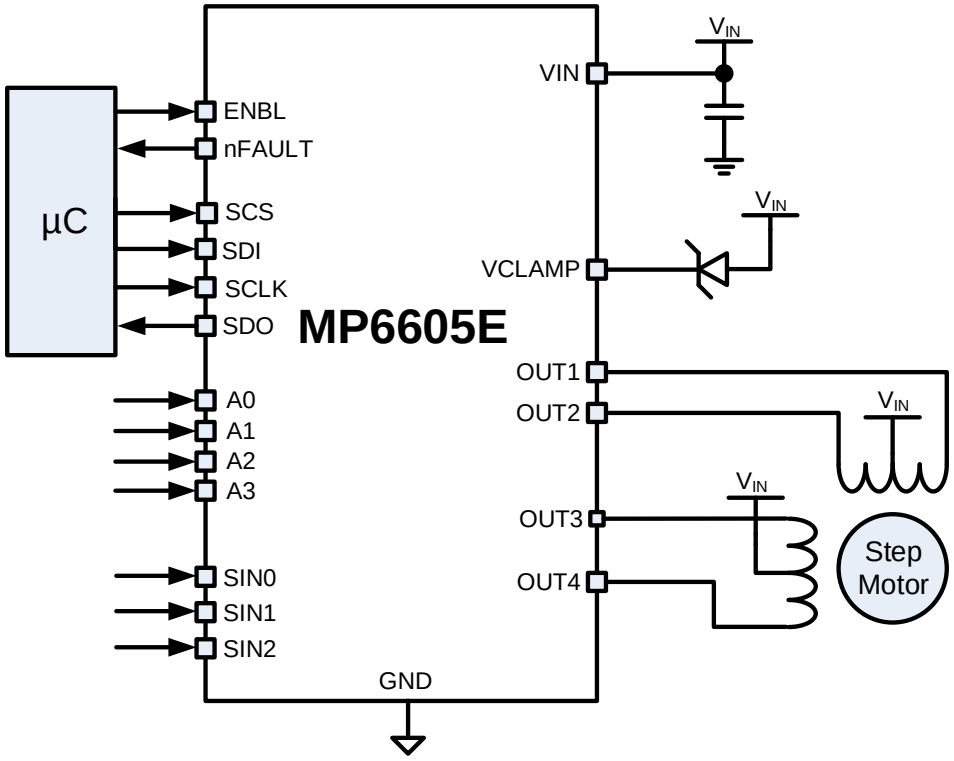
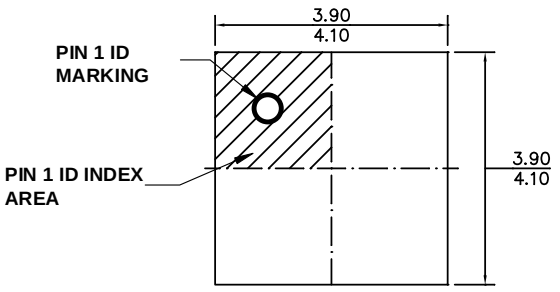


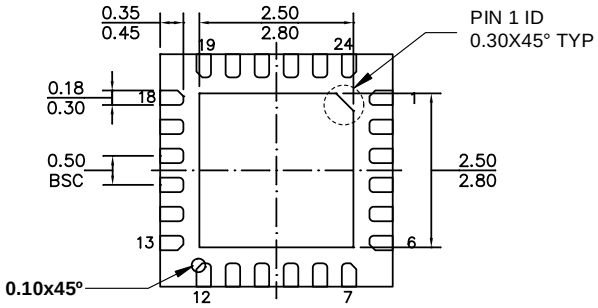
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

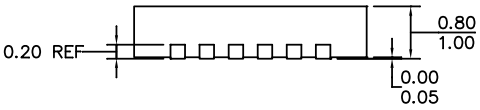
QFN-24 (4mmx4mm)



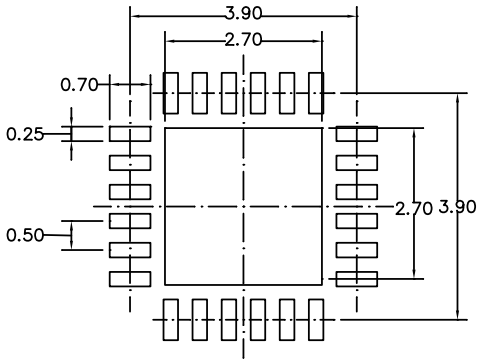
TOP VIEW



BOTTOM VIEW



SIDE VIEW

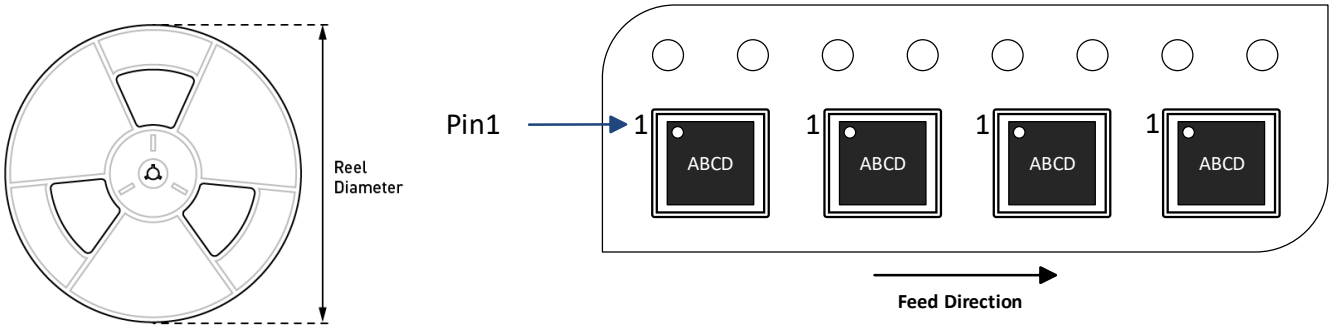


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6605EGR-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/23/2022	Initial Release	-