

Quad 2-Input Exclusive OR Gate

MM74HC86

The MM74HC86 exclusive OR gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates, while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 12 ns
- Wide Operating Voltage Range: 2 V – 6 V
- Low Input Current: 1 μ A Maximum
- Low Quiescent Current: 40 μ A Maximum (74 Series)
- Output Drive Capability: 10 LS-TTL Loads
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

Connection Diagram

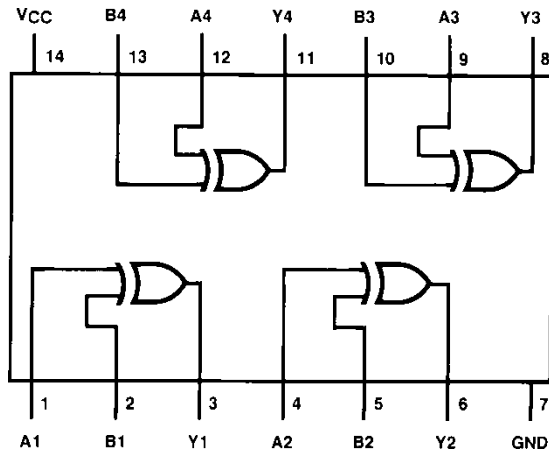
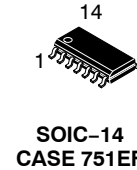
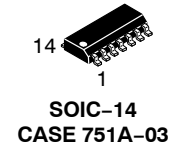


Figure 1. Pin Assignments (Top View)

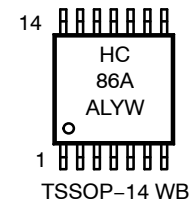
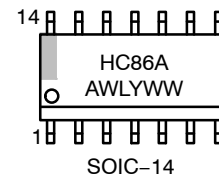
TRUTH TABLE

Inputs		Outputs
A	B	Y (Note1)
L	L	L
L	H	H
H	L	H
H	H	L

1. $Y = A \oplus B = \overline{A}B + A\overline{B}$



MARKING DIAGRAM



HC86A = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

MM74HC86

MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_{IN}	DC Input Voltage	-0.5	$V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage	-0.5	$V_{CC} + 0.5$	V
I_{IK}, I_{OK}	Clamp Diode Current	± 20		mA
I_{OUT}	DC Output Current, per Pin	± 25		mA
I_{CC}	DC V_{CC} or GND Current, per Pin	± 50		mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)	-	260	°C
P_D	Power Dissipation (Note 3), (Note 2)	-	600	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Power dissipation temperature derating – plastic “N” package: -12 mW/°C from 65°C to 85°C.

3. S.O. package only 500 mW.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		-55	+125	°C
t_r, t_f	Input Rise or Fall Times	$V_{CC} = 2.0\text{ V}$	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	500	
		$V_{CC} = 6.0\text{ V}$	-	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MM74HC86

DC CHARACTERISTICS (Note 4)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0	–	1.5	1.5	1.5	V
			4.5	–	3.15	3.15	3.15	
			6.0	–	4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage		2.0	–	0.5	0.5	0.5	V
			4.5	–	1.35	1.35	1.35	
			6.0	–	1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20 μA	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 4.0 mA	4.5	4.2	3.98	3.84	3.70	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 5.2 mA	6.0	5.7	5.48	5.34	5.20	
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20 μA	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 4.0 mA	4.5	0.2	0.26	0.33	0.4	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 5.2 mA	6.0	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0	–	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0 mA	6.0	–	2.0	20	40	μA

4. For a power supply of 5 V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} values at 5 V and 5.5 V are 3.5 V and 3.85 V, respectively.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occurs for CMOS at the higher voltage, so the 6.0 V values should be used.

AC CHARACTERISTICS (C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit	
				Typ	Guaranteed Limits				
t _{PHL} , t _{PLH}	Maximum Propagation Delay	C _L = 15 pF, t _R = t _F = 6 ns	5.0	12	–	20	–	ns	
t _{PHL} , t _{PLH}	Maximum Propagation Delay	C _L = 50 pF, t _R = t _F = 6 ns	2.0	60	120	151	179	ns	
			4.5	12	24	30	36		
			6.0	10	20	26	30		
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0	30	75	95	110	ns	
			4.5	8	15	19	22		
			6.0	7	13	16	19		
C _{PD}	Power Dissipation Capacitance (per Gate) (Note 5)				25	–	–	–	pF
C _{IN}	Maximum Input Capacitance				5	10	10	10	pF

5. C_{PD} determines the no-load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

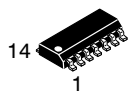
MM74HC86

ORDERING INFORMATION

Part Number	Package	Shipping†
MM74HC86M	SOIC-14, Case 751A-03 (Pb-Free, Halide Free)	55 Units / Tube
MM74HC86MTC	TSSOP-14, Case 948G-01 (Pb-Free, Halide Free)	96 Units / Tube
MM74HC86MX	SOIC-14, Case 751EF (Pb-Free, Halide Free)	2500 / Tape & Reel
MM74HC86MTCX	TSSOP-14, Case 948G-01 (Pb-Free, Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

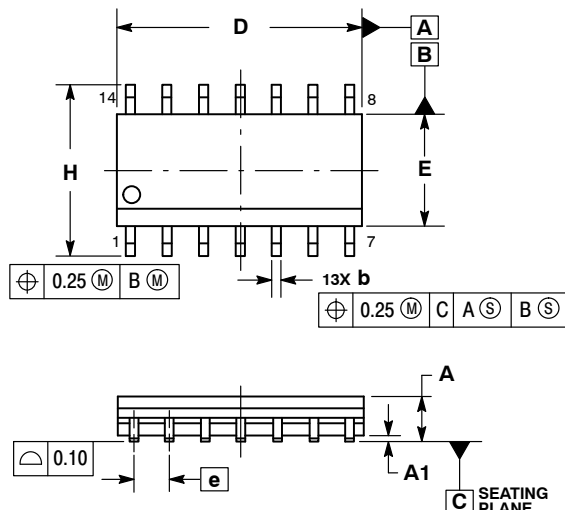
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

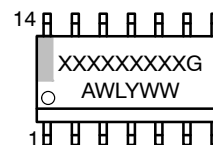
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

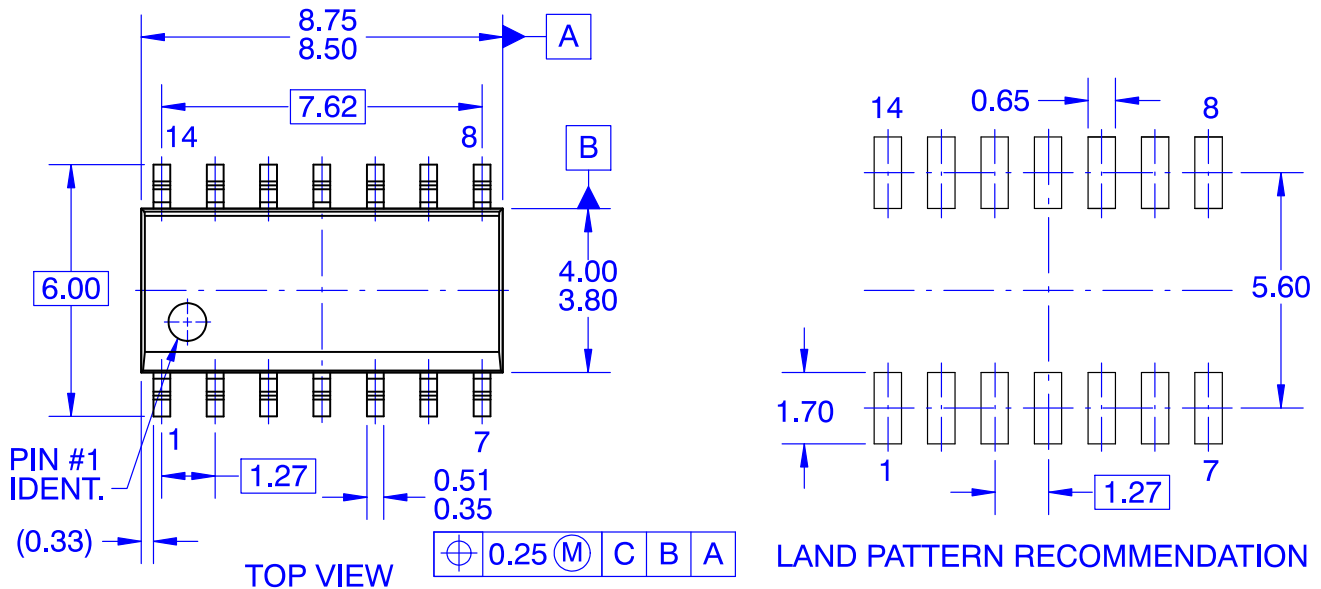
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

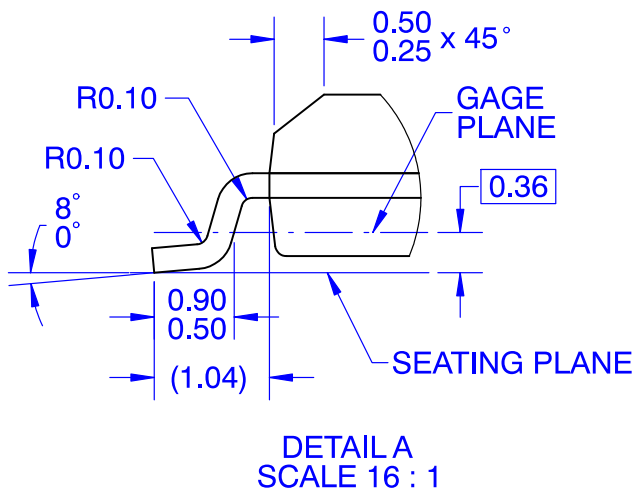
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



DOCUMENT NUMBER:	98AON13739G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC14	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales