

NLSF595

Serial (SPI) Tri-Color LED Driver

The NLSF595 is advanced CMOS shift register with open drain outputs fabricated with 0.6 μm silicon gate CMOS technology. This device is used in conjunction with a microcontroller, with only one dedicated line. All pins have Overvoltage Protection that allows voltages above V_{CC} up to 7.0 V to be present on the pins without damage or disruption of operation of the part, regardless of the operating voltage. This device may be used between 2.0 and 5.5 volts, the output driver level may be independent of supply voltage: 0–7.0 volts.

Features

- Parallel Outputs are Open Drain Capable of Sinking > 12 mA
 - ♦ Output Withstands up to +7.0 Regardless of V_{CC}
- Standard Serial (SPI) Interface, Data, Clock, Enable (Low)
- All Inputs CMOS Level Compatible
- Frees up I/O around a Microcontroller
- Only One Pin Dedicated to this Device (Latch Enable)
- Output Enable may be Permanently Pulled Low
- High Speed Clocking, $F_{max} > 25 \text{ MHz}$ (Shift Clock)
- Eight Bits Parallel Output
- Double Buffered Outputs, so Register may Fill without Affecting Output
- STD CMOS Serial Output, may be used to Cascade more than One Device
- Each Part Controls Two Tri-Color LEDs
- Two Devices can Control 5 Tri-Color LEDs
- Low Leakage: $I_{CC} = 2.0 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Latchup Performance Exceeds 100 mA
- QFN-16/TSSOP-16 Packages
- ESD Performance:
 - ♦ Human Body Model; > 2000 V
 - ♦ Machine Model; > 200 V
- Functionally Similar to the Popular 74VHC595
- These Devices are Pb-Free and are RoHS Compliant



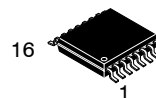
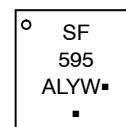
ON Semiconductor®

<http://onsemi.com>

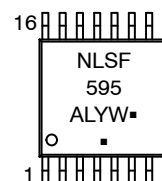
MARKING DIAGRAMS



QFN-16
MN SUFFIX
CASE 485G



TSSOP-16
DT SUFFIX
CASE 948F



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NLSF595

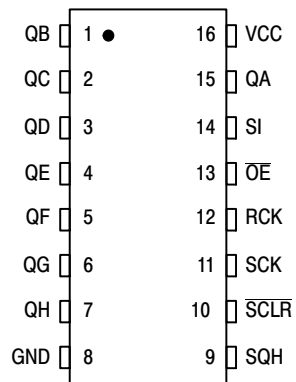


Figure 1. Pin Assignment (TSSOP-16)

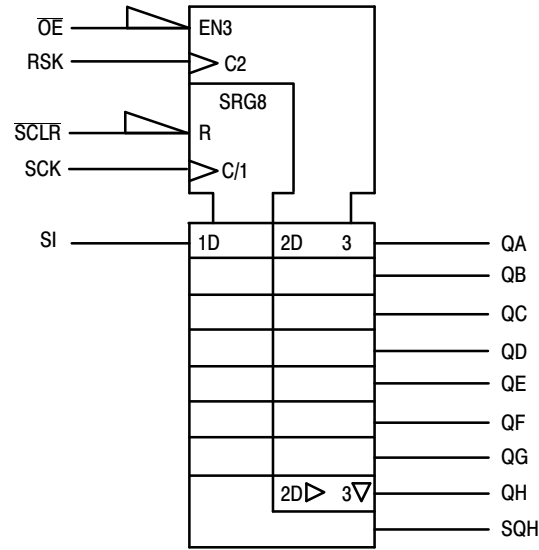


Figure 2. IEC Logic Symbol

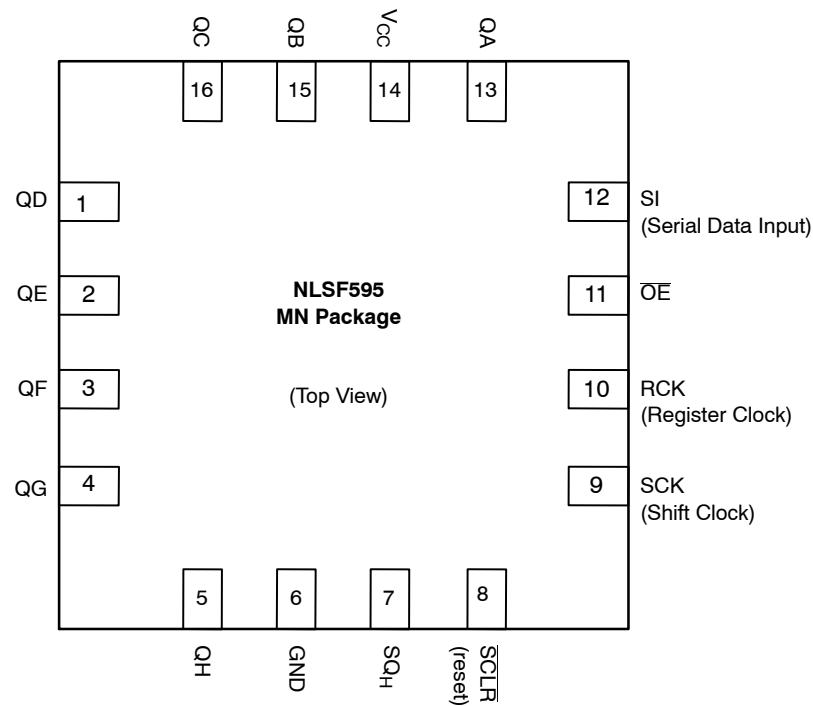


Figure 3. Pin Assignment (QFN-16)

NLSF595

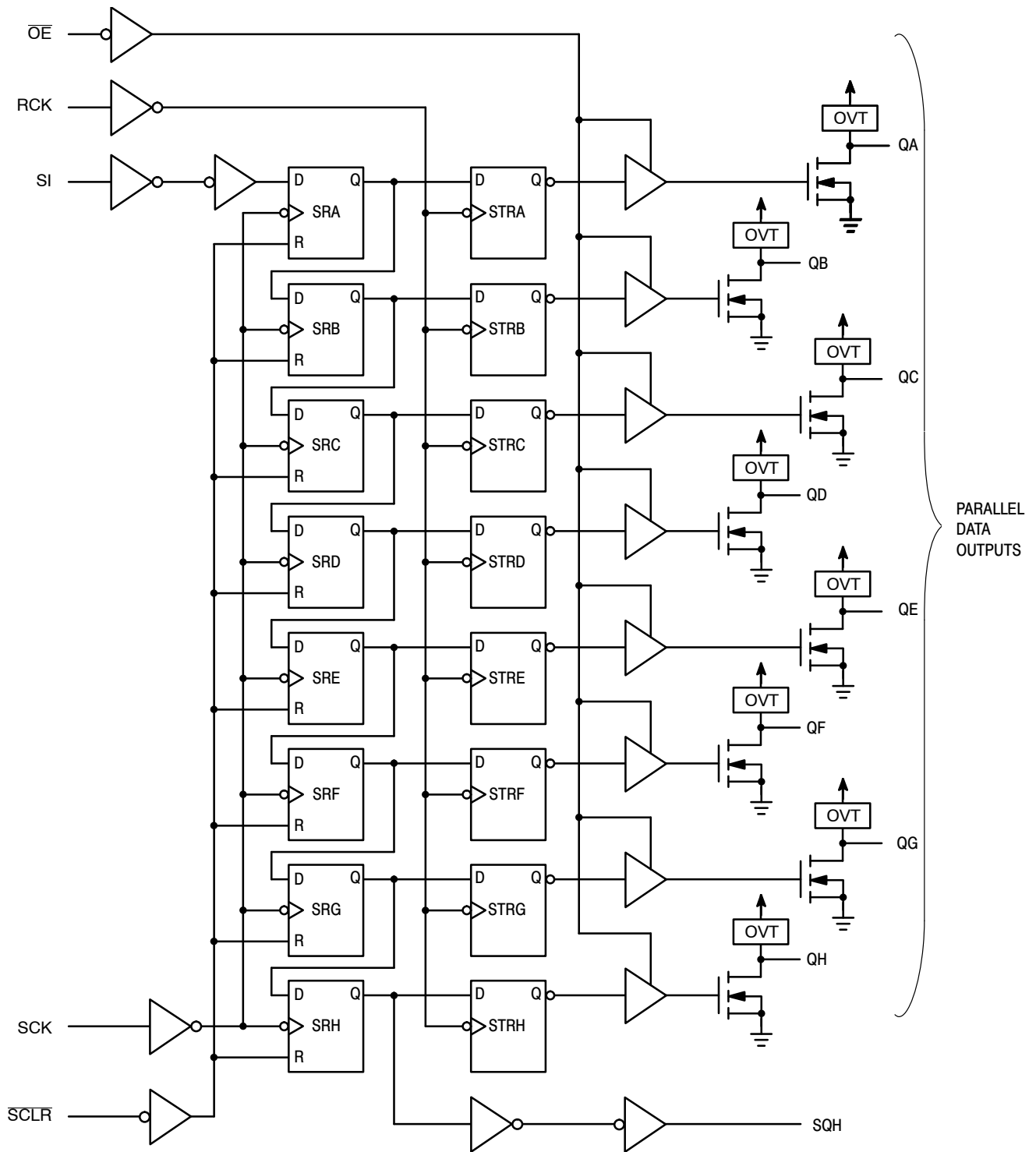


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V _{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	Digital Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} +7.0	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±50	mA
I _{OUT}	DC Output Current, per Pin	+50	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air	450	mW
T _{STG}	Storage Temperature Range	-65 to +150	°C
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 1)	±300	mA
θ _{JA}	Thermal Resistance, Junction-to-Ambient	128	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Units
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	-55	125	°C
t _r , t _f	Input Rise or Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0	50 15	ns/V

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset (SCLR)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable (OE)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D → SR _A ; SR _N → SR _{N+1}	U	SR _G → SR _H	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	SR _N → STR _N	*	SR _N
Storage register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents

D = data (L, H) logic level

↓ = High-to-Low

* = depends on Reset and Shift Clock inputs

STR = storage register contents

U = remains unchanged

↑ = Low-to-High

** = depends on Register Clock input

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65	V
V _{OH}	Minimum High-Level Serial Output Only Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
V _{OL2}	Maximum Low-Level Output Voltage with Max. Load V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 mA I _{OL} = 25 mA	3.0 4.5		0.8 0.5	1.0 0.6		1.1 0.7		1.25 0.8	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			4.0		40.0		40.0	µA
I _{OZ}	Three-State Output Off-State Current QA-QH	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.25		±2.5		±2.5	µA
I _{LKG}	Active (2) State Off Output Leakage Current QA-QH	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.25		±2.5		±2.5	µA
I _{OFF}	Power Off Output Leakage All Outputs	V _{IN} = 0 or 5.5 V V _{OUT} = 5.5 V	0			±0.25		±2.5		±2.5	µA

NLSF595

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Units
			Min	Typ	Max	Min	Max	Min	Max	
$f_{\max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V	80 135	150 185		70 115		70 115		MHz
t_{PLH} , t_{PHL}	Propagation Delay, SCK to SQH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF $V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		8.8 11.3 6.2 7.7	13.0 16.5 8.2 10.2	1.0 1.0 1.0 1.0	15.0 18.5 9.4 11.4	1.0 1.0 1.0 1.0	15.0 18.5 9.4 11.4	ns
t_{PHL}	Propagation Delay, SCLR to SQH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF $V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		8.4 10.9 5.9 7.4	12.8 16.3 8.0 10.0	1.0 1.0 1.0 1.0	13.7 17.2 9.1 11.1	1.0 1.0 1.0 1.0	13.7 17.2 9.1 11.1	ns
t_{PLZ}	Output Disable Time RCK to QA–QH Output Enable Time RCK to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF $V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		7.7 10.2 5.4 6.9	11.9 15.4 7.4 9.4	1.0 1.0 1.0 1.0	13.5 17.0 8.5 10.5	1.0 1.0 1.0 1.0	13.5 17.0 8.5 10.5	ns
t_{PZL}	Output Disable Time RCK to QA–QH Output Enable Time RCK to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF $V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		7.7 10.2 5.4 6.9	11.9 15.4 7.4 9.4	1.0 1.0 1.0 1.0	13.5 17.0 8.5 10.5	1.0 1.0 1.0 1.0	13.5 17.0 8.5 10.5	ns
t_{PZL}	Output Enable Time, OE to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1$ k Ω $C_L = 50$ pF $V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1$ k Ω $C_L = 50$ pF		7.5 9.0 4.8 8.3	11.5 15.0 8.6 10.6	1.0 1.0 1.0 1.0	13.5 17.0 10.0 12.0	1.0 1.0 1.0 1.0	13.5 17.0 10.0 12.0	ns
t_{PLZ}	Output Disable Time, OE to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1$ k Ω $V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1$ k Ω		12.1 7.6	15.7 10.3	1.0 1.0	16.2 11.0	1.0 1.0	16.2 11.0	ns
C_{IN}	Input Capacitance			4	10		10		10	pF
C_{OUT}	Three-State Output Capacitance (Output in High-Impedance State), QA–QH			6			10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 2)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		87	

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Units
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.8	–1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

NLSF595

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	V _{CC} V	T _A = 25°C		T _A = - 40 to 85°C	T _A = - 55 to 125°C	Units
			Typ	Limit	Limit	Limit	
t _{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	3.5 3.0	ns
t _{su(H)}	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	8.5 5.0	ns
t _{su(L)}	Setup Time, $\overline{\text{SCLR}}$ to RCK	3.3 5.0		8.0 5.0	9.0 5.0	9.0 5.0	ns
t _h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	1.5 2.0	ns
t _{h(L)}	Hold Time, $\overline{\text{SCLR}}$ to RCK	3.3 5.0		0 0	0 0	1.0 1.0	ns
t _{rec}	Recovery Time, $\overline{\text{SCLR}}$ to SCK	3.3 5.0		3.0 2.5	3.0 2.5	3.0 2.5	ns
t _w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns
t _{w(L)}	Pulse Width, $\overline{\text{SCLR}}$	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns

NLSF595

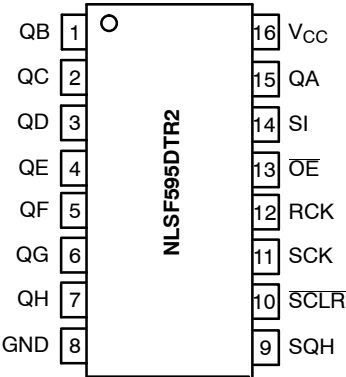
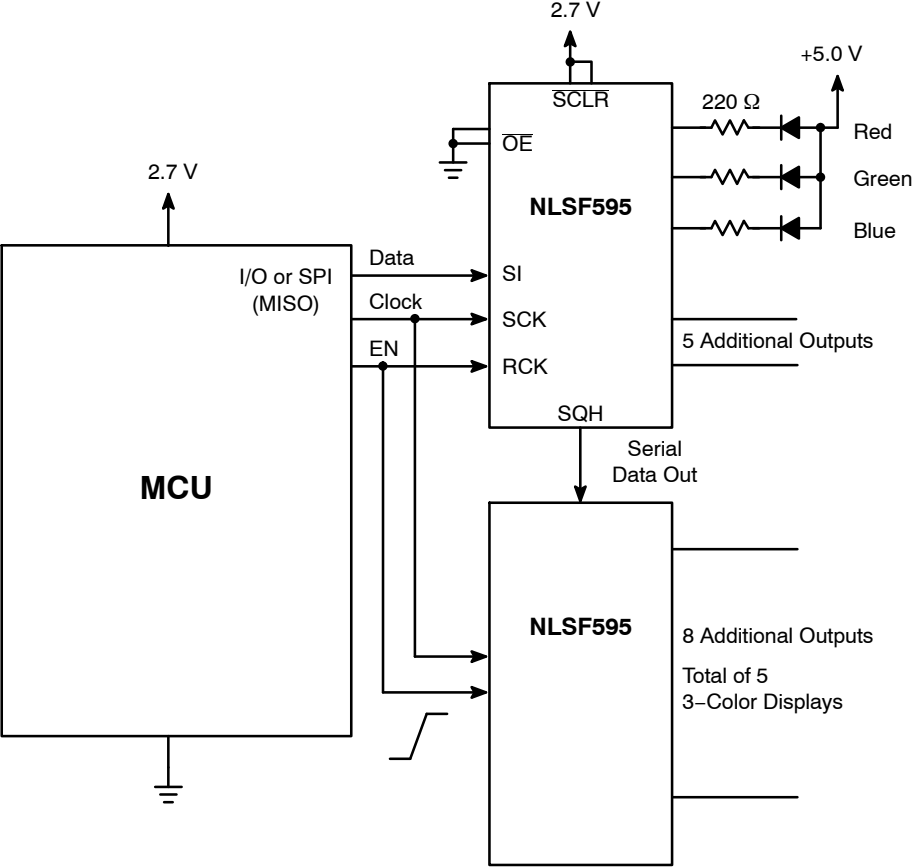


Figure 5. NLSF595 Shown Driving 5 3-Color LEDs

NLSF595

SWITCHING WAVEFORMS

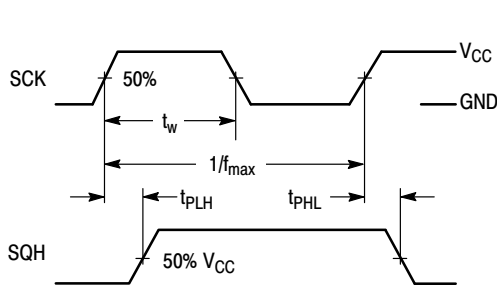


Figure 6.

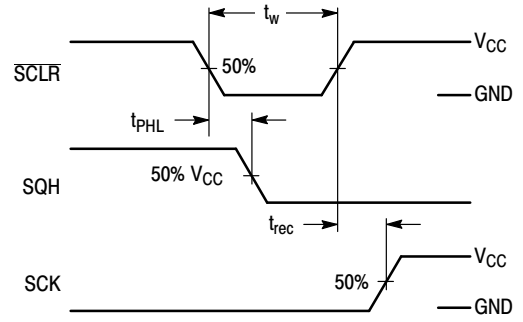


Figure 7.

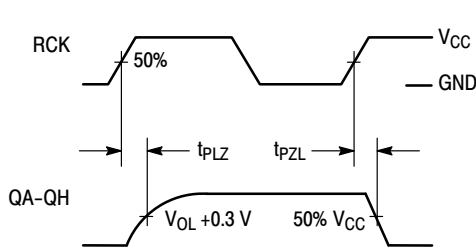


Figure 8.

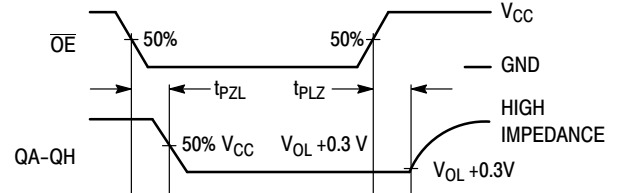


Figure 9.

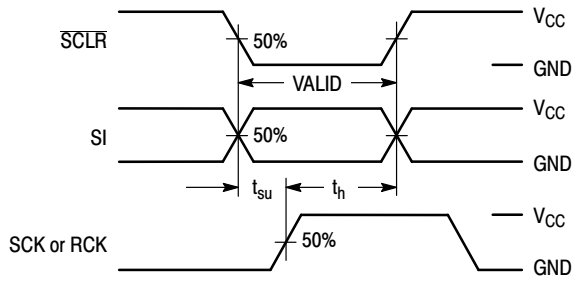


Figure 10.

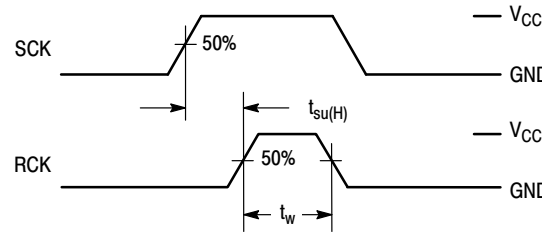
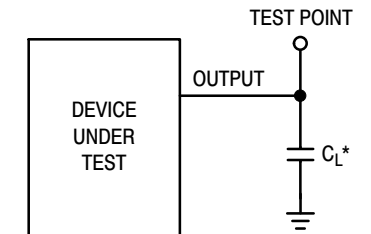


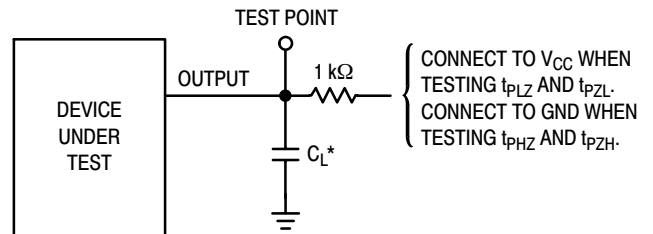
Figure 11.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 12.



*Includes all probe and jig capacitance

Figure 13.

NLSF595

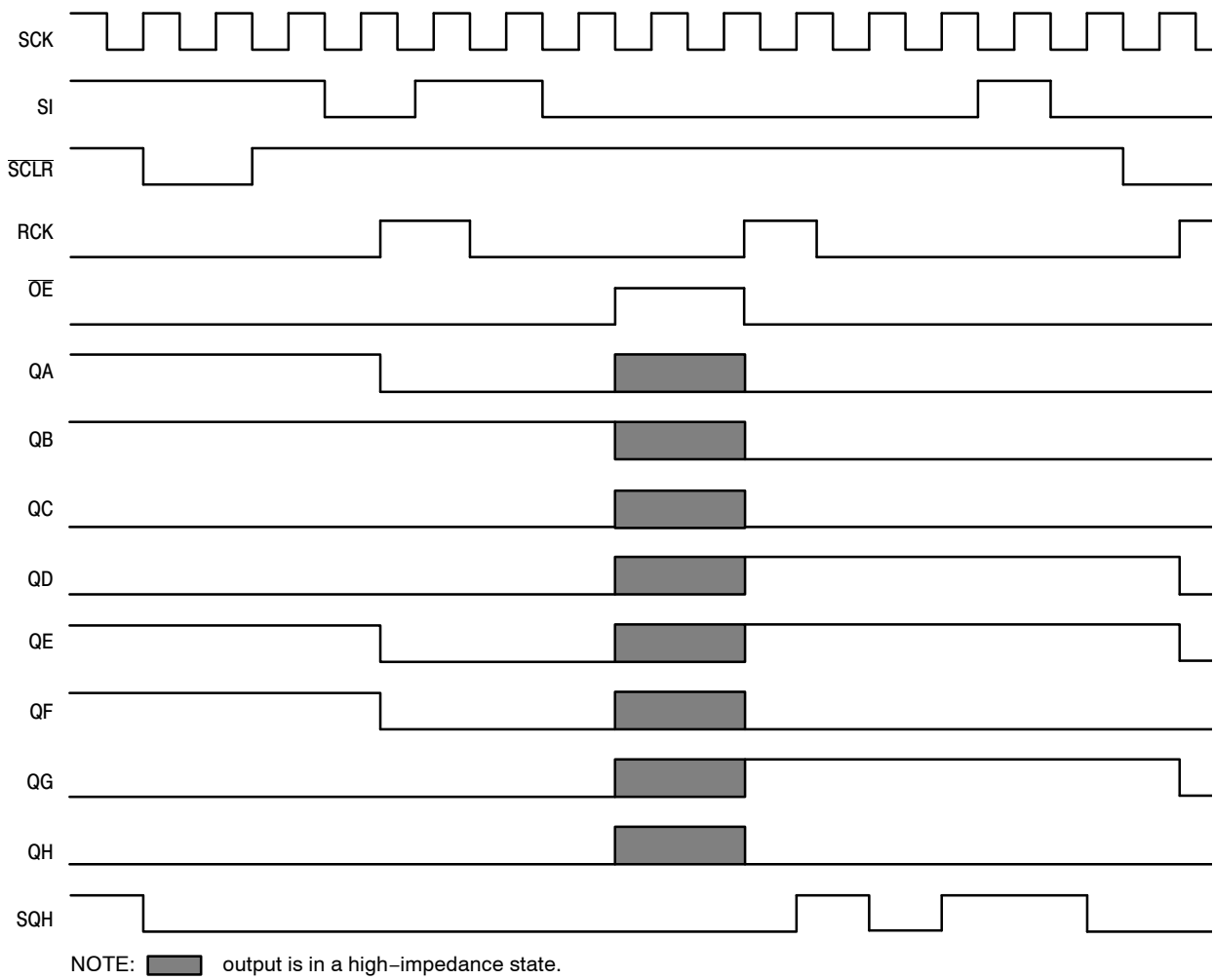


Figure 14. Timing Diagram

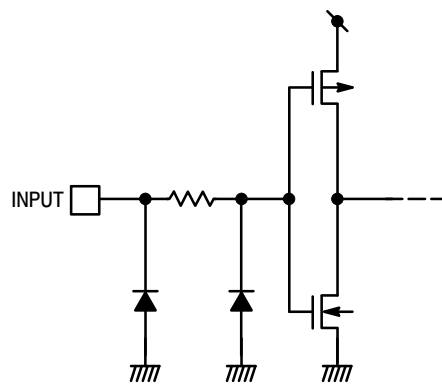


Figure 15. Input Equivalent Circuit

NLSF595

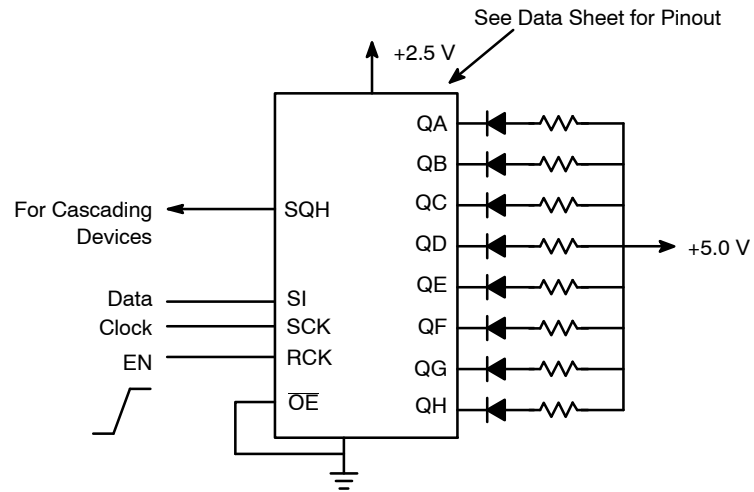
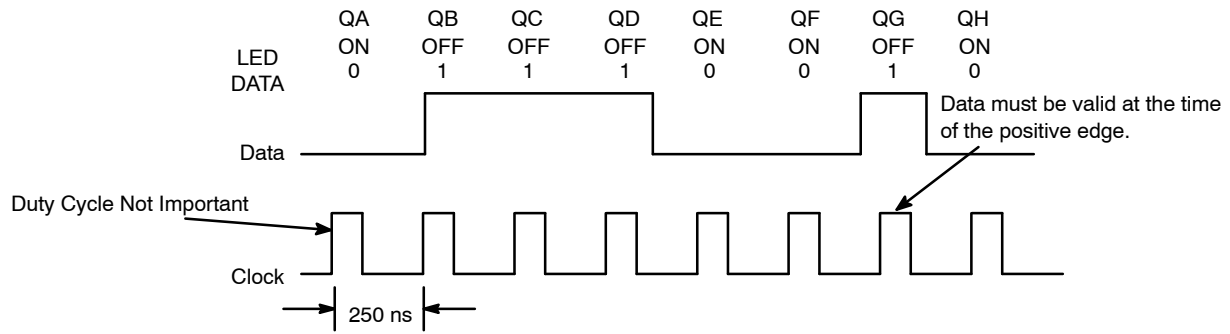


Figure 16. NLSF595 Example

NLSF595

ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package	Shipping [†]
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLSF595MNR2G	NL	SF	595	MN	R2	QFN (Pb-Free)	13-inch/3000 Unit
NLSF595DTR2G	NL	SF	595	DT	R2	TSSOP* (Pb-Free)	13-inch/2500 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

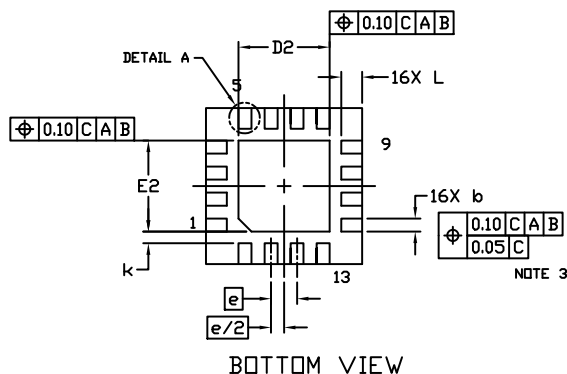
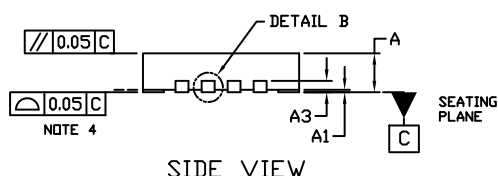
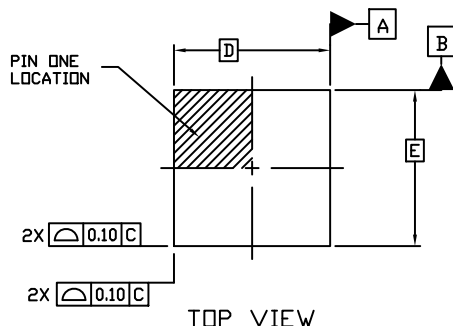
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

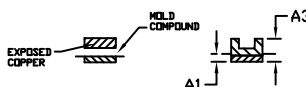
QFN16 3x3, 0.5P CASE 485G ISSUE G

DATE 08 OCT 2021

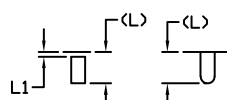


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



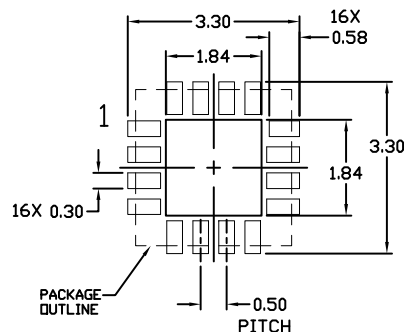
DETAIL B
ALTERNATE
CONSTRUCTIONS



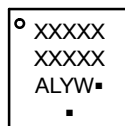
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

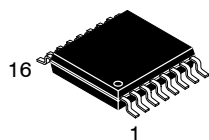
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON04795D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	QFN16 3X3, 0.5P	PAGE 1 OF 1

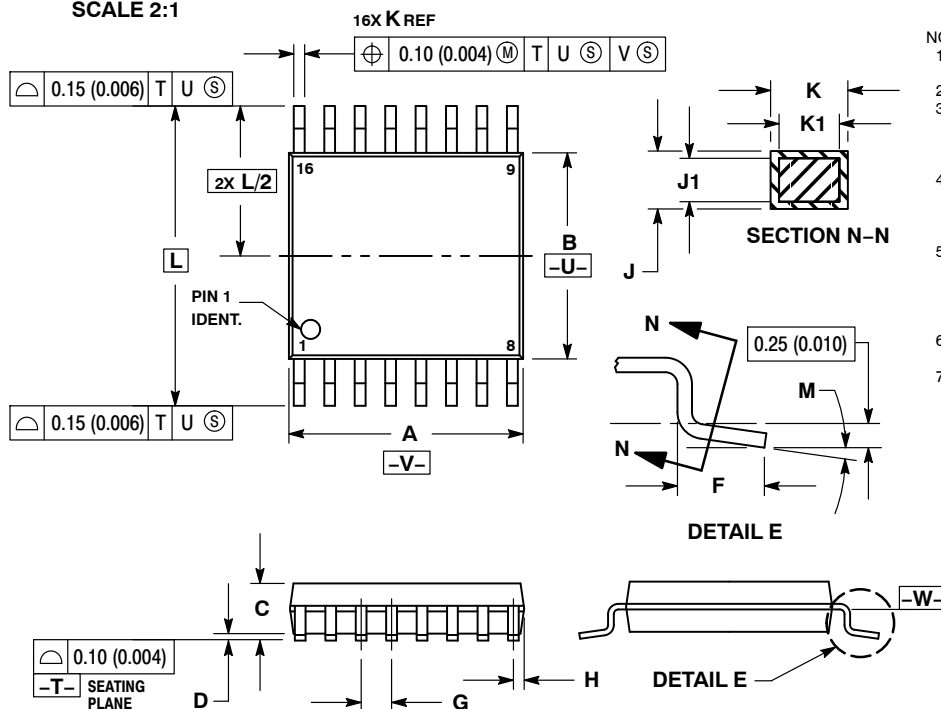
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

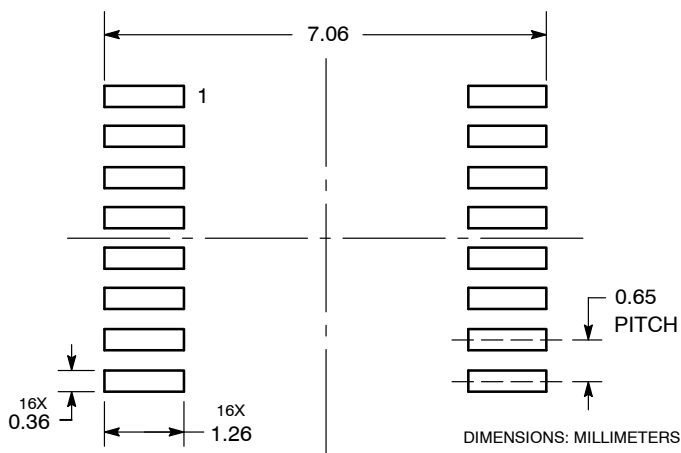


NOTES:

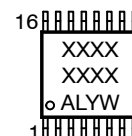
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales