

P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 40	0.054 at $V_{GS} = - 10$ V	- 4.5	9
	0.072 at $V_{GS} = - 4.5$ V	- 3.9	

FEATURES

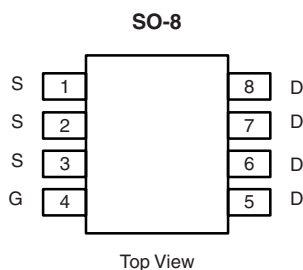
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested



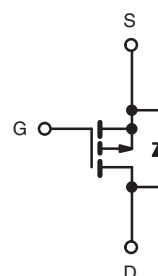
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- CCFL Inverter



Ordering Information: Si4447DY-T1-E3 (Lead (Pb)-free)
Si4447DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 40		V
Gate-Source Voltage		V_{GS}	± 16		
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) ^a	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	- 4.5	- 3.3	A
	$T_A = 70\text{ }^{\circ}\text{C}$		- 3.6	- 2.7	
Pulsed Drain Current		I_{DM}	- 30		
Continuous Source Current (Diode Conduction) ^a		I_S	- 1.7	- 0.9	
Avalanche Current	L = 0.1 mH	I_{AS}	16		
Single Pulse Avalanche Energy		E_{AS}	13		mJ
Maximum Power Dissipation ^a	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	2	1.1	W
	$T_A = 70\text{ }^{\circ}\text{C}$		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	50	62.5	$^\circ\text{C/W}$	
		85	110		
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

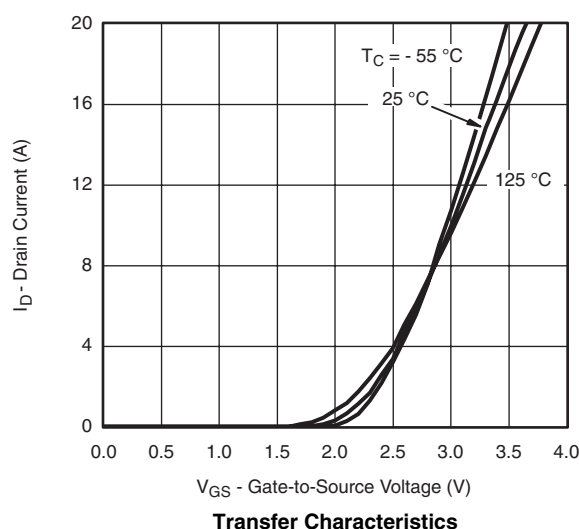
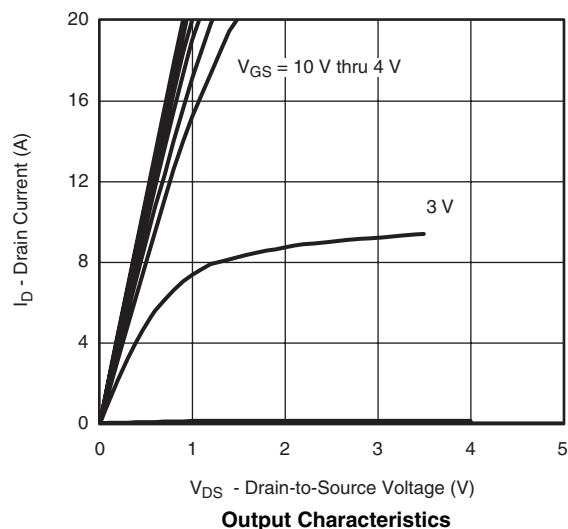
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-0.8		-2.2	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-40		mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.4		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 16\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -10\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -4.5\text{ A}$		0.045	0.054	Ω
		$V_{GS} = -15\text{ V}$, $I_D = -4.5\text{ A}$		0.059	0.072	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -4.5\text{ A}$		13		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\text{ A}$, $V_{GS} = 0\text{ V}$		-0.79	-1.2	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		805		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			85		
Total Gate Charge	Q_g	$V_{DS} = -20\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -4.5\text{ A}$		9	14	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$		11.5	18	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 6\text{ }\Omega$		8	13	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			74	110	
Fall Time	t_f			38	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$		27	45	nC
Body Diode Reverse Recovery Charge	Q_{rr}			17	26	

Notes:

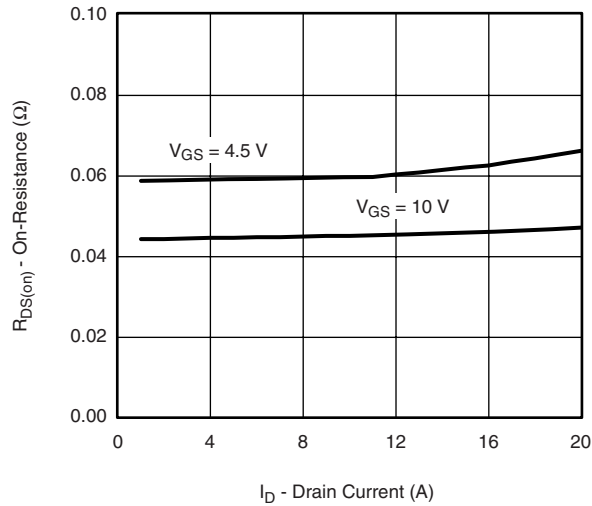
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

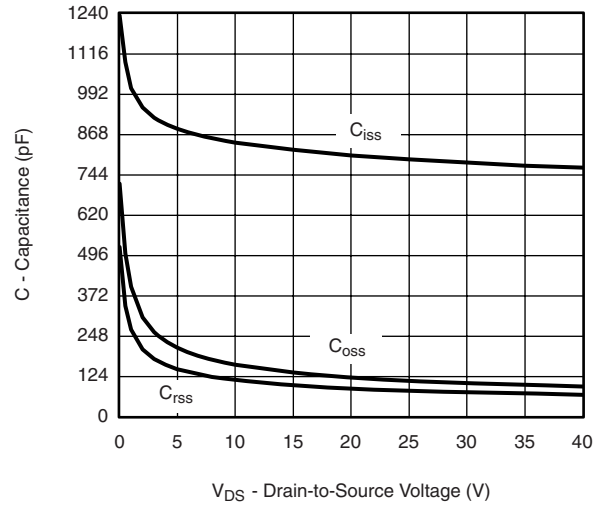
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted

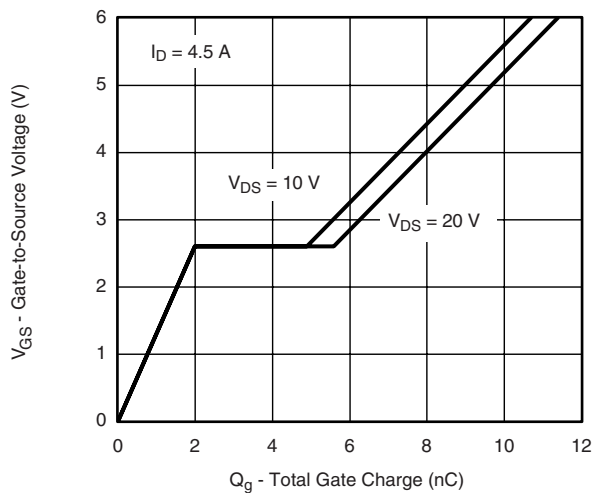
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



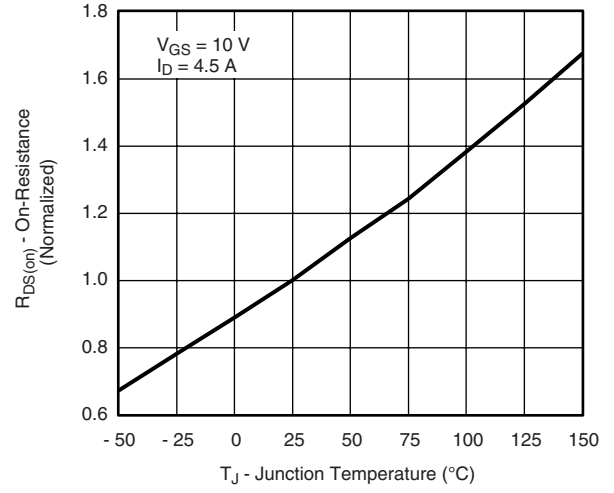
On-Resistance vs. Drain Current



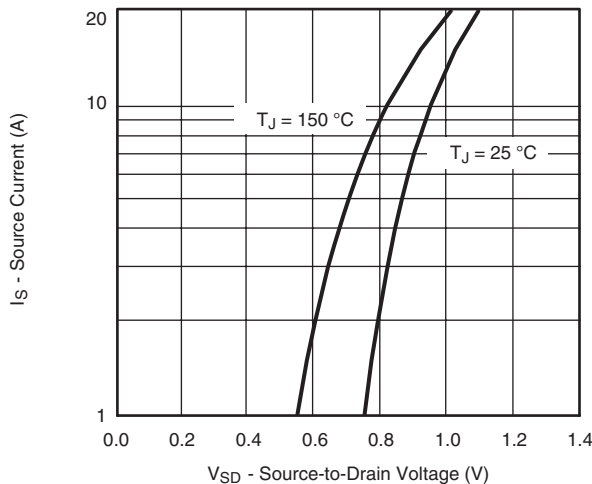
Capacitance



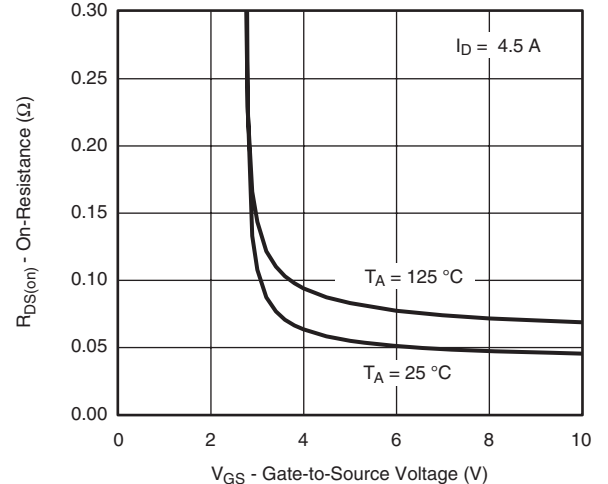
Gate Charge



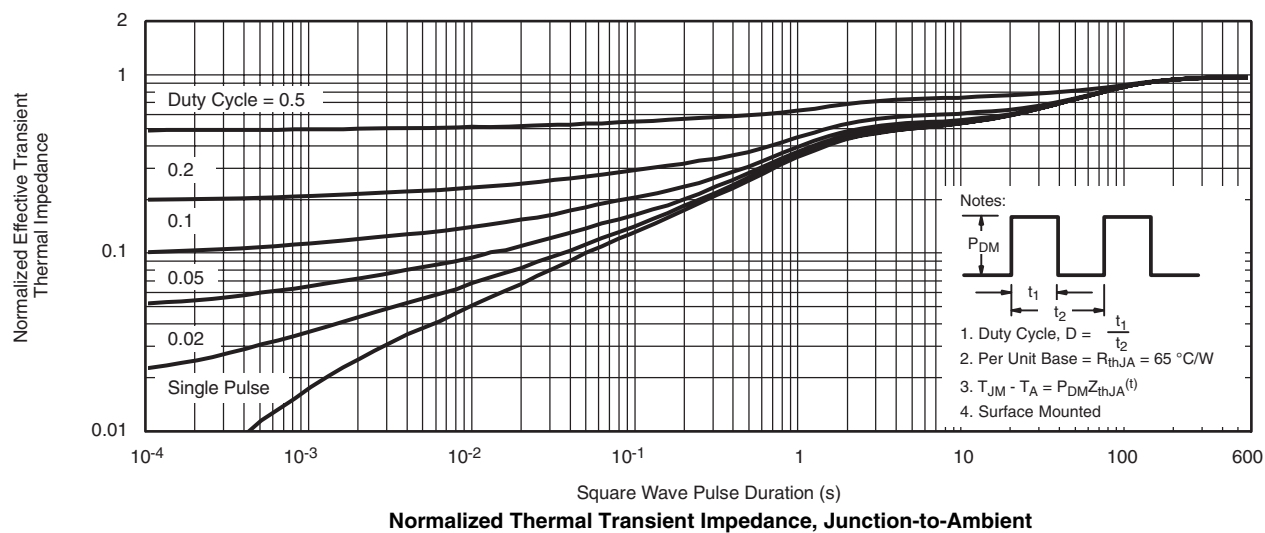
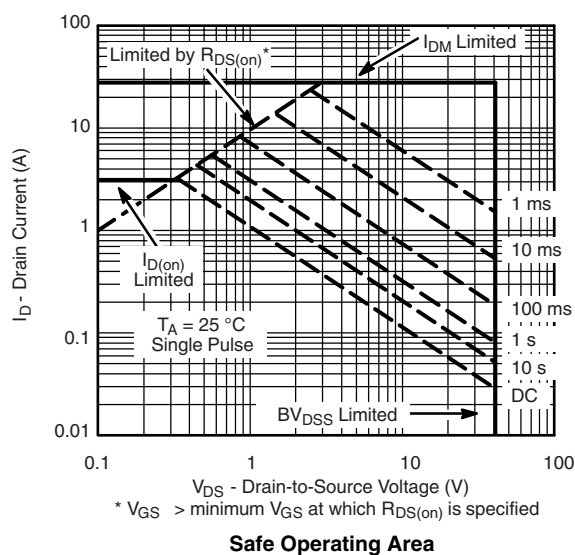
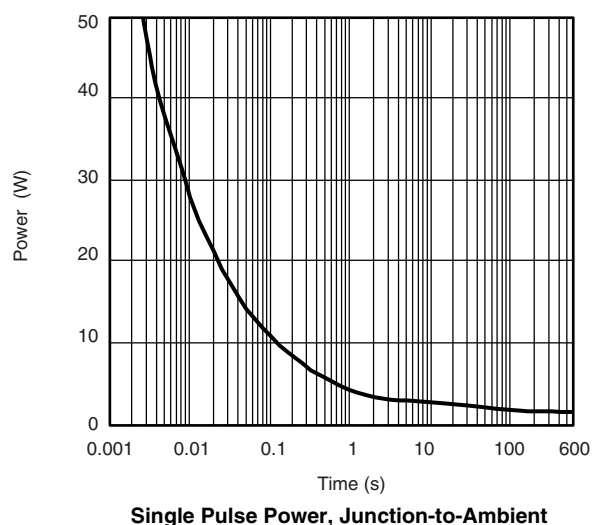
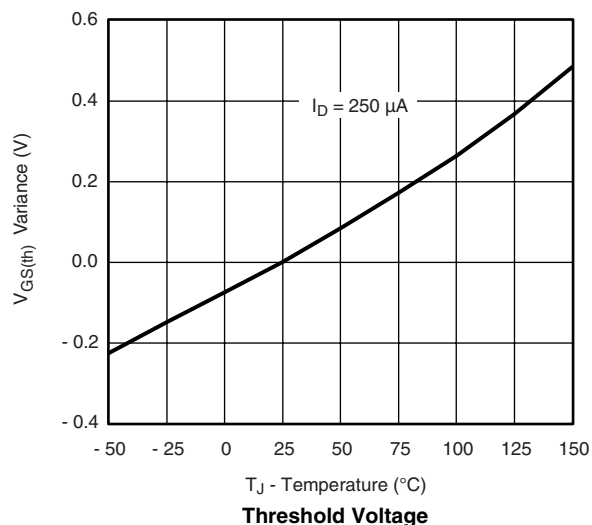
On-Resistance vs. Junction Temperature



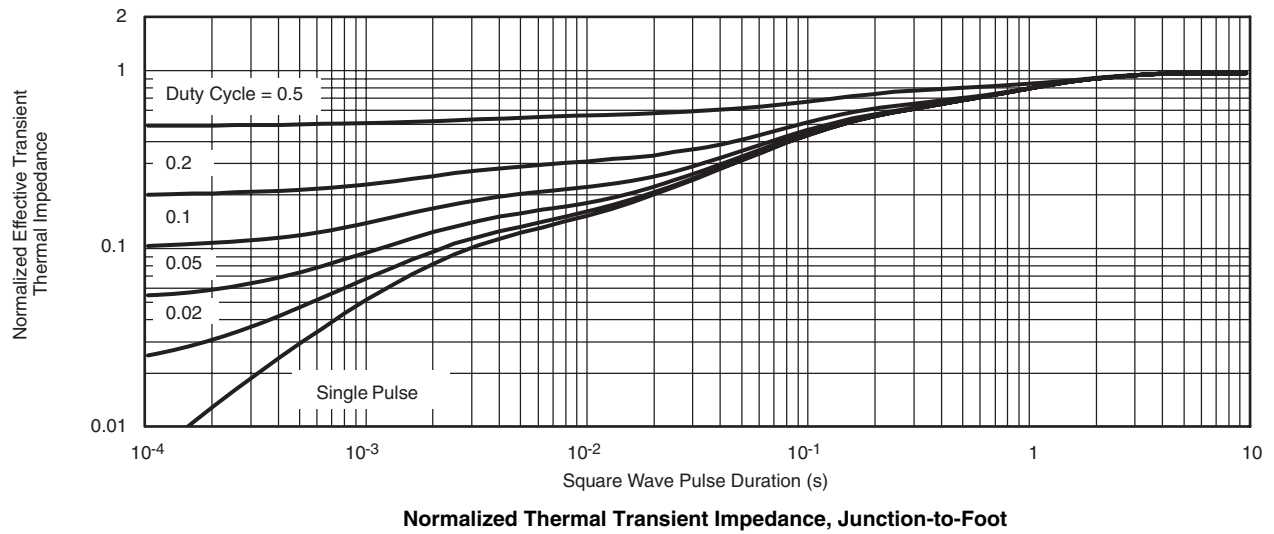
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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