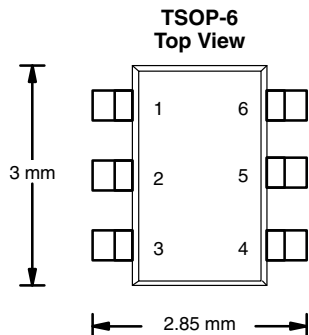


P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.0240 at $V_{GS} = - 4.5$ V	- 8 ^a	21 nC
	0.0372 at $V_{GS} = - 2.5$ V	- 8 ^a	



Ordering Information:

Si3407DV-T1-E3 (Lead (Pb)-free)
Si3407DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- PWM Optimized
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

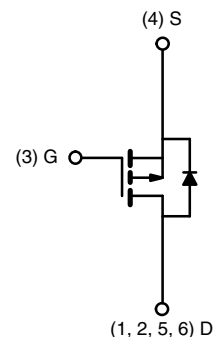
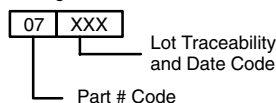


RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch
- Notebook PC

Marking Code



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	I_D	- 8 ^a	A
		- 8 ^a	
		- 7.5 ^{b, c}	
		- 6 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 25	mJ
Continuous Source-Drain Diode Current	I_S	- 3.5	
		- 1.7 ^{b, c}	
Avalanche Current	I_{AS}	- 8	
Single Pulse Avalanche Energy	E_{AS}	3.2	W
Maximum Power Dissipation	P_D	4.2	
		2.7	
		2 ^{b, c}	
		1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	45	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	25	30	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Maximum under steady state conditions is 110 °C/W.

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-18.7		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-0.65		-1.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	-25			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -7.5\text{ A}$		0.0200	0.0240	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -6.4\text{ A}$		0.0310	0.0327	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}$, $I_D = -7.5\text{ A}$		25		S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1670		pF
Output Capacitance	C_{oss}			335		
Reverse Transfer Capacitance	C_{rss}			284		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -7.5\text{ A}$		42	63	nC
				21	32	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -7.5\text{ A}$		6		
Gate-Drain Charge	Q_{gd}			5		
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.3	6.5	13	Ω
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}$, $R_L = 1.7\text{ }\Omega$ $I_D \cong -6\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$		8	16	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			65	98	
Fall Time	t_f			39	59	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}$, $R_L = 1.7\text{ }\Omega$ $I_D \cong -6\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$		32	48	
Rise Time	t_r			62	93	
Turn-Off Delay Time	$t_{d(off)}$			53	80	
Fall Time	t_f			38	57	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			-3.5	A
Pulse Diode Forward Current ^a	I_{SM}				-25	
Body Diode Voltage	V_{SD}	$I_S = -6\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		37	56	ns
Body Diode Reverse Recovery Charge	Q_{rr}			22	33	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			25		

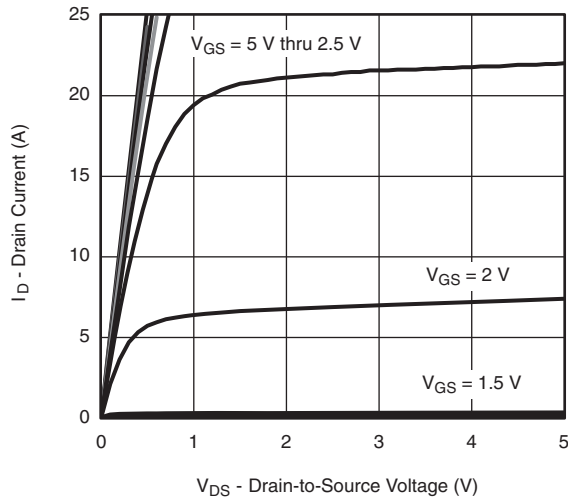
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

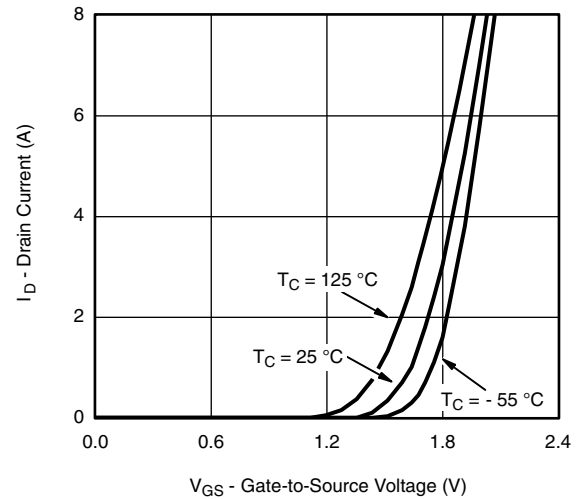
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

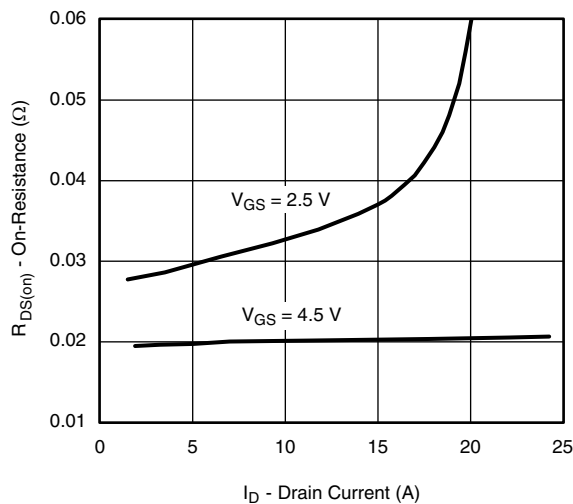
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



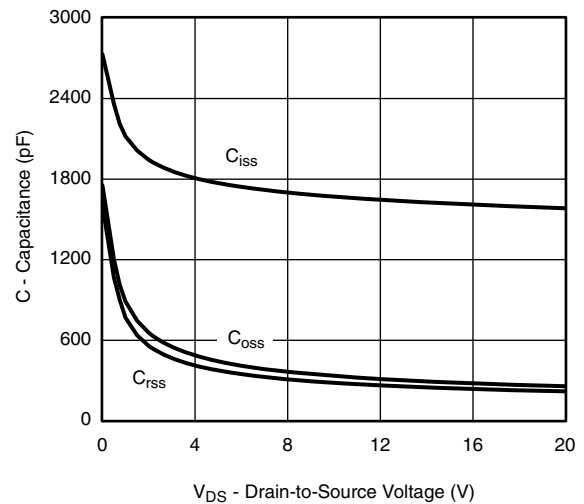
Output Characteristics



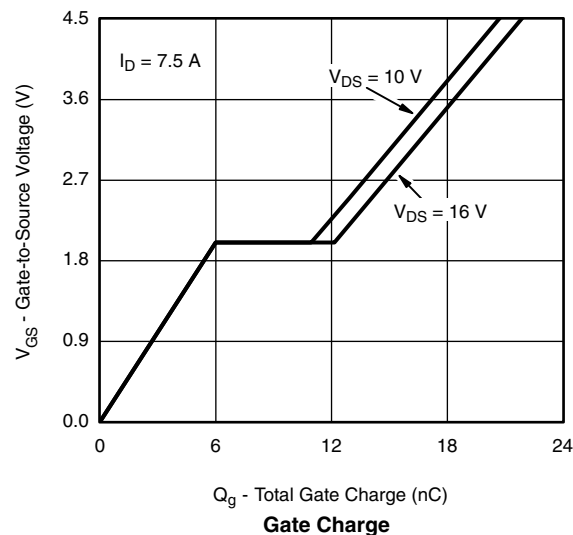
Transfer Characteristics



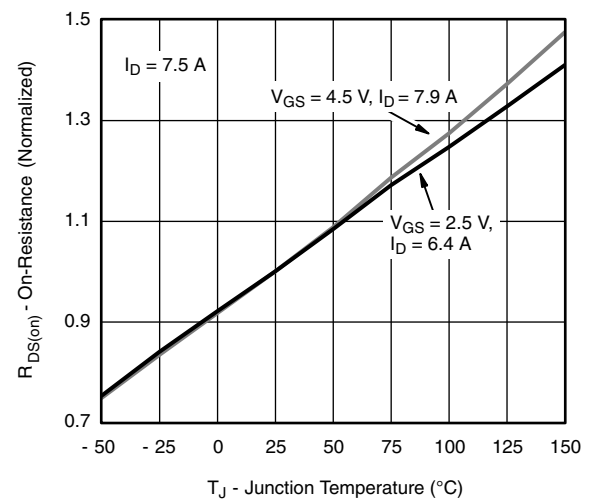
On-Resistance vs. Drain Current and Gate Voltage



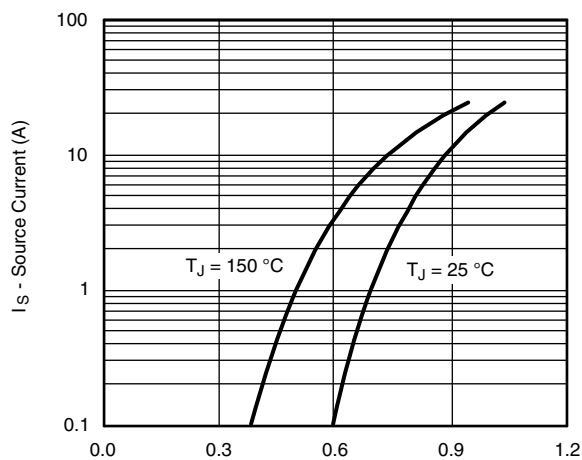
Capacitance



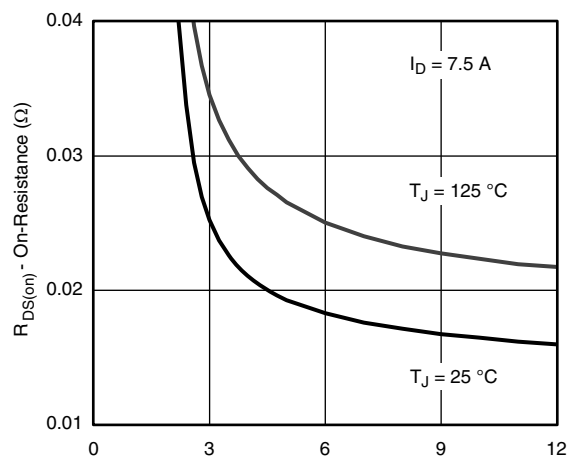
Gate Charge



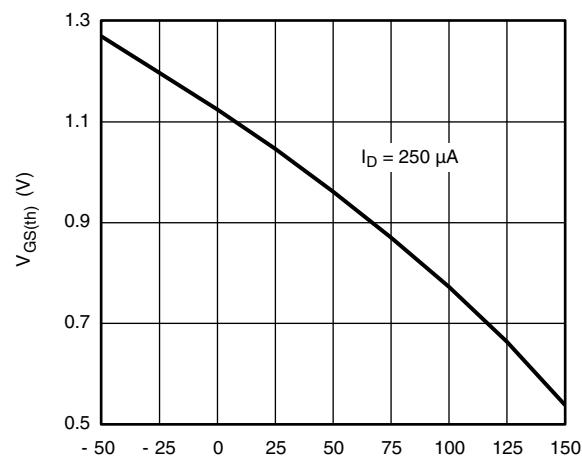
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

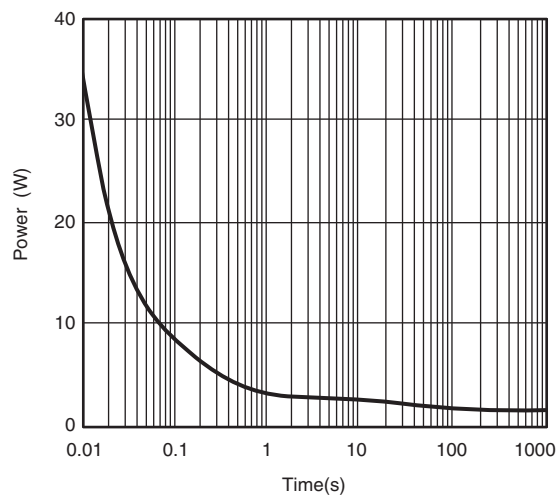
Source-Drain Diode Forward Voltage



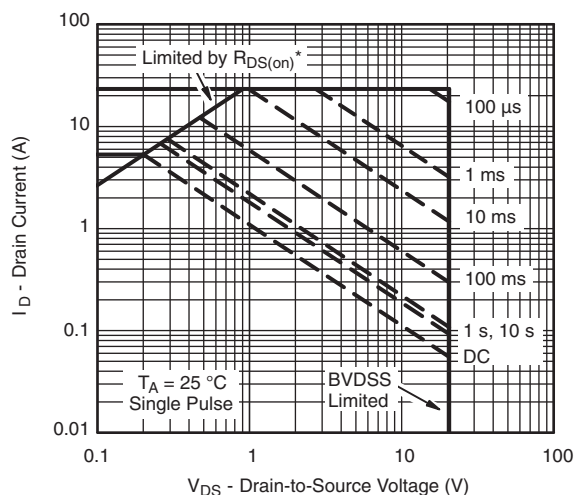
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



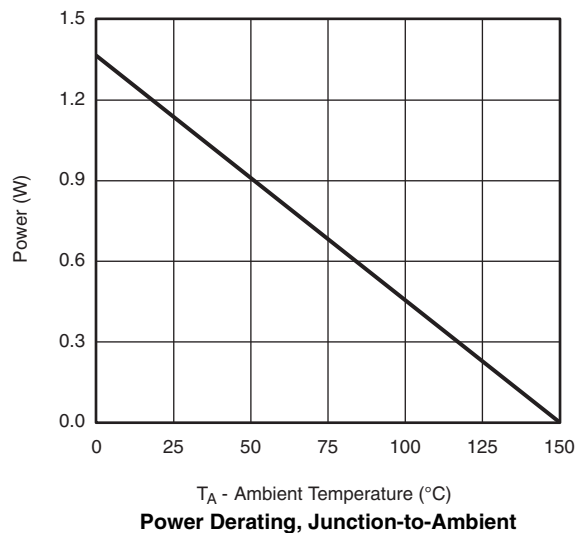
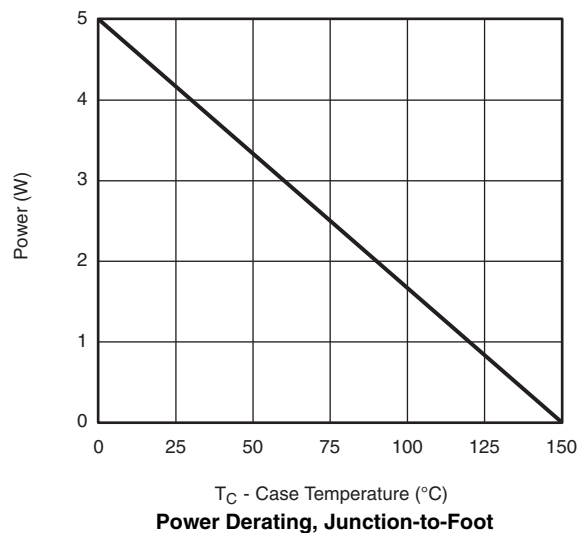
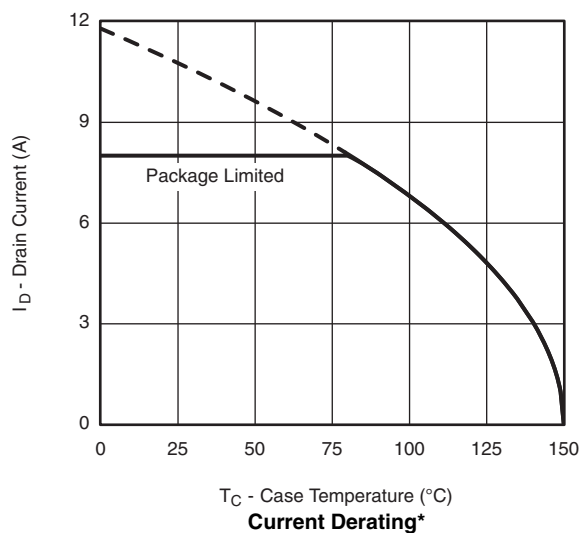
Single Pulse Power



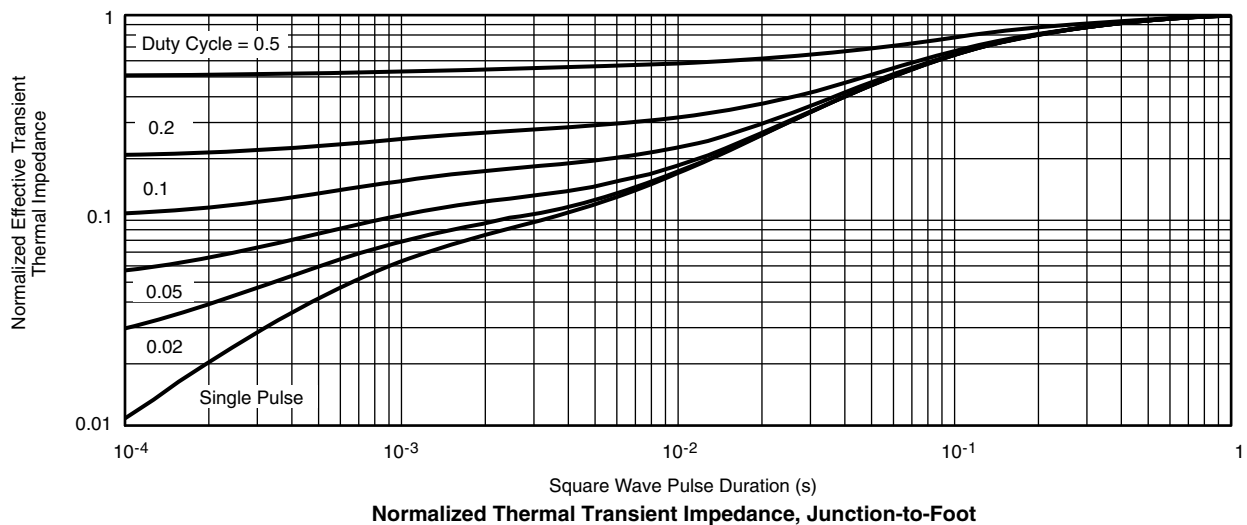
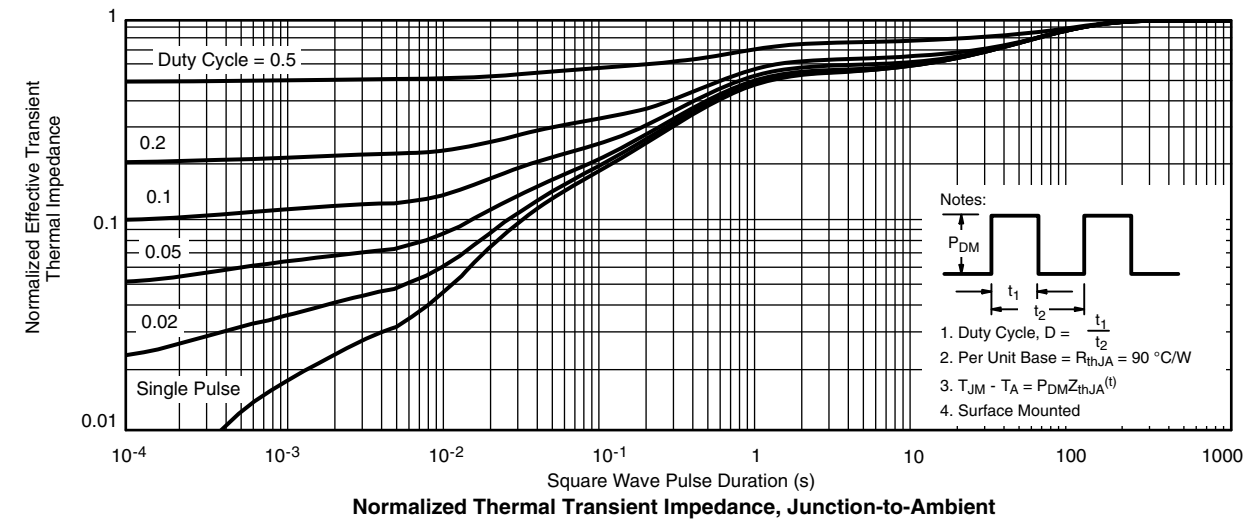
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69987.

TSOP: 5/6-LEAD

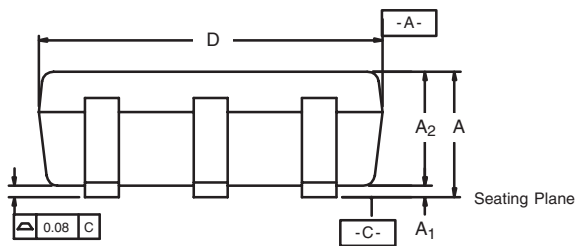
JEDEC Part Number: MO-193C



5-LEAD TSOP

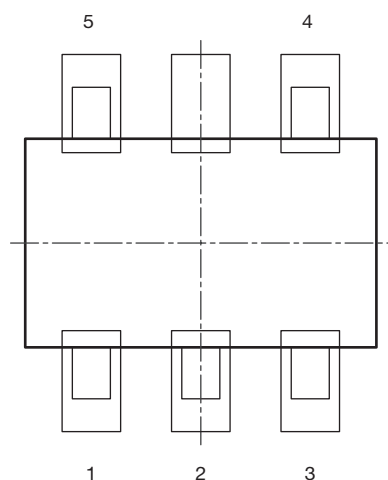


6-LEAD TSOP

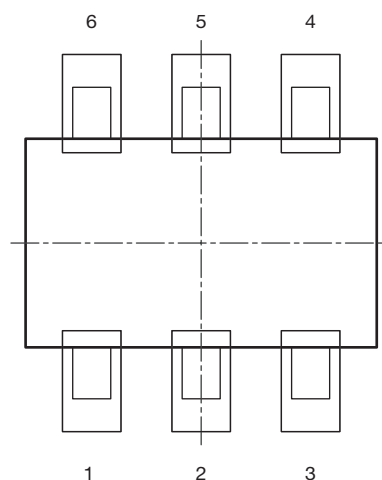


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

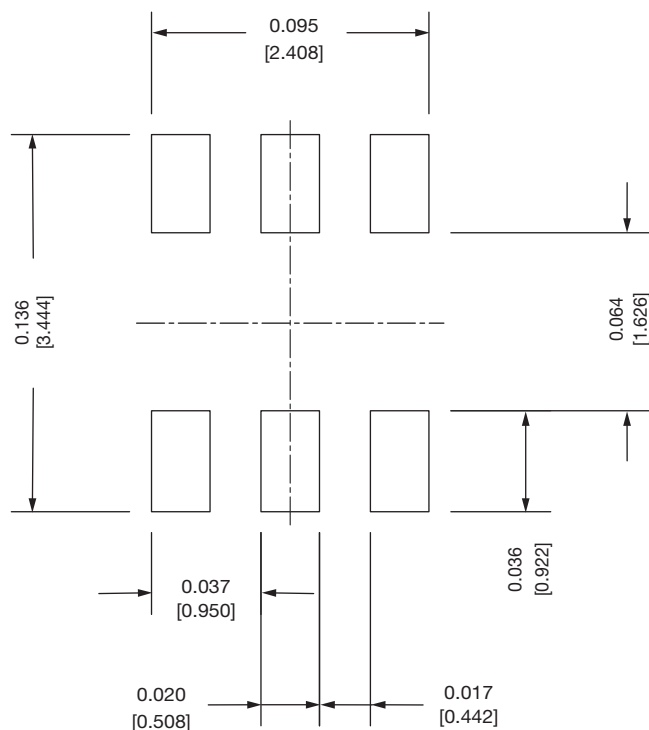
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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