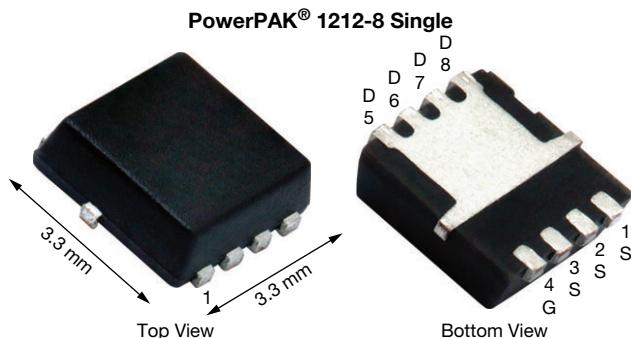


N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0088
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0120
Q_g typ. (nC)	9.9
I_D (A)	16 a, g
Configuration	Single

FEATURES

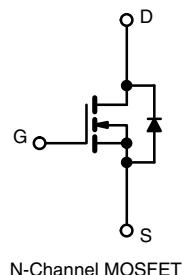
- TrenchFET® Gen IV power MOSFET
- Tuned for reducing transient spikes
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck converter
- High power density DC/DC
- Motor drive control
- Battery management
- Load switch



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK 1212-Single
Lead (Pb)-free and halogen-free	SiSA96DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20 / -16	
Continuous drain current ($T_J = 150$ °C)	I_D	16 a	A
		12 a	
		14.8 b, c	
		12 b, c	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	65	A
Continuous source-drain diode current	I_S	16 a	
		3.2 b, c	mJ
Single pulse avalanche current	I_{AS}	15	
Single pulse avalanche energy	E_{AS}	11.25	W
Maximum power dissipation	P_D	26.5	
		17	
		3.5 c	
		2.3 b, c	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b	$t \leq 10$ s	R_{thJA}	28	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	3.8	
4.7				

Notes

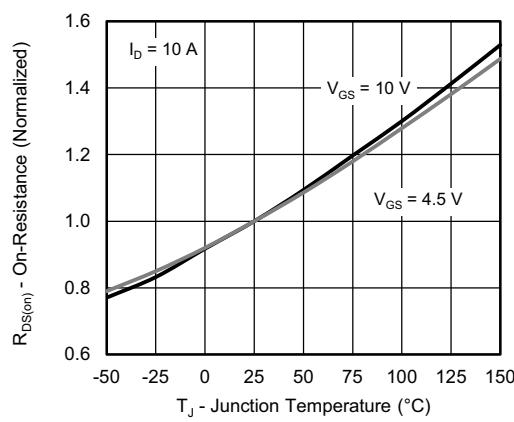
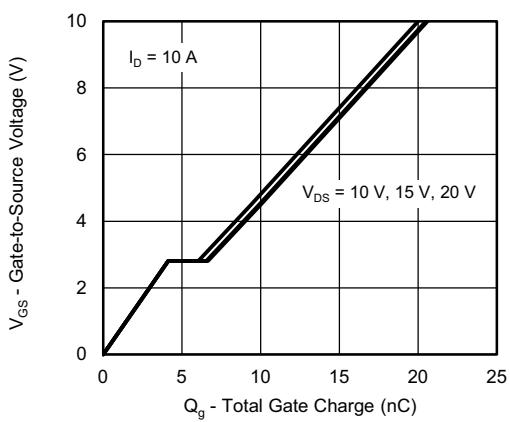
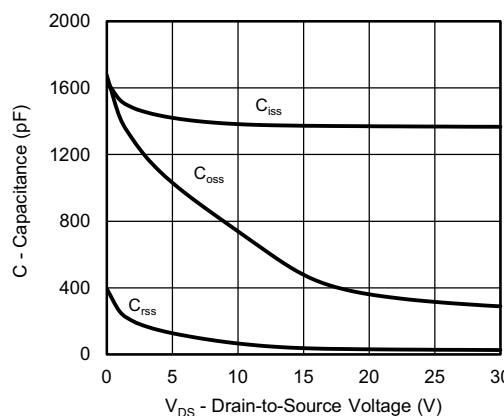
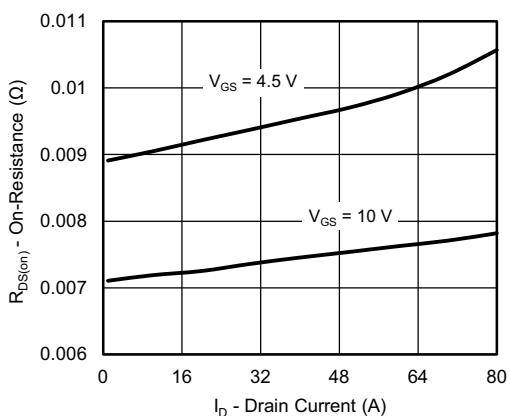
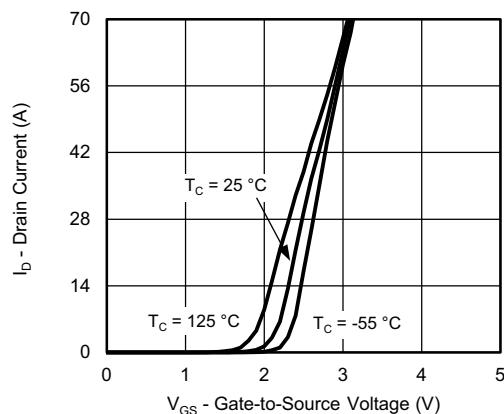
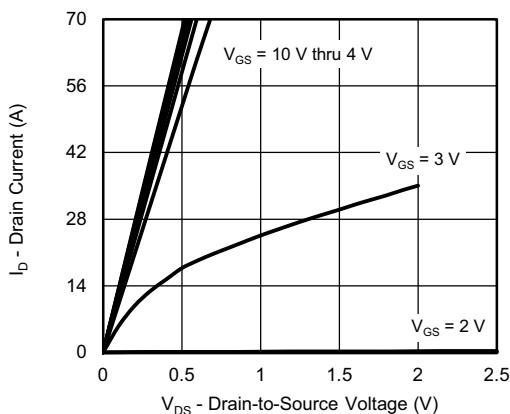
- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See solder profile (www.vishay.com/doc?273257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- $T_C = 25$ °C.

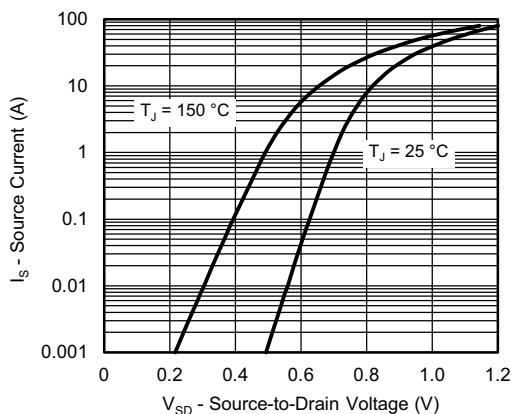
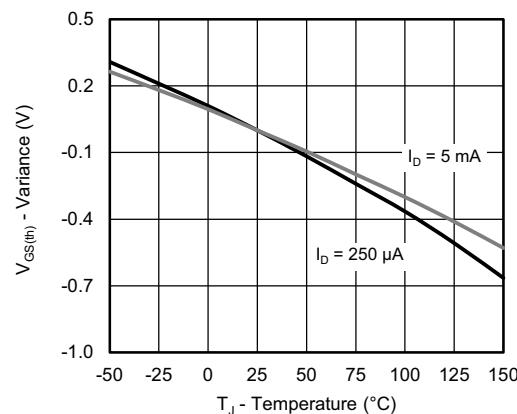
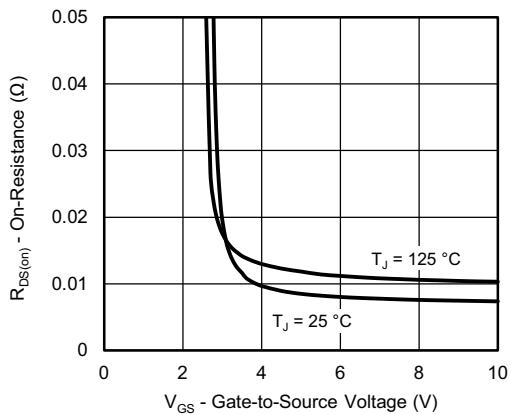
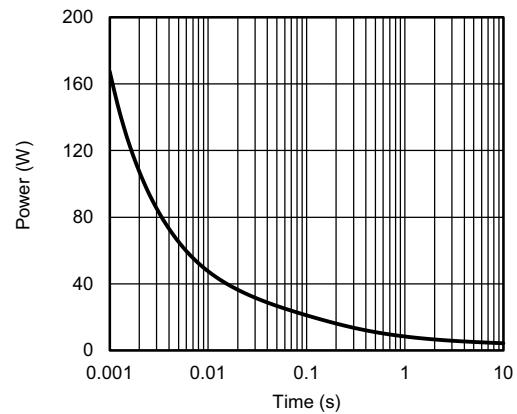
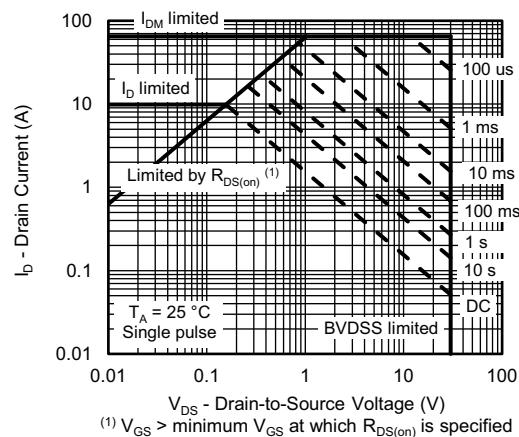
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30	-	-	V	
Drain-source breakdown voltage (transient) ^a	V_{DSt}	$V_{GS} = 0\text{ V}$, $I_{D(\text{aval})} = 15\text{ A}$, $t_{\text{transient}} = 50\text{ ns}$	36	-	-		
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	13	-	$\text{mV}/^\circ\text{C}$	
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-4.7	-		
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	-	2.2	V	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = +20\text{ }/-16\text{ V}$	-	-	100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA	
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 70^\circ\text{C}$	-	-	15		
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 10\text{ V}$, $V_{GS} = 10\text{ V}$	30	-	-	A	
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	0.0073	0.0088	Ω	
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	-	0.0092	0.0120		
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 10\text{ A}$	-	70	-	S	
Dynamic^b							
Input capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	1385	-	pF	
Output capacitance	C_{oss}		-	478	-		
Reverse transfer capacitance	C_{rss}		-	37	-		
Total gate charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	20.5	31	nC	
Gate-source charge	Q_{gs}	$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	-	9.9	15		
Gate-drain charge	Q_{gd}		-	4.2	-		
Gate resistance	R_g		-	2.5	-		
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$, $I_D \approx 10\text{ A}$, $V_{\text{GEN}} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	0.2	0.73	1.4	ns
Rise time	t_r		-	8	16		
Turn-off delay time	$t_{d(\text{off})}$		-	25	50		
Fall time	t_f		-	13	26		
Turn-on delay time	$t_{d(\text{on})}$		-	9	18		
Rise time	t_r	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$, $I_D \approx 10\text{ A}$, $V_{\text{GEN}} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	12	24	ns	
Turn-off delay time	$t_{d(\text{off})}$		-	47	94		
Fall time	t_f		-	15	30		
			-	25	50		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	16	A	
Pulse diode forward current	I_{SM}		-	-	50		
Body diode voltage	V_{SD}	$I_S = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.77	1.1	V	
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	50	100	ns	
Body diode reverse recovery charge	Q_{rr}		-	75	150	nC	
Reverse recovery fall time	t_a		-	43	-	ns	
Reverse recovery rise time	t_b		-	7	-		

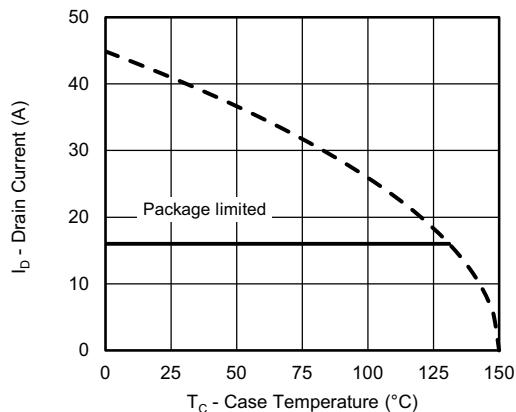
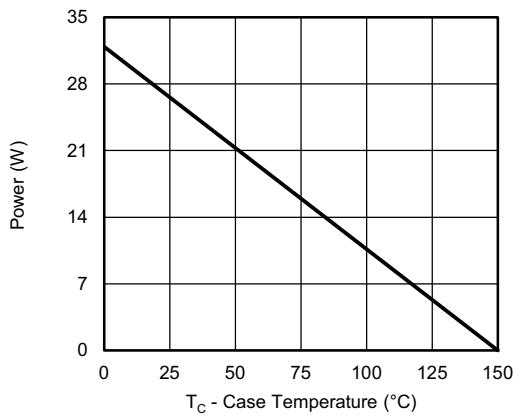
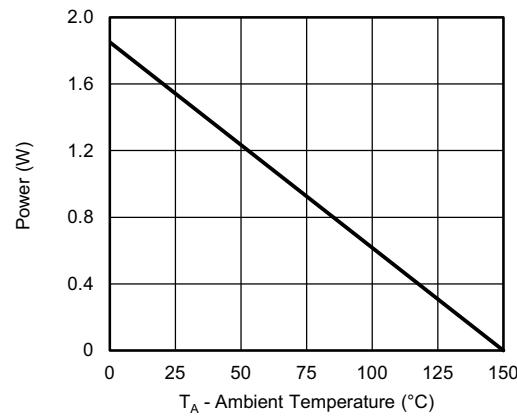
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ \%}$.
- b. Guaranteed by design, not subject to production testing.
- c. $T_{\text{CASE}} = 25^\circ\text{C}$. Expected voltage stress during 100 % UIS test. Production datalog is not available.

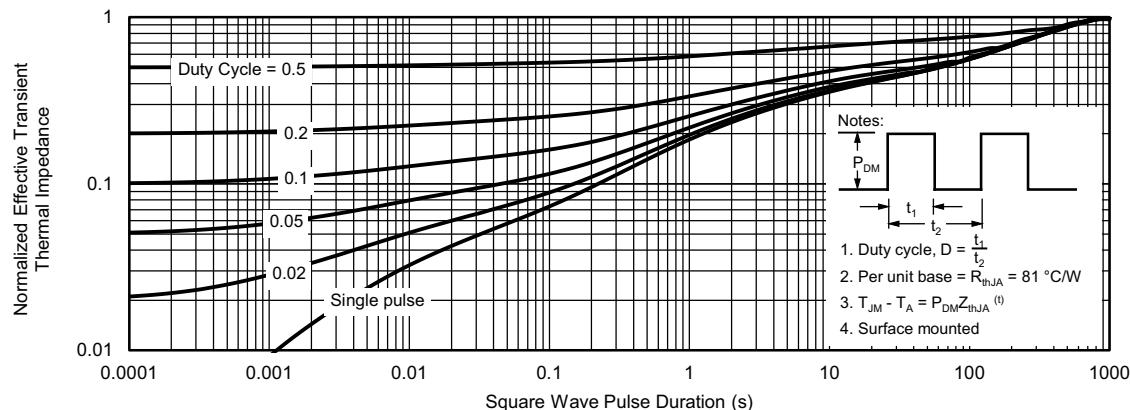
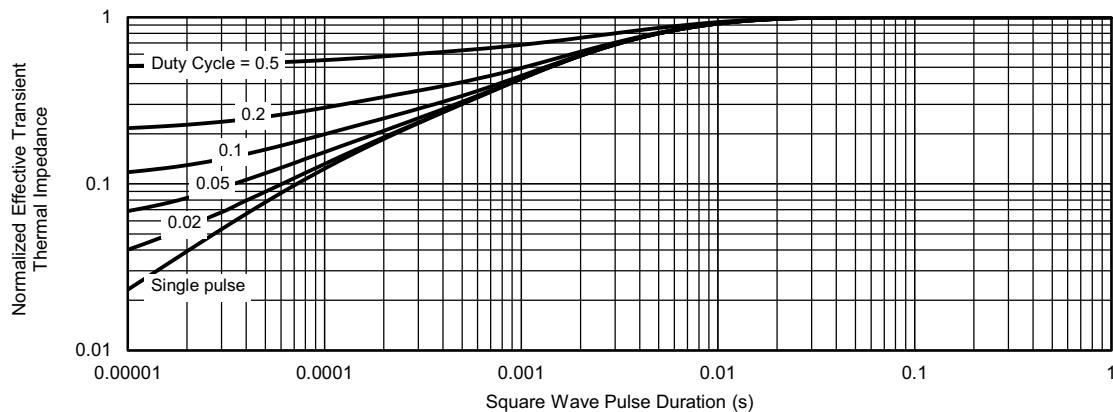
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

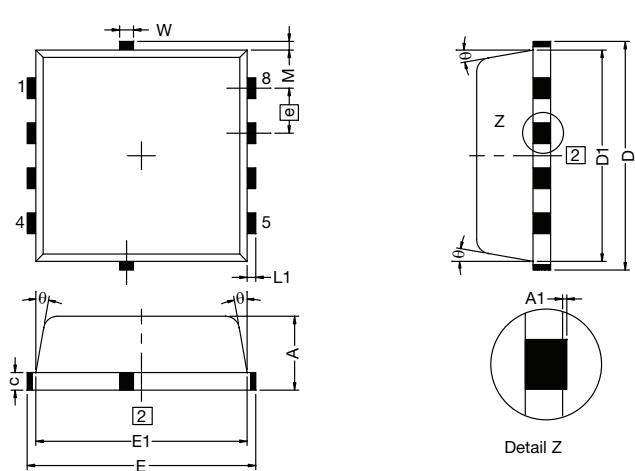
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

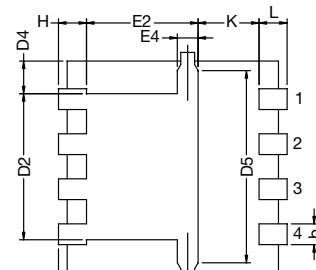
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PowerPAK® 1212-8, (Single / Dual)

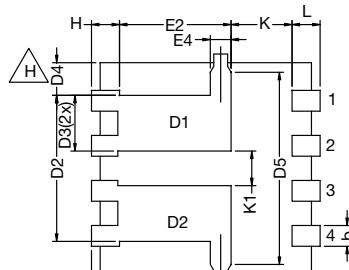


Notes

1. Inch will govern
2. Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs



Backside view of single pad

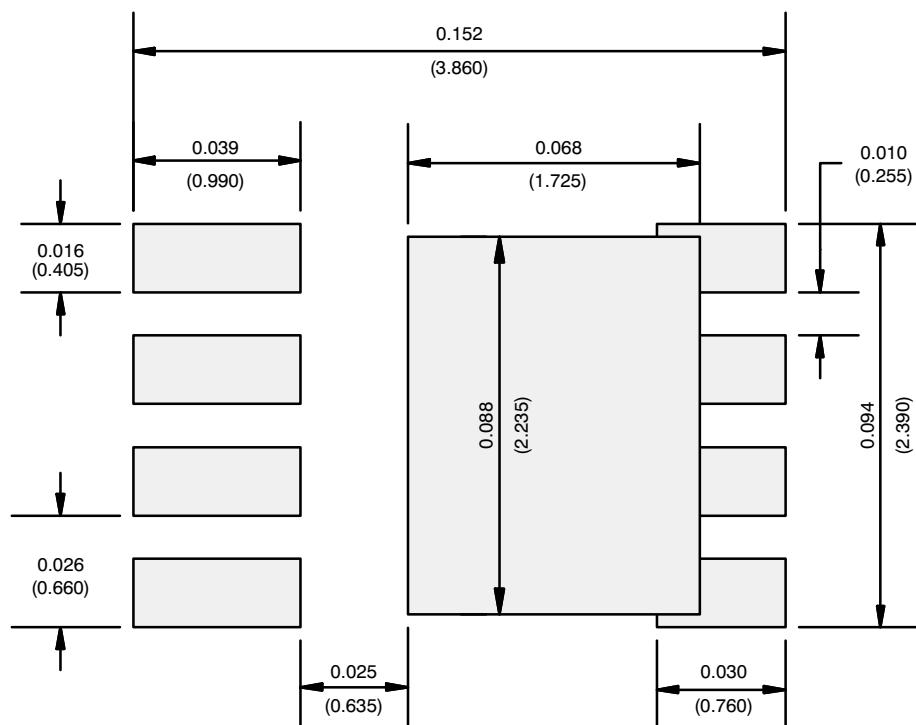


Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17

DWG: 5882

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single

Recommended Minimum Pads
Dimensions in Inches/(mm)

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