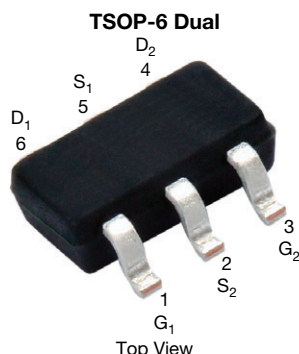


N- and P-Channel 30 V (D-S) MOSFET



FEATURES

- TrenchFET® power MOSFET
- Ultra low $R_{DS(on)}$ n- and p-channel for high efficiency
- Optimized for high side / low side
- Minimized conduction losses
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

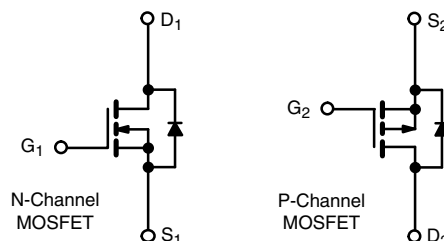


RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Portable devices including PDAs, cellular phones, and pagers

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	30	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.077	0.170
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 2.5$ V	0.120	0.300
Q_g typ. (nC)	3	3.8
I_D (A)	3	-2
Configuration	N- and p-pair	



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3590DV-T1-E3
Lead (Pb)-free and halogen-free	Si3590DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			10 s	STEADY STATE	10 s	STEADY STATE	
Drain-source voltage		V _{DS}	30		-30		V
Gate-source voltage		V _{GS}	± 12		± 12		
Continuous drain current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	3	2.5	-2	-1.7	A
	T _A = 70 °C		2.3	2	-1.6	-1.3	
Pulsed drain current		I _{DM}	8		-8		
Continuous source current (diode conduction) ^a		I _S	1.05	0.75	-1.05	-0.75	
maximum power dissipation ^a	T _A = 25 °C	P _D	1.15	0.83	1.15	0.83	W
	T _A = 70 °C		0.70	0.53	0.70	0.53	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150				°C

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	N-CHANNEL		P-CHANNEL		UNIT	
		TYP.	MAX.	TYP.	MAX.		
Maximum junction-to-ambient ^a	R_{thJA}	93	110	93	110	$^\circ\text{C/W}$	
		130	150	130	150		
Maximum junction-to-foot (drain)	R_{thJF}	75	90	75	90		

Note

a. Surface mounted on 1" x 1" FR4 board



SPECIFICATIONS (T _J = 25°C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6	-	1.5	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6	-	-1.5	
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch	-	-	± 100	nA
			P-Ch	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch	-	-	1	μA
		V _{DS} = -30 V, V _{GS} = 0 V	P-Ch	-	-	-1	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	5	
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-5	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	5	-	-	A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-5	-	-	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 3 A	N-Ch	-	0.062	0.077	Ω
		V _{GS} = -4.5 V, I _D = -2 A	P-Ch	-	0.135	0.170	
		V _{GS} = 2.5 V, I _D = 2 A	N-Ch	-	0.095	0.120	
		V _{GS} = -2.5 V, I _D = -1.2 A	P-Ch	-	0.235	0.300	
Forward transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 3 A	N-Ch	-	10	-	S
		V _{DS} = -5 V, I _D = -2 A	P-Ch	-	5	-	
Diode forward voltage ^a	V _{SD}	I _S = 1.05 A, V _{GS} = 0 V	N-Ch	-	0.8	1.1	V
		I _S = -1.05 A, V _{GS} = 0 V	P-Ch	-	-0.83	-1.1	
Dynamic ^b							
Total gate charge	Q _g	N-Channel V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 2 A P-Channel V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -2 A	N-Ch	-	3	4.5	nC
Gate-source charge	Q _{gs}		P-Ch	-	3.8	6	
			N-Ch	-	0.6	-	
Gate-drain charge	Q _{gd}		P-Ch	-	0.6	-	
		N-Ch	-	1	-		
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω P-Channel V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 6 Ω	P-Ch	-	1.5	-	ns
			N-Ch	-	5	8	
P-Ch	-		5	8			
N-Ch	-		12	23			
P-Ch	-		15	23			
Turn-off delay time	t _{d(off)}		N-Ch	-	13	23	
			P-Ch	-	20	30	
Fall time	t _f		N-Ch	-	7	12	
		P-Ch	-	20	30		
Source-drain reverse recovery time	t _{rr}	I _F = 1.05 A, di/dt = 100 A/μs	N-Ch	-	15	25	
		I _F = -1.05 A, di/dt = 100 A/μs	P-Ch	-	18	30	

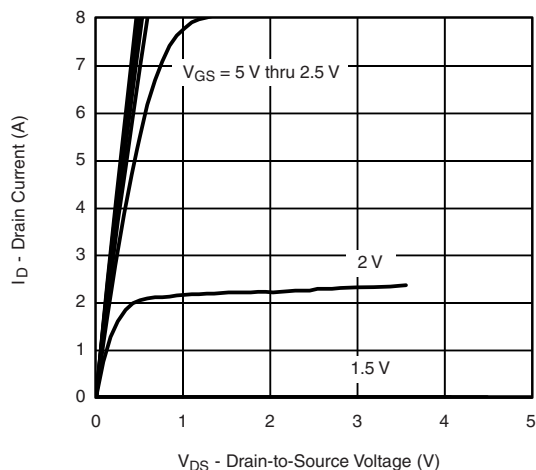
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$
b. Guaranteed by design, not subject to production testing

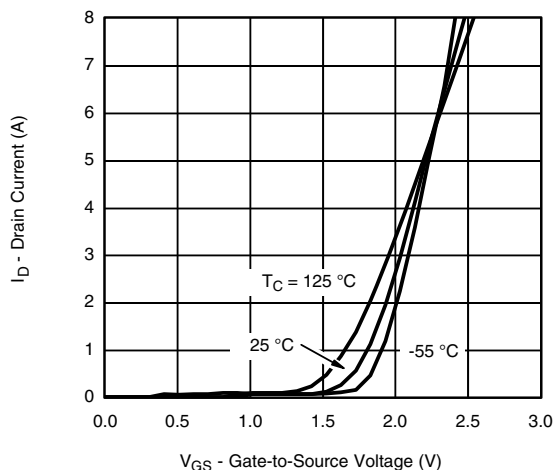
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



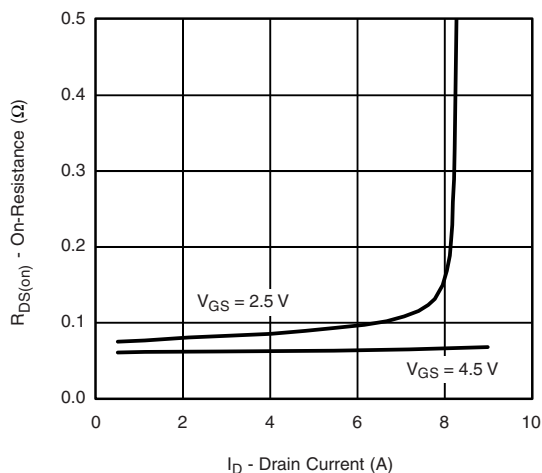
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



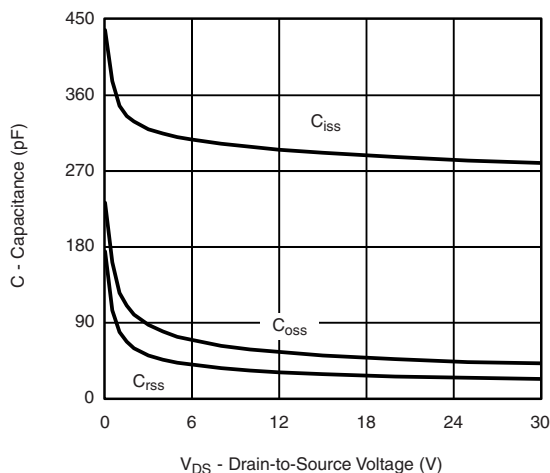
Output Characteristics



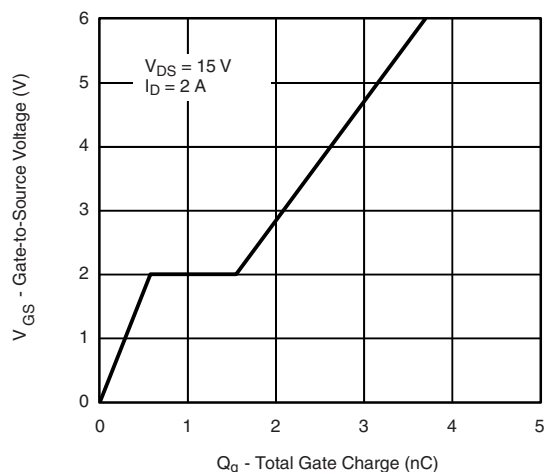
Transfer Characteristics



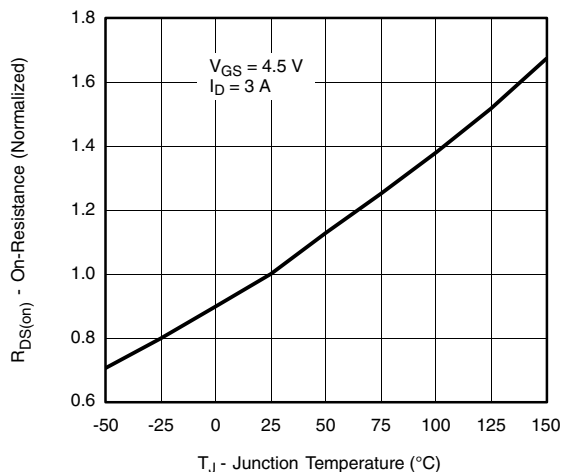
On-Resistance vs. Drain Current



Capacitance



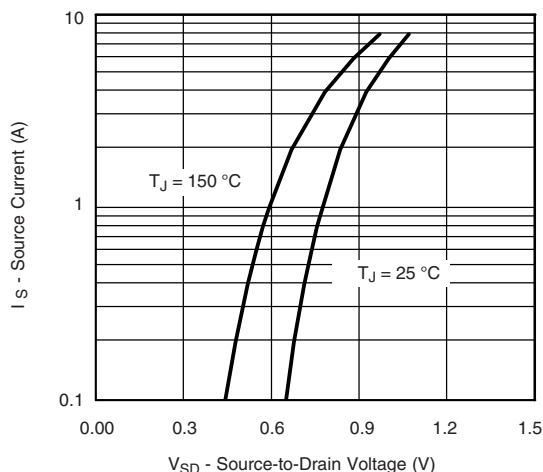
Gate Charge



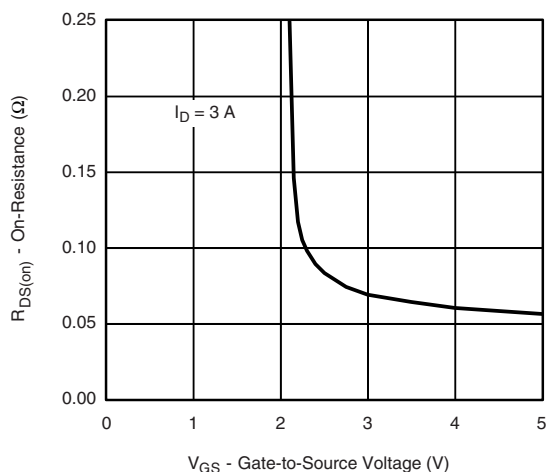
On-Resistance vs. Junction Temperature



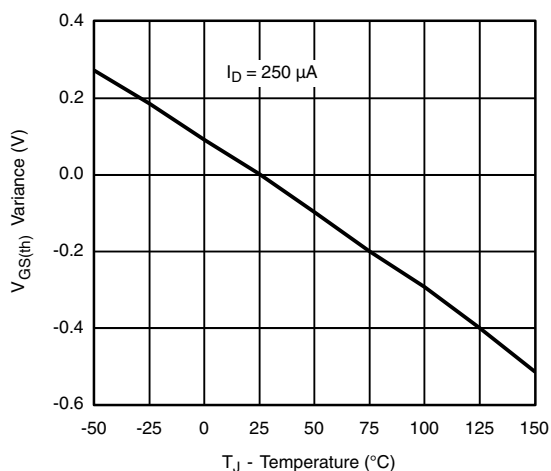
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



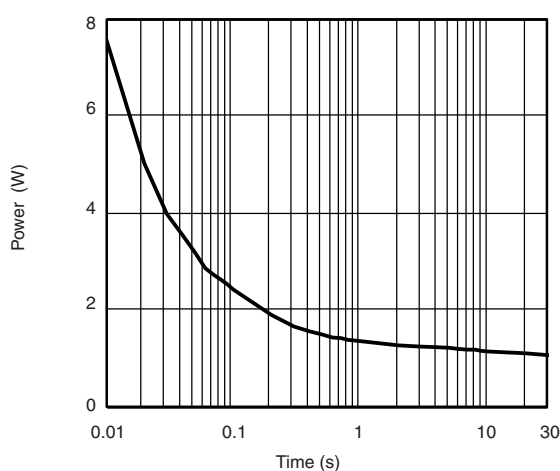
Source-Drain Diode Forward Voltage



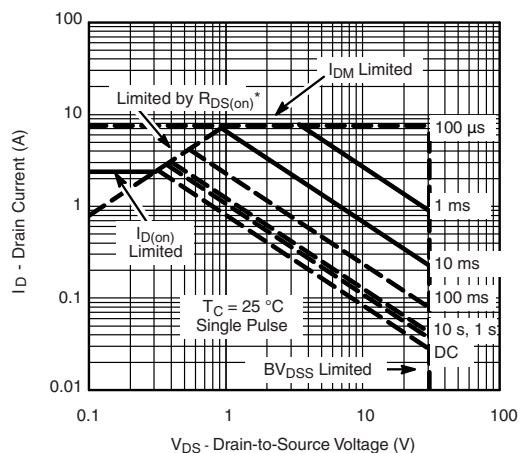
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

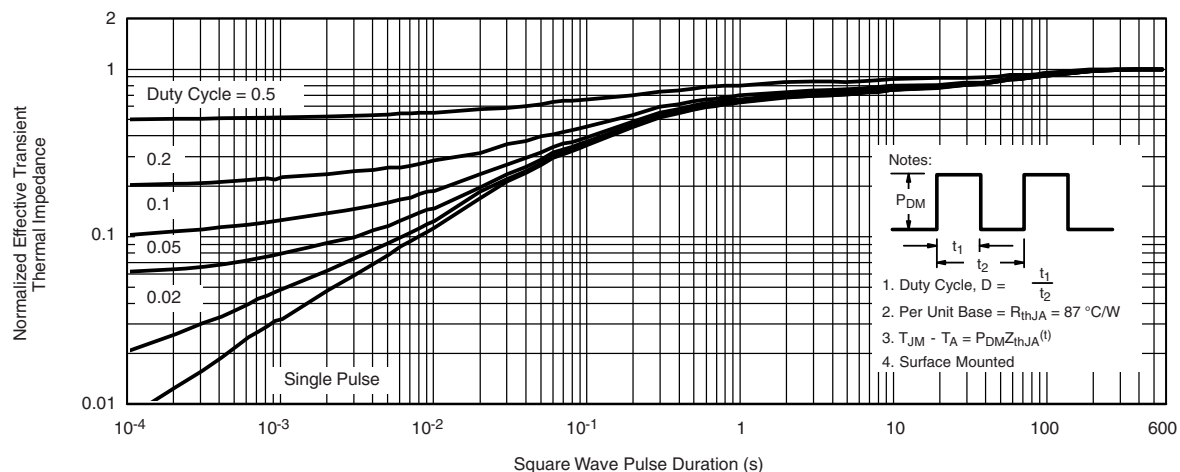


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

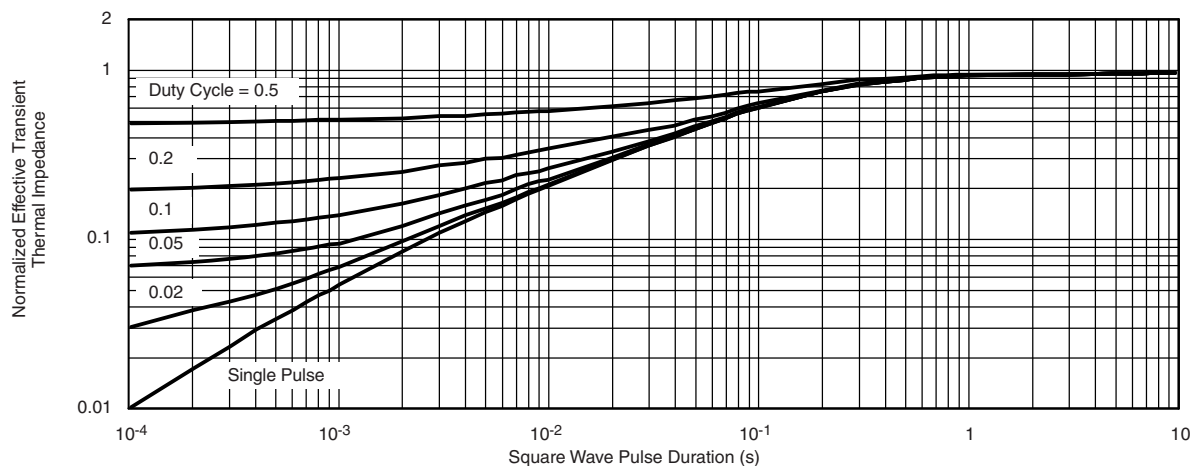
Safe Operating Area, Junction-to-Case



N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



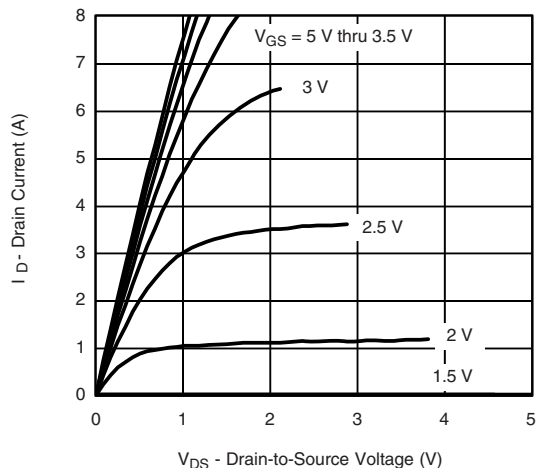
Normalized Thermal Transient Impedance, Junction-to-Ambient



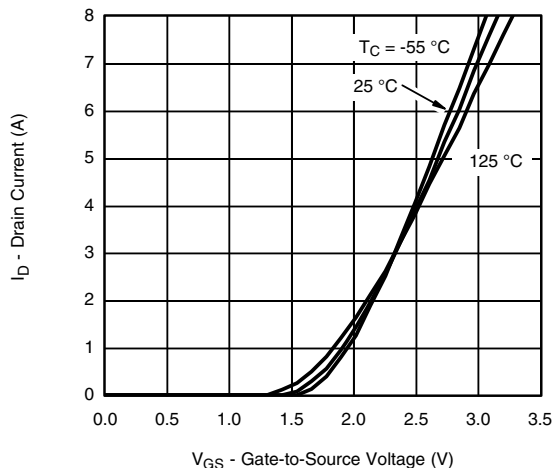
Normalized Thermal Transient Impedance, Junction-to-Foot



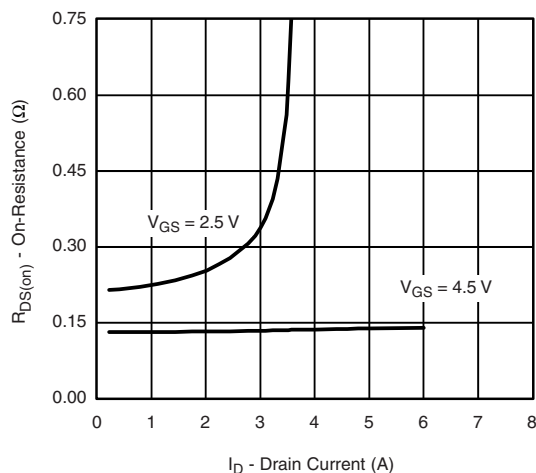
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



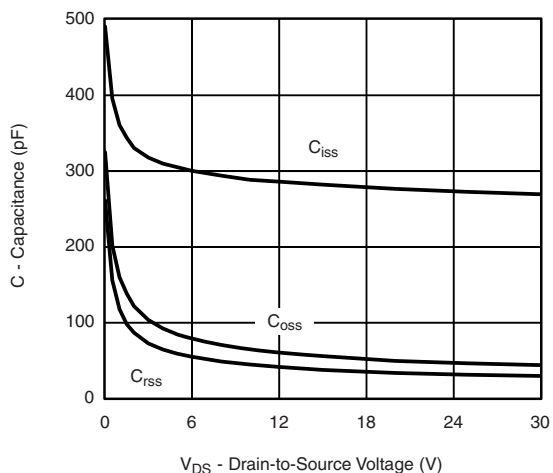
Output Characteristics



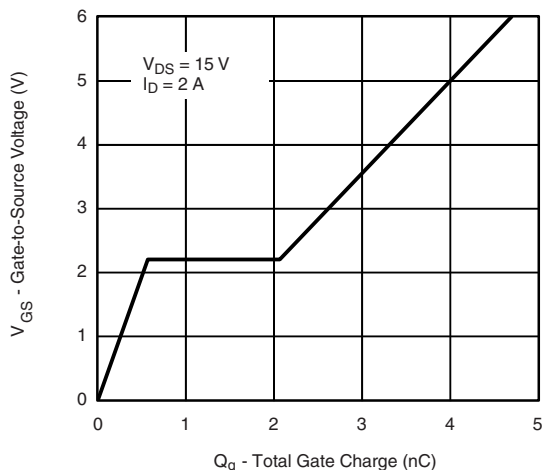
Transfer Characteristics



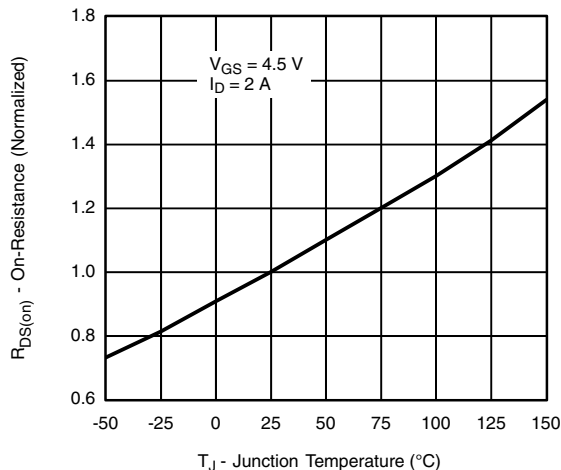
On-Resistance vs. Drain Current



Capacitance



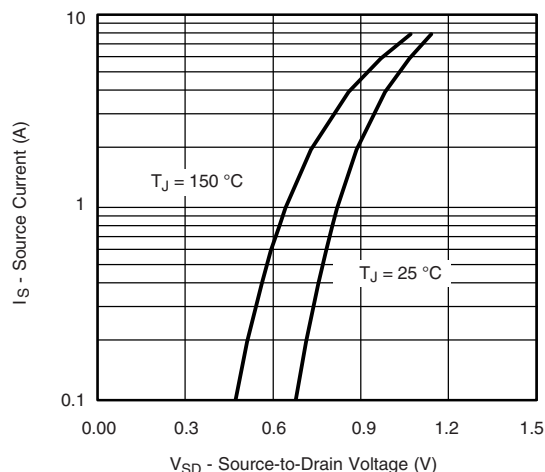
Gate Charge



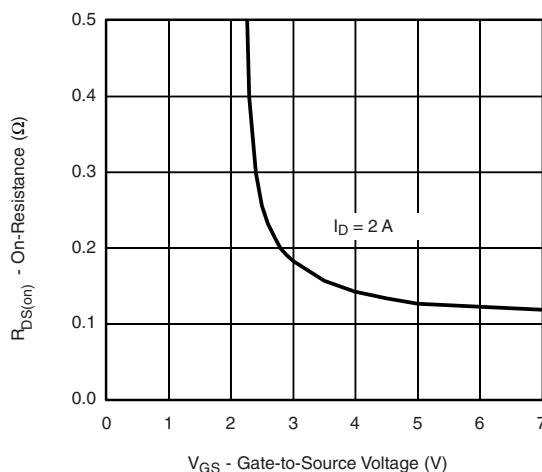
On-Resistance vs. Junction Temperature



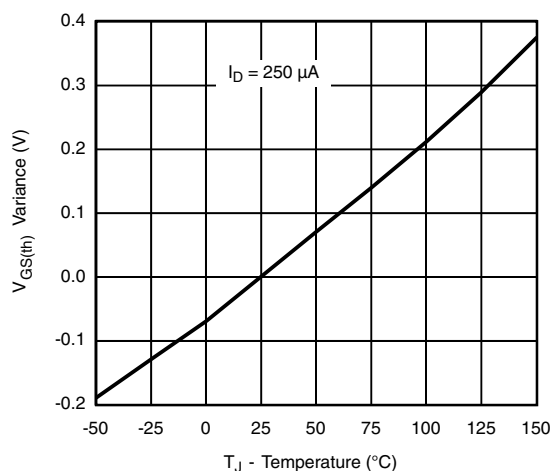
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



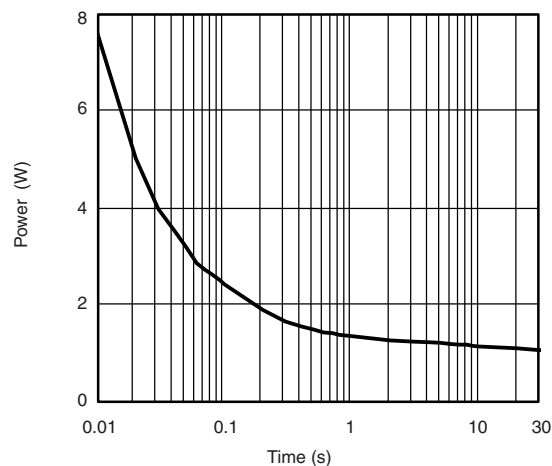
Source-Drain Diode Forward Voltage



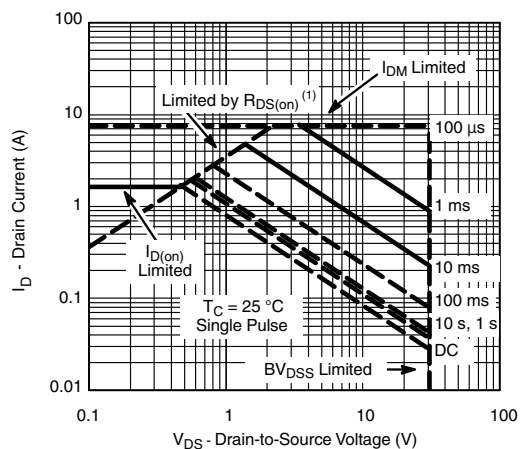
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

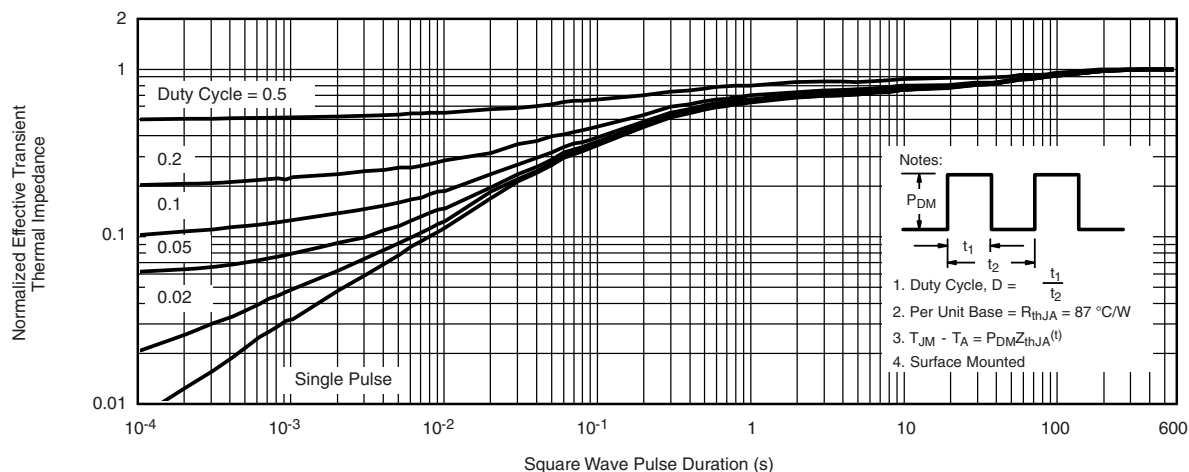


(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

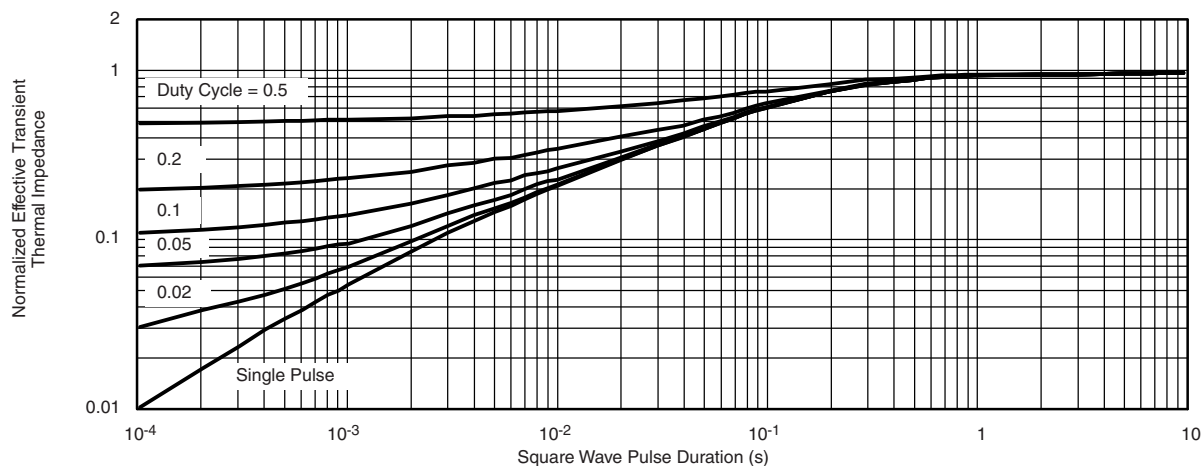
Safe Operating Area, Junction-to-Case



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

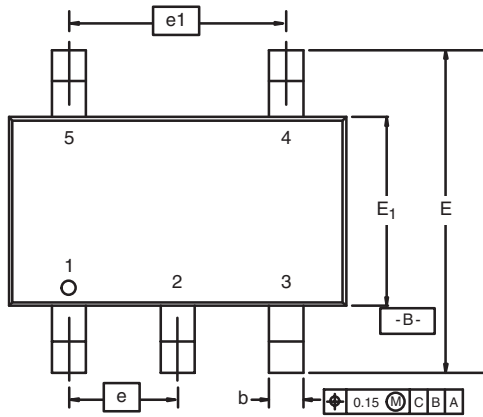


Normalized Thermal Transient Impedance, Junction-to-Foot

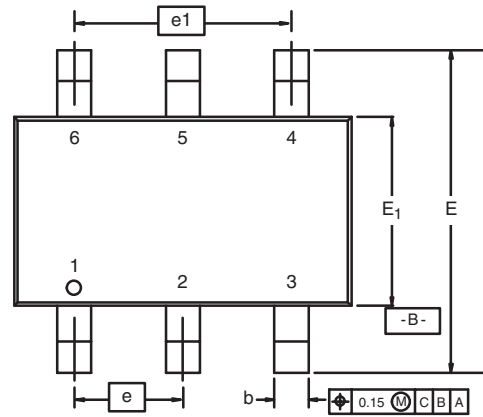
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72032.

TSOP: 5/6-LEAD

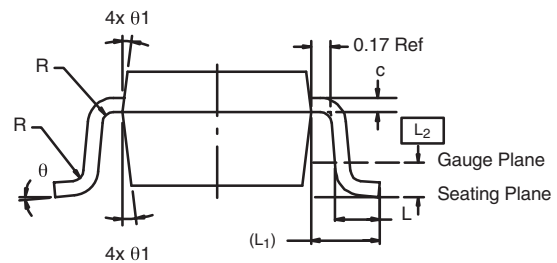
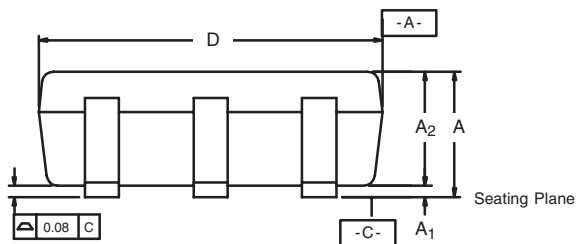
JEDEC Part Number: MO-193C



5-LEAD TSOP

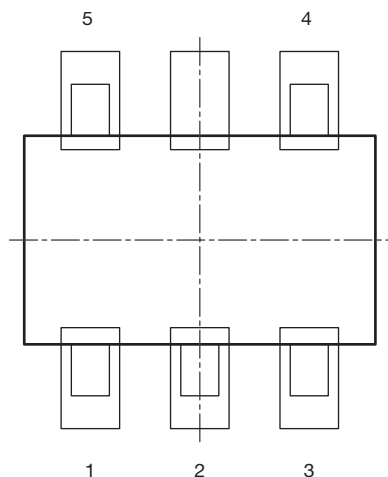


6-LEAD TSOP

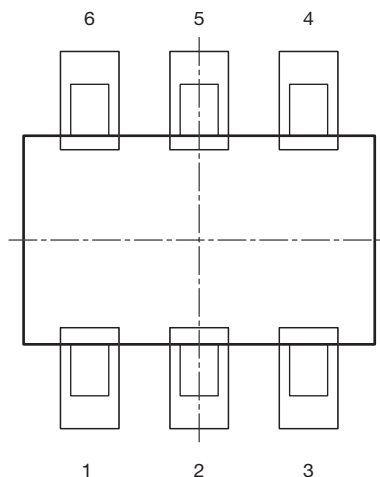


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

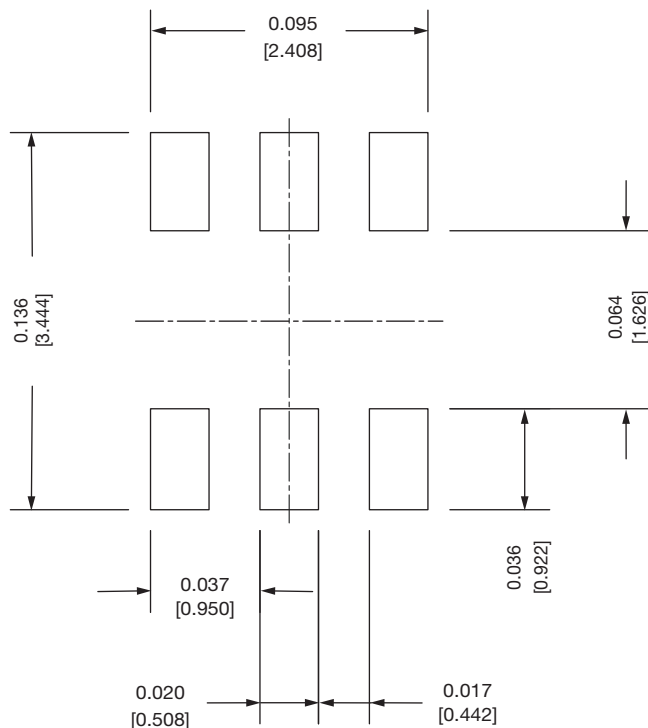
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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