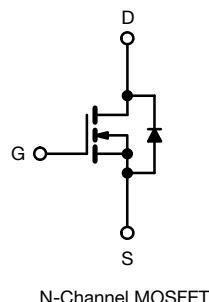
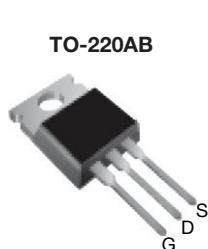


Power MOSFET



PRODUCT SUMMARY

V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0$ V	0.18
Q_g max. (nC)	66	
Q_{gs} (nC)	9.0	
Q_{gd} (nC)	38	
Configuration	Single	

FEATURES

- Dynamic dv/dt rating
- Repetitive avalanche rated
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4$ V and 5 V
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRL640PbF
Lead (Pb)-free and halogen-free	IRL640PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	200	V
Gate-source voltage		± 10	
Continuous drain current	I_D	17	A
		11	
Pulsed drain current ^a	I_{DM}	68	
Linear derating factor		1.0	W/°C
Single pulse avalanche energy ^b	E_{AS}	580	mJ
Repetitive avalanche current ^a	I_{AR}	10	A
Repetitive avalanche energy ^a	E_{AR}	13	mJ
Maximum power dissipation	P_D	125	W
Peak diode recovery dv/dt ^c	dv/dt	5.0	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 3.0$ mH, $R_g = 25$ Ω $I_{AS} = 17$ A (see fig. 12)
- $I_{SD} \leq 17$ A, $dI/dt \leq 150$ A/ms, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C

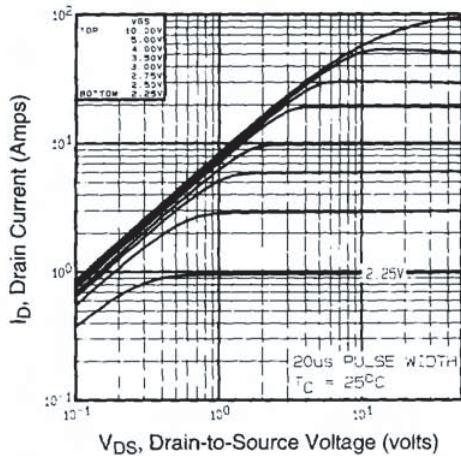
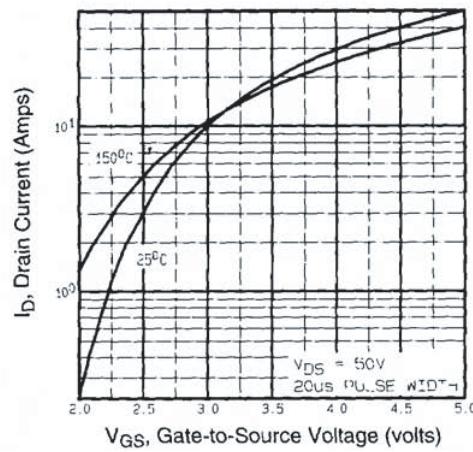
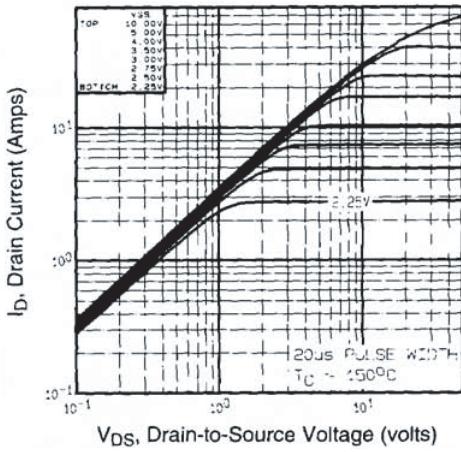
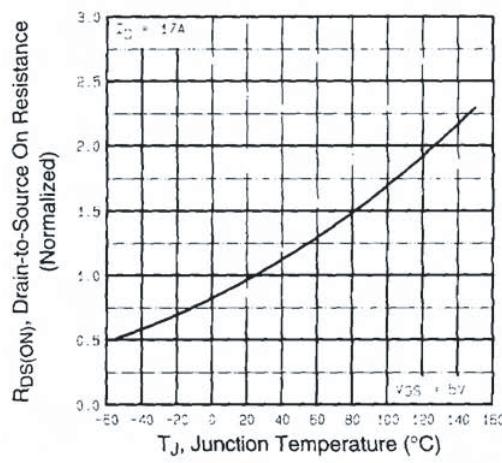
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Static									
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		200	-	-	V		
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1\text{ mA}$		-	0.27	-	$^{\circ}\text{C}/\text{C}$		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V		
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 10$		-	-	± 100	nA		
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA		
		$V_{DS} = 160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	250			
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 10\text{ A}^b$	-	-	0.18	Ω		
		$V_{GS} = 4.0\text{ V}$	$I_D = 8.5\text{ A}^b$	-	-	0.27			
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 10\text{ A}^b$		16	-	-	S		
Dynamic									
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5		-	1800	-	pF		
Output capacitance	C_{oss}			-	400	-			
Reverse transfer capacitance	C_{rss}			-	120	-			
Total gate charge	Q_g	$V_{GS} = 5.0\text{ V}$	$I_D = 17\text{ A}$, $V_{DS} = 160\text{ V}$, see fig. 6 and 13 ^b	-	-	66	nC		
Gate-source charge	Q_{gs}			-	-	9.0			
Gate-drain charge	Q_{gd}			-	-	38			
Turn-on delay time	$t_{d(on)}$			-	8.0	-			
Rise time	t_r	$V_{DD} = 100\text{ V}$, $I_D = 17\text{ A}$ $R_g = 4.6\text{ }\Omega$, $R_D = 5.7\text{ }\Omega$, see fig. 10 ^b		-	83	-	ns		
Turn-off delay time	$t_{d(off)}$			-	44	-			
Fall time	t_f			-	52	-			
Internal drain inductance	L_D			-	4.5	-	nH		
Internal source inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5	-			
Gate input resistance	R_g			$f = 1\text{ MHz}$, open drain	0.3	-	1.2	Ω	
Drain-Source Body Diode Characteristics									
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	17	A		
Pulsed diode forward current ^a	I_{SM}			-	-	68			
Body diode voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 17\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	2.0	V		
Body diode reverse recovery time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = 17\text{ A}$, $dl/dt = 100\text{ A}/\mu\text{s}^b$		-	310	470	ns		
Body diode reverse recovery charge	Q_{rr}			-	3.2	4.8	μC		
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)							

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_c = 25 \text{ } ^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_c = 150 \text{ } ^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

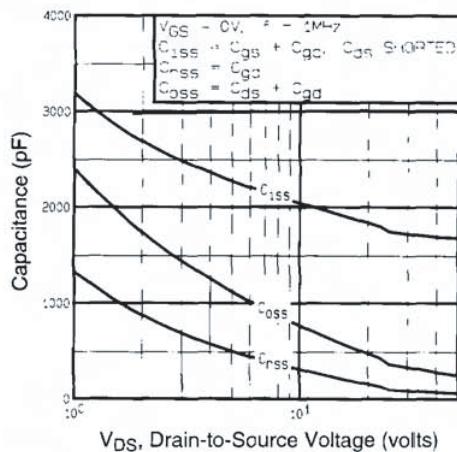


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

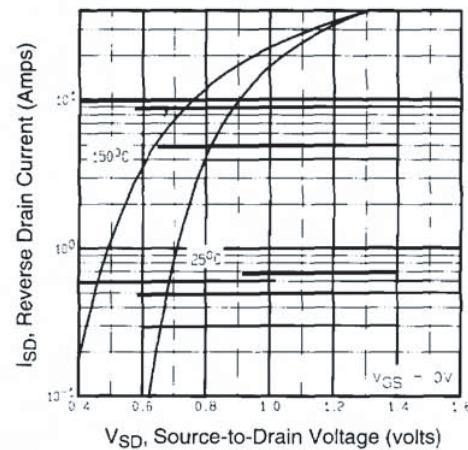


Fig. 7 - Typical Source-Drain Diode Forward Voltage

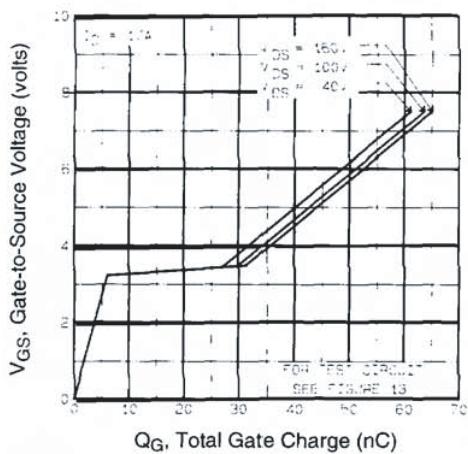


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

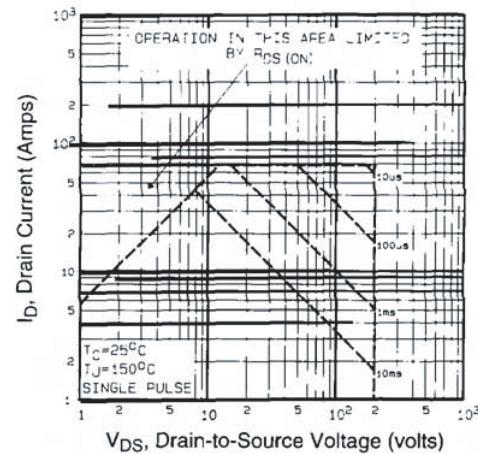


Fig. 8 - Maximum Safe Operating Area

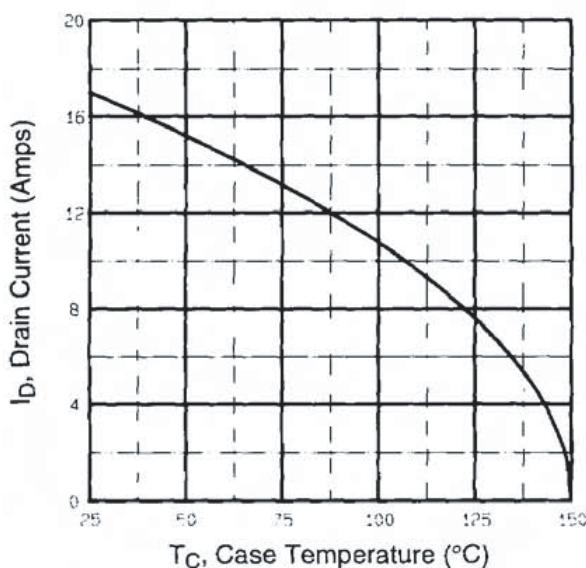


Fig. 9 - Maximum Drain Current vs. Case Temperature

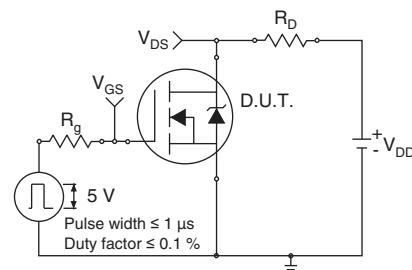


Fig. 10a - Switching Time Test Circuit

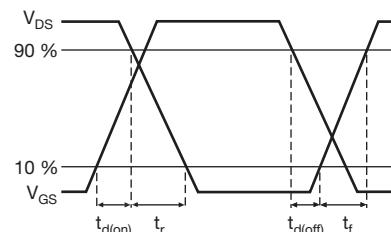


Fig. 10b - Switching Time Waveforms

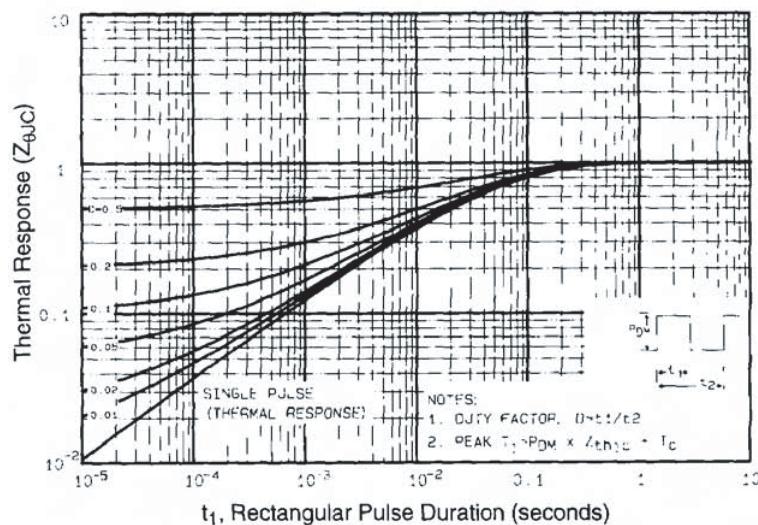


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

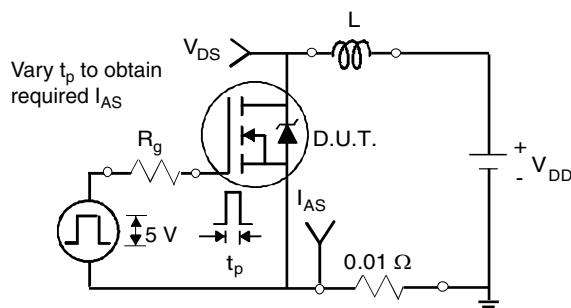


Fig. 12a - Unclamped Inductive Test Circuit

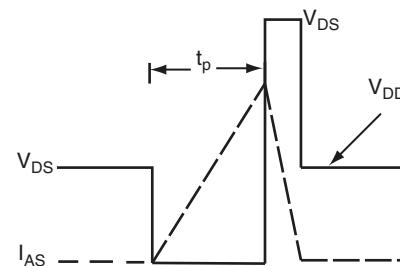


Fig. 12b - Unclamped Inductive Waveforms

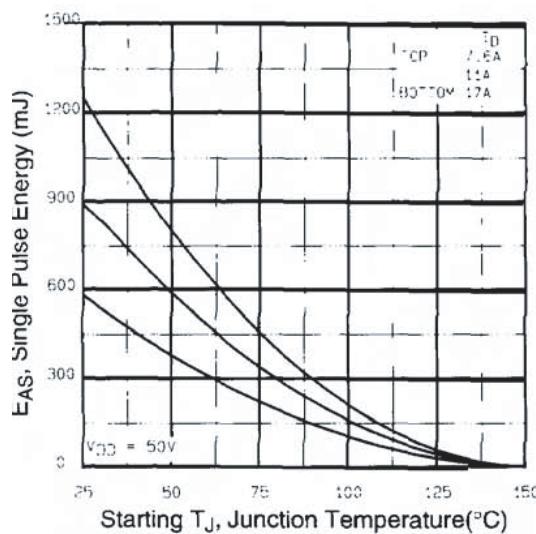


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

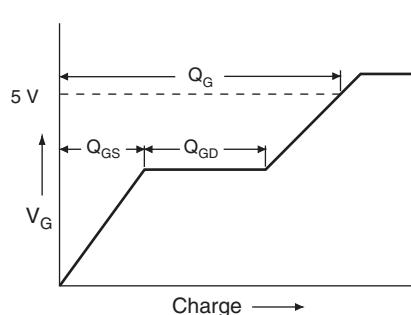


Fig. 13a - Basic Gate Charge Waveform

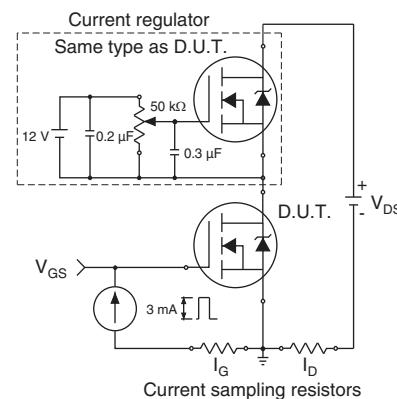


Fig. 13b - Gate Charge Test Circuit

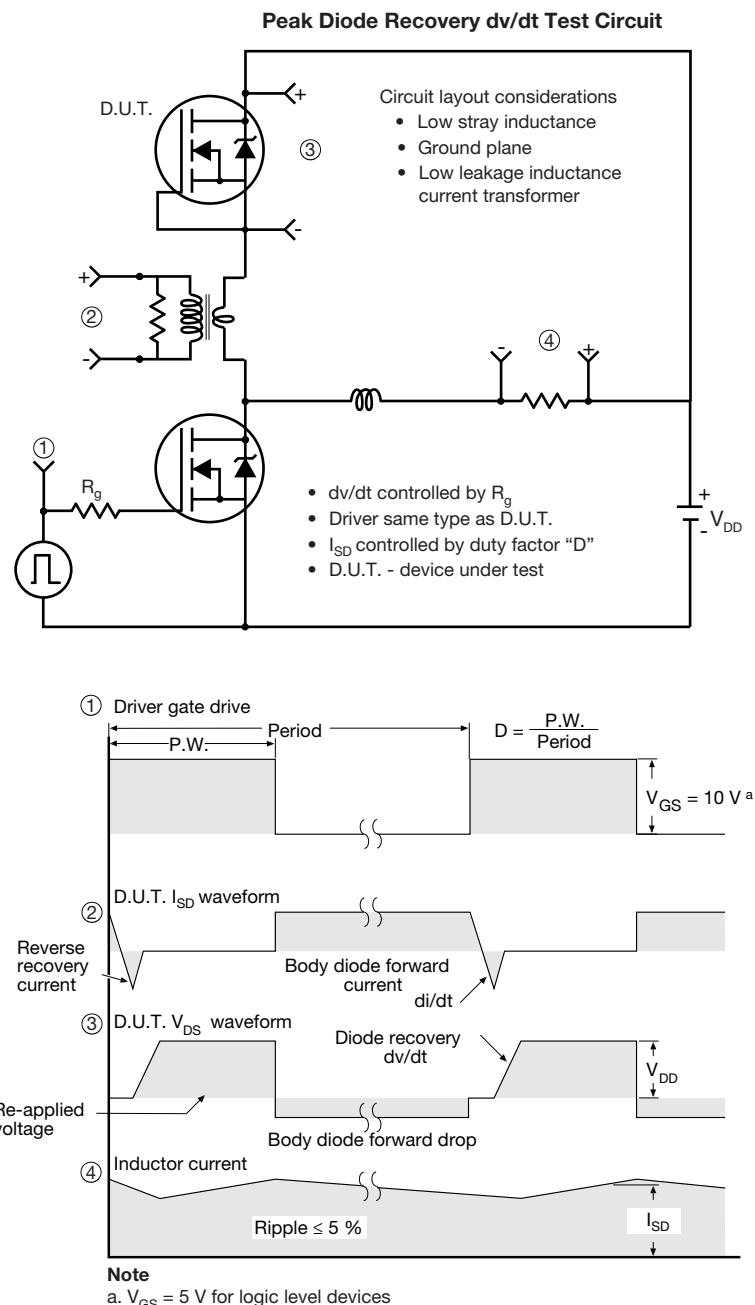


Fig. 14 - For N-Channel

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