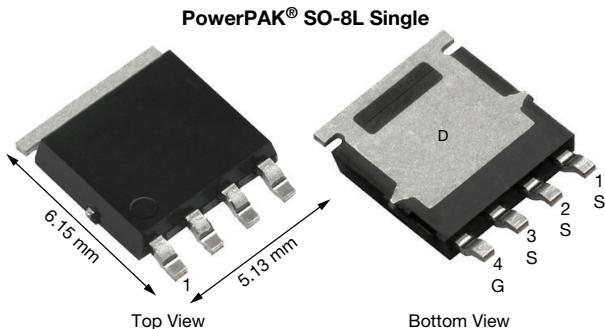


N-Channel 60 V (D-S) MOSFET

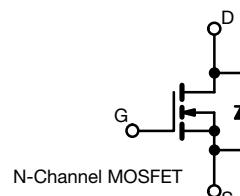


FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency
- Flexible leads provide resilience to mechanical stress
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY

| | |
|--|--------|
| V_{DS} (V) | 60 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V | 0.0072 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V | 0.0110 |
| Q_g typ. (nC) | 15 |
| I_D (A) ^a | 39.3 |
| Configuration | Single |

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters
- Boost converters
- Motor drive control

ORDERING INFORMATION

| | |
|---------------------------------|------------------|
| Package | PowerPAK SO-8L |
| Lead (Pb)-free and halogen-free | SiJ462ADP-T1-GE3 |

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

| PARAMETER | SYMBOL | LIMIT | UNIT |
|--|----------------|-------------|------|
| Drain-source voltage | V_{DS} | 60 | V |
| Gate-source voltage | V_{GS} | ± 20 | |
| Continuous drain current ($T_J = 150$ °C) | I_D | 39.3 | A |
| | | 31.4 | |
| | | 15.8 b, c | |
| | | 12.6 b, c | |
| Pulsed drain current ($t = 100$ μ s) | I_{DM} | 100 | |
| Continuous source-drain diode current | I_S | 20.2 | |
| | | 3.2 b, c | |
| Single pulse avalanche current | I_{AS} | 15 | mJ |
| Single pulse avalanche energy | E_{AS} | 11.25 | |
| Maximum power dissipation | P_D | 22.3 | W |
| | | 14.2 | |
| | | 3.6 b, c | |
| | | 2.3 b, c | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C |
| Soldering recommendations (peak temperature) ^{d, e} | | 260 | |

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYPICAL | MAXIMUM | UNIT |
|----------------------------------|------------|---------|---------|------|
| Maximum junction-to-ambient b, f | R_{thJA} | 27 | 34 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | 4.5 | 5.6 | |

Notes

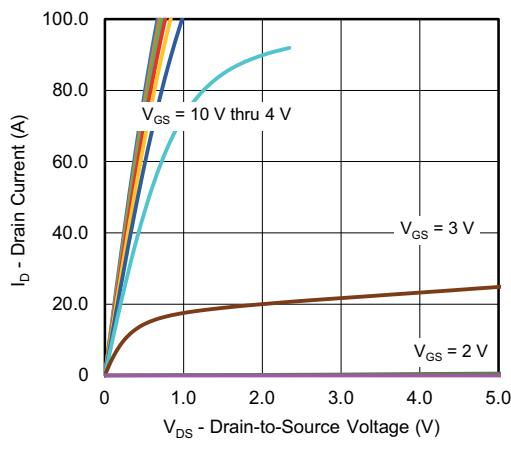
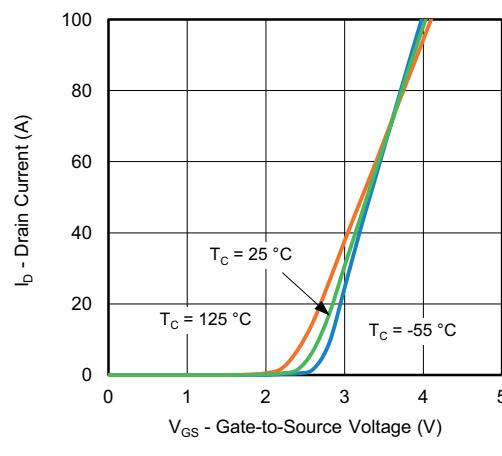
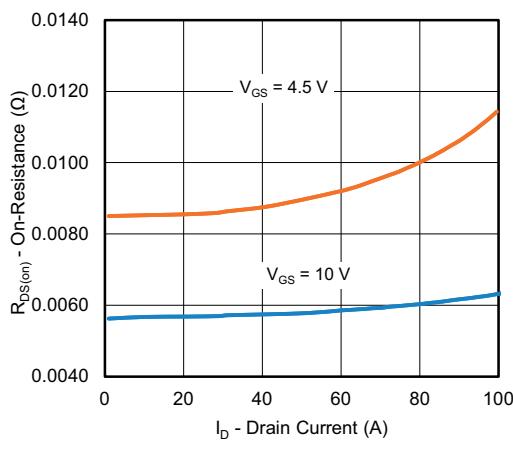
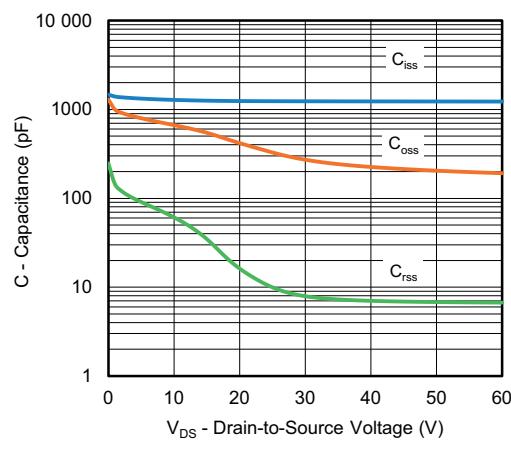
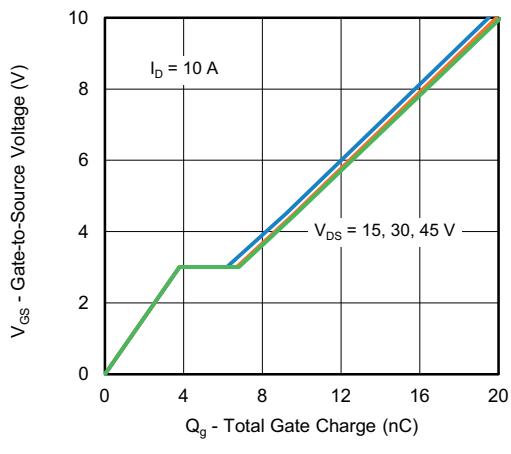
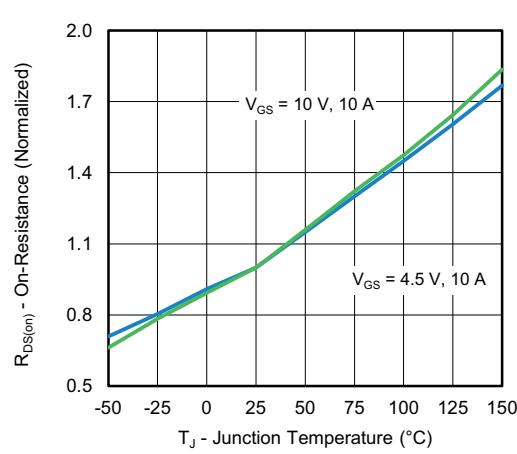
- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W

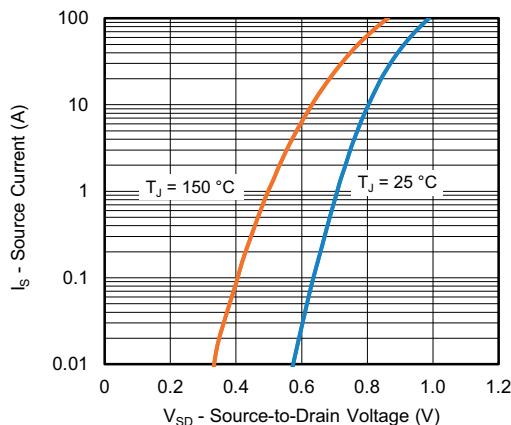
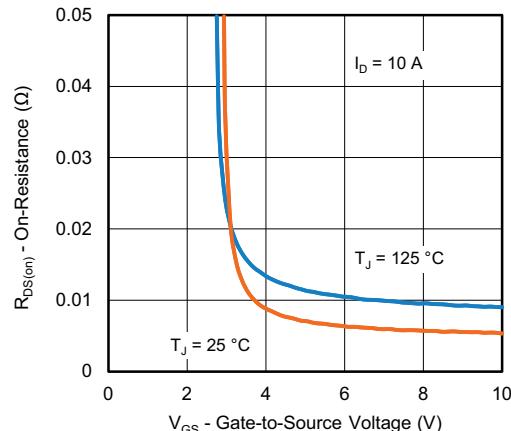
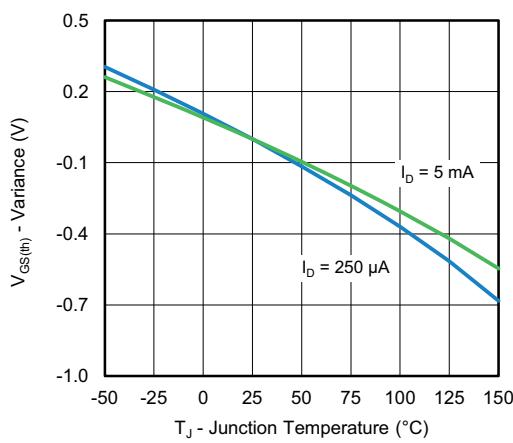
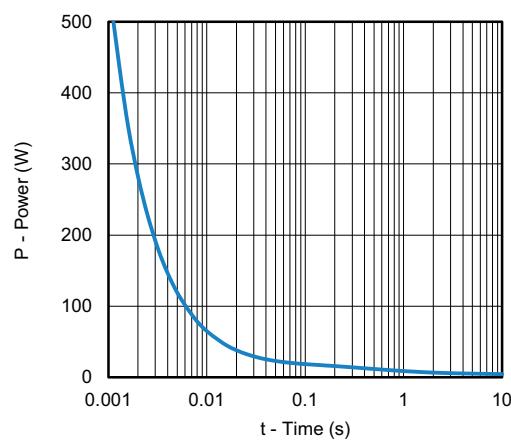
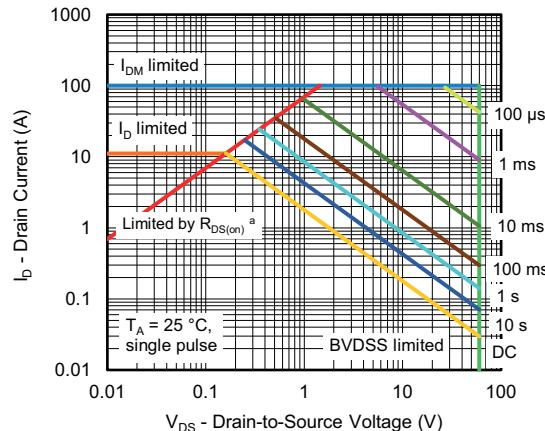
| SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted) | | | | | | |
|--|--------------------------------|--|------|--------|-----------|----------------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$ | 60 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | $I_D = 1 \text{ mA}$ | - | 33 | - | mV/ $^\circ\text{C}$ |
| $V_{GS(\text{th})}$ temperature coefficient | $\Delta V_{GS(\text{th})}/T_J$ | $I_D = 250 \mu\text{A}$ | - | -4.7 | - | |
| Gate-source threshold voltage | $V_{GS(\text{th})}$ | $V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$ | 1 | - | 2.5 | V |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$ | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$ | - | - | 1 | μA |
| | | $V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 75^\circ\text{C}$ | - | - | 20 | |
| On-state drain current ^a | $I_{D(\text{on})}$ | $V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$ | 30 | - | - | A |
| Drain-source on-state resistance ^a | $R_{DS(\text{on})}$ | $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$ | - | 0.0057 | 0.0072 | Ω |
| | | $V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$ | - | 0.0086 | 0.0110 | |
| Forward transconductance ^a | g_{fs} | $V_{DS} = 10 \text{ V}$, $I_D = 10 \text{ A}$ | - | 49 | - | S |
| Dynamic^b | | | | | | |
| Input capacitance | C_{iss} | $V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$ | - | 1235 | - | pF |
| Output capacitance | C_{oss} | | - | 282 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 10 | - | |
| Total gate charge | Q_g | $V_{DS} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$ | - | 19.8 | 30 | nC |
| | | $V_{DS} = 30 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$ | - | 9.6 | 15 | |
| Gate-source charge | Q_{gs} | | - | 3.8 | - | |
| Gate-drain charge | Q_{gd} | | - | 2.9 | - | |
| Output charge | Q_{oss} | $V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$ | - | 17.1 | - | Ω |
| Gate resistance | R_g | $f = 1 \text{ MHz}$ | 0.3 | 0.85 | 1.5 | |
| Turn-on delay time | $t_{d(\text{on})}$ | $V_{DD} = 30 \text{ V}$, $R_L = 3 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$ | - | 11 | 22 | ns |
| Rise time | t_r | | - | 6 | 12 | |
| Turn-off delay time | $t_{d(\text{off})}$ | | - | 20 | 40 | |
| Fall time | t_f | | - | 6 | 12 | |
| Turn-on delay time | $t_{d(\text{on})}$ | $V_{DD} = 30 \text{ V}$, $R_L = 3 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$ | - | 20 | 40 | |
| Rise time | t_r | | - | 73 | 146 | |
| Turn-off delay time | $t_{d(\text{off})}$ | | - | 21 | 42 | |
| Fall time | t_f | | - | 10 | 20 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous source-drain diode current | I_S | $T_C = 25^\circ\text{C}$ | - | - | 20.2 | A |
| Pulse diode forward current ($t_p = 100 \mu\text{s}$) | I_{SM} | | - | - | 100 | |
| Body diode voltage | V_{SD} | $I_S = 5 \text{ A}$ | - | 0.76 | 1.1 | V |
| Body diode reverse recovery time | t_{rr} | $I_F = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$ | - | 9.5 | 19 | ns |
| Body diode reverse recovery charge | Q_{rr} | | - | 21 | 42 | |
| Reverse recovery fall time | t_a | | - | 10 | - | |
| Reverse recovery rise time | t_b | | - | 11 | - | |

Notes

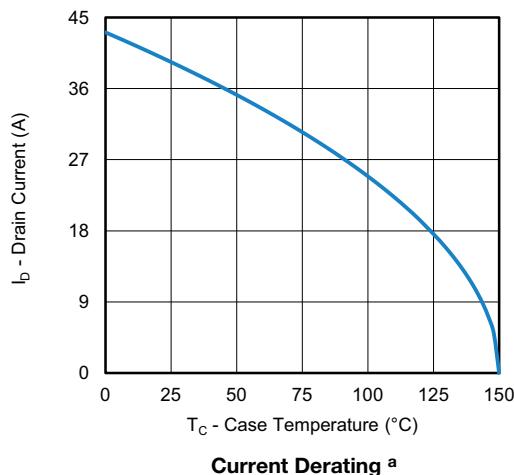
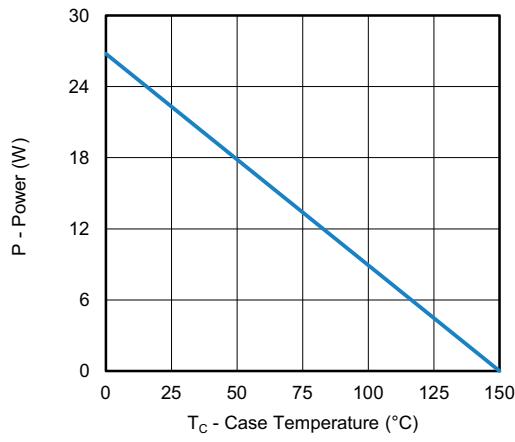
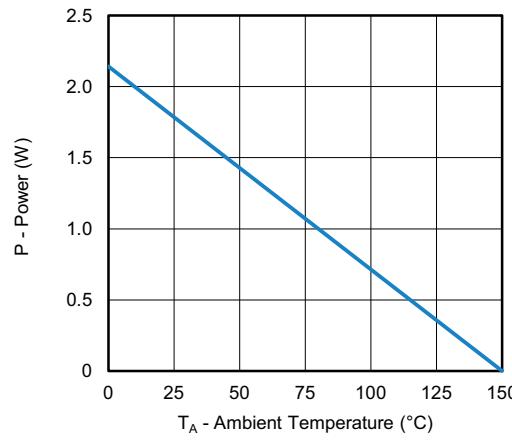
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

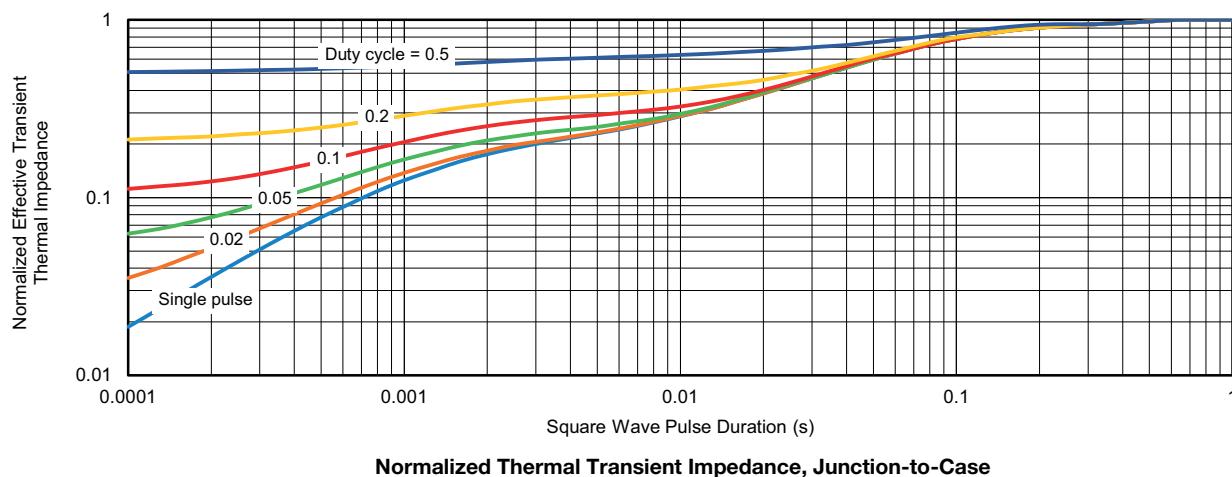
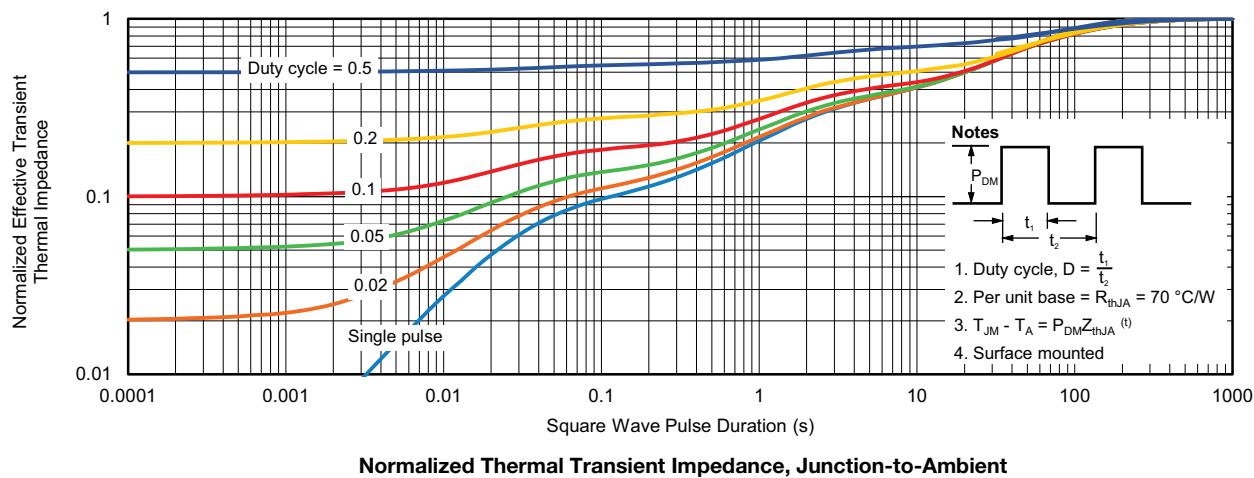
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

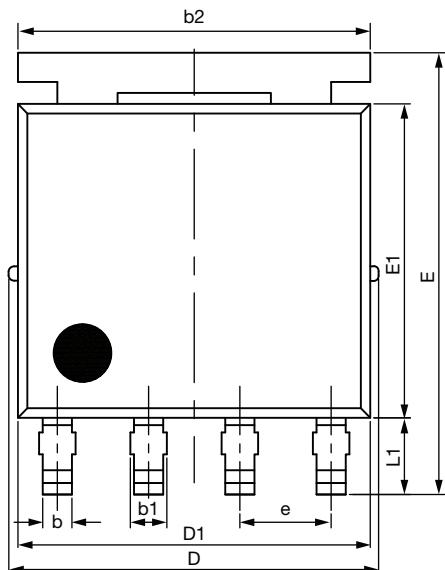
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

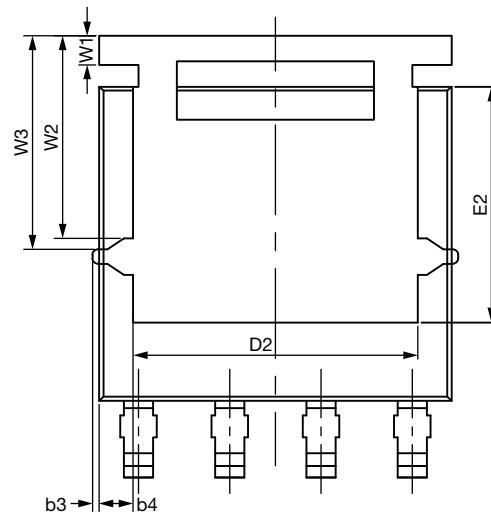
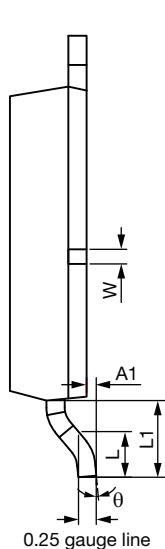
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77286.

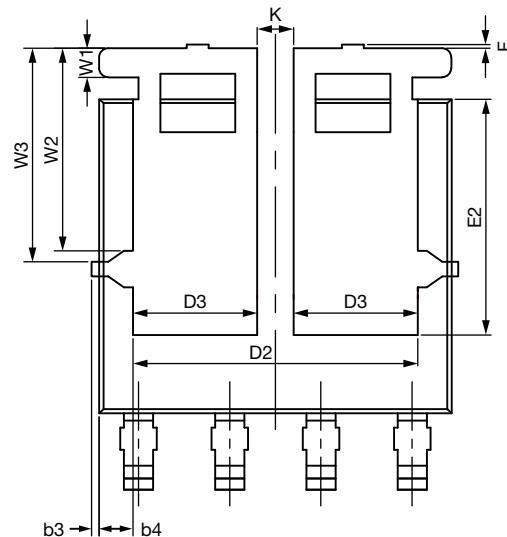
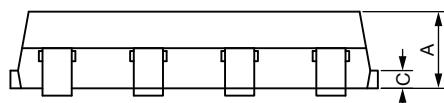
PowerPAK® SO-8L Case Outline 1



Topside view



Backside view (single)



Backside view (dual)



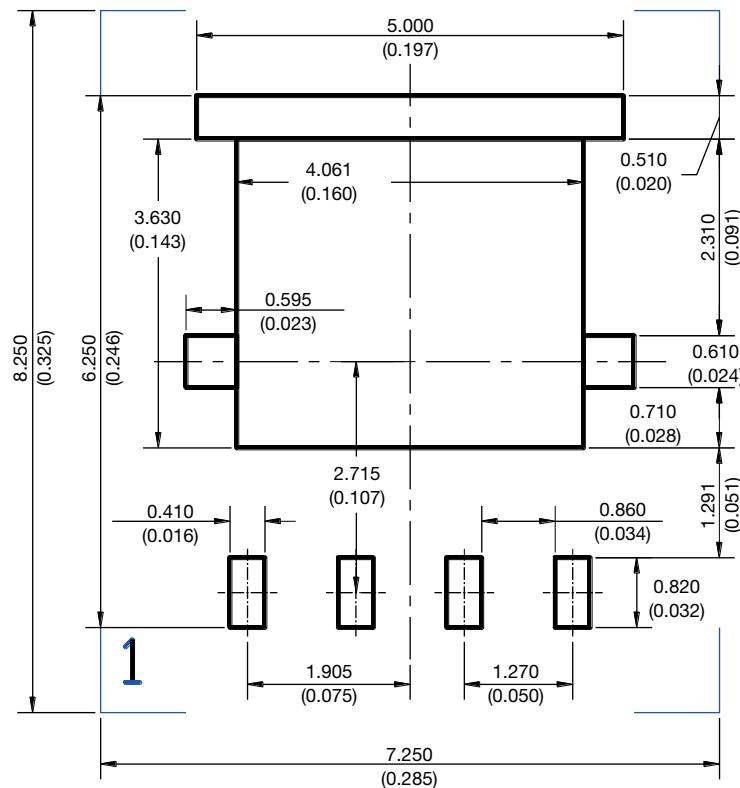
| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|------|-------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | 1.07 | 1.14 | 0.039 | 0.042 | 0.045 |
| A1 | 0.00 | - | 0.127 | 0.00 | - | 0.005 |
| b | 0.33 | 0.41 | 0.48 | 0.013 | 0.016 | 0.019 |
| b1 | 0.44 | 0.51 | 0.58 | 0.017 | 0.020 | 0.023 |
| b2 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| b3 | 0.094 | | | 0.004 | | |
| b4 | 0.47 | | | 0.019 | | |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 5.00 | 5.13 | 5.25 | 0.197 | 0.202 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.86 | 3.96 | 4.06 | 0.152 | 0.156 | 0.160 |
| D3 | 1.63 | 1.73 | 1.83 | 0.064 | 0.068 | 0.072 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 4.27 | 4.37 | 4.47 | 0.168 | 0.172 | 0.176 |
| E2 | 3.18 | 3.28 | 3.38 | 0.125 | 0.129 | 0.133 |
| F | - | - | 0.15 | - | - | 0.006 |
| L | 0.62 | 0.72 | 0.82 | 0.024 | 0.028 | 0.032 |
| L1 | 0.92 | 1.07 | 1.22 | 0.036 | 0.042 | 0.048 |
| K | 0.51 | | | 0.020 | | |
| W | 0.23 | | | 0.009 | | |
| W1 | 0.41 | | | 0.016 | | |
| W2 | 2.82 | | | 0.111 | | |
| W3 | 2.96 | | | 0.117 | | |
| θ | 0° | - | 10° | 0° | - | 10° |

ECN: S19-0643-Rev. E, 05-Aug-2019

DWG: 5976

Note

- Millimeters will govern

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE


Recommended Minimum Pads
Dimensions in mm (inches)

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