1.5A, Low Input Voltage, Ultra-Low Dropout Linear Regulator with Enable

General Description

The RT9048A is a high performance positive voltage regulator designed for applications requiring ultra-low input voltage and ultra-low dropout voltage at up to 1.5A. The feature of ultra-low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 1.6V and the output voltage is adjustable by an external resistive divider as low as 0.65V. The RT9048A provides an excellent output voltage regulation over variations in line, load and temperature. Over-current and over-temperature protection functions are provided. Additionally, an enable pin is designed to further reduce power consumption while shutdown and the shutdown current is as low as 0.1μA.

The RT9048A is available in the WDFN-8L 3x3 package.

Ordering Information

RT9048A□□

Package Type
QW : WDFN-8L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

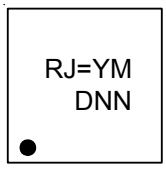
Features

- **Input Voltage as Low as 1.6V**
- **Ultra-Low Dropout Voltage 300mV @ 1.5A**
- **Over-Current Protection**
- **Over-Temperature Protection**
- **0.1μA Input Current in Shutdown Mode**
- **Enable Control**
- **RoHS Compliant and Halogen Free**

Applications

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructure
- Set-Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

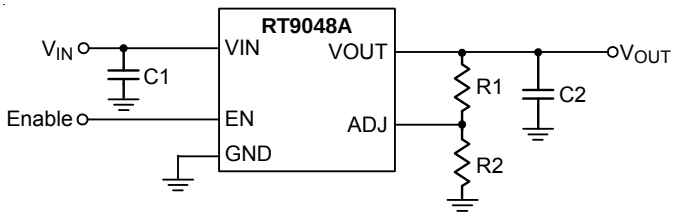
Marking Information



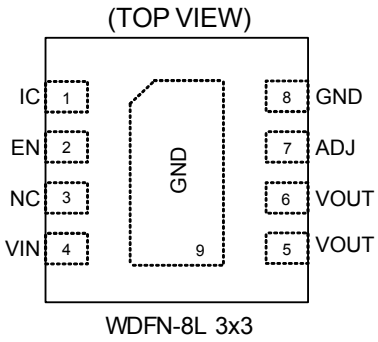
RJ = : Product Code

YMDNN : Date Code

Simplified Application Circuit



Pin Configuration

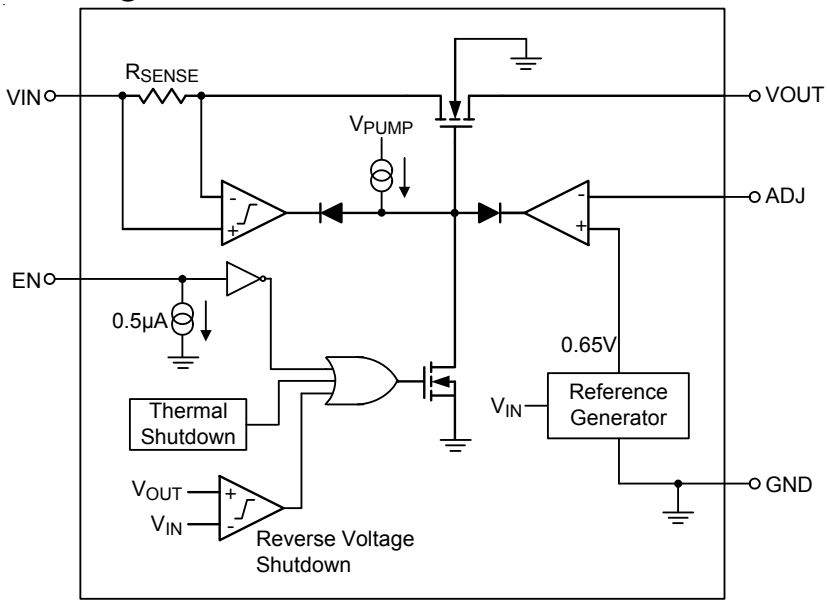


WDFN-8L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	IC	Internal connection, leave this pin floating for normal operation.
2	EN	Enable control input (initial pull low). Pulling this pin above 1.4V turns the regulator on. The device will be disabled if this pin is left open.
3	NC	No internal connection.
4	VIN	Supply voltage input. For regulation at full load, the input to this pin must be between (V_{OUT} + 0.3V) and 6V. The minimum input voltage is 1.6V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.6V. Also, a minimum of 10μF ceramic capacitor should be placed directly at this pin.
5, 6	VOUT	Output voltage. A minimum of 10μF capacitor should be placed directly at this pin.
7	ADJ	Feedback voltage input. If connected to the VOUT pin, the output voltage will be set at 0.65V. If external feedback resistors are used, the output voltage will be determined by the resistor ratio.
8, 9 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT9048A is a low input voltage low dropout LDO that supports the input voltage range from 1.6V to 6V and the output current can be up to 1.5A. The RT9048A uses internal charge pump to achieve low input voltage operation and the internal compensation network is well designed to achieve fast transient response with good stability.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the on resistance of the power MOSFET is decreased to increase the output current through the power MOSFET, and the feedback voltage will be charge back to reference. If the feedback voltage is less than the reference, the power MOSFET current is decreased to make the output voltage discharge back to reference by the loading current.

Reverse Current Protection

The reverse current protection is guaranteed by the N-MOSFET with bulk capacitors connected to GND and the internal circuit. The reverse voltage detection circuit shuts the total loop down if the output voltage is higher than input voltage.

UVLO Protection

The RT9048A provides an input under-voltage lockout protection (UVLO). When the input voltage exceeds the UVLO rising threshold voltage (1.43V typ.), the device resets the internal circuit and prepares for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will be shut down. A hysteresis (150mV typ.) between the UVLO rising and falling threshold voltage is designed to avoid noise.

Current Limit Protection

The RT9048A continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.

Output Active Discharge

When the RT9048A is operating at shutdown mode, the device has an internal active pull down circuit that connects the output to GND through a 500Ω resistor for output discharging purpose.

Over-Temperature Protection

The over-temperature protection function will turn off the MOSFET when the junction temperature exceeds160°C (typ.). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation.

Soft-Start

The V_{OUT} soft-start ramp up speed has related with V_{IN} driving ability, with higher V_{IN} input level with faster V_{OUT} ramp up speed and less soft-start time required. Table 1, Table 2, Table 3 and Table 4 show the required soft-start time with different V_{IN} operating range for design reference.

Table 1. Output 0.75V Soft-Start time with V_{IN}

Soft-Start Time of 10%~90% of V_{OUT} rising			
T_{SS} (μs)	V_{OUT} = 0.75V		
V_{IN} (V)	Min	Typ	Max
1.6	130	230	345
2	100	195	310
3	85	165	260
4	75	150	235
5	65	130	210
6	55	110	180

Table 2. Output 0.9V Soft-Start time with V_{IN}

Soft-Start Time of 10%~90% of V_{OUT} rising			
T_{SS} (μs)	V_{OUT} = 0.9V		
V_{IN} (V)	Min	Typ	Max
1.6	135	250	400
2	115	220	340
3	100	185	275
4	85	160	250
5	75	140	220
6	65	120	195

Table 3. Output 1.1V Soft-Start time with V_{IN}

Soft-Start Time of 10%~90% of V_{OUT} rising			
T_{SS} (μs)	V_{OUT} = 1.1V		
V_{IN} (V)	Min	Typ	Max
1.6	160	310	480
2	140	270	410
3	115	220	330
4	100	195	290
5	90	170	270
6	80	150	235

Table 4. Output 1.8V Soft-Start time with V_{IN}

Soft-Start Time of 10%~90% of V_{OUT} rising			
T_{SS} (μs)	V_{OUT} = 1.8V		
V_{IN} (V)	Min	Typ	Max
1.6	--	N/A	--
2	231	425	650
3	175	305	455
4	150	260	380
5	130	235	350
6	120	205	315

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 7V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 3x3 ---------- 3.22W
- Package Thermal Resistance (Note 2)
  WDFN-8L 3x3, θ_{JA} ---------- 31°C/W
  WDFN-8L 3x3, θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 1.6V to 6V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 1.6V to 6V, I_{OUT} = 10μA to 1.5A, V_{ADJ} = V_{OUT} , T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Under-Voltage Lockout	V_{UVLO}	V_{IN} rising	1.31	1.43	1.55	V
	V_{UVLO_Hys}	Hysteresis	--	0.15	--	V
ADJ Reference Voltage	V_{ADJ}	V_{IN} = 3.3V, V_{ADJ} = V_{OUT}, I_{OUT} = 10mA	0.641	0.65	0.659	V
		V_{IN} = 3.3V, V_{ADJ} = V_{OUT}, I_{OUT} = 1.5A (Note 5)	0.637	0.65	0.663	V
ADJ Pin Current	I_{ADJ}	V_{ADJ} = 0.65V	--	20	200	nA
Dropout Voltage	V_{DROP}	I_{OUT} = 1.5A, $V_{IN} \geq$ 1.6V	--	180	300	mV
Line Regulation	ΔV_{LINE}	I_{OUT} = 10mA	--	0.2	--	%/V
Load Regulation	ΔV_{LOAD}	10mA $\leq I_{OUT} \leq$ 1.5A	--	0.33	--	%/A
Quiescent Current	I_Q	V_{IN} = 3.3V, I_{OUT} = 0A	--	0.7	--	mA
Shutdown Current	I_{SHDN}	V_{IN} = 3.3V, V_{EN} = 0V	--	0.1	--	μA
Current Limit	I_{LIM}	V_{IN} = 3.3V	1.5	--	--	A
Discharge Resistance	R_{DISCH}	$V_{EN} \leq$ 0.4V	--	0.5	1	KΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable						
EN Input Voltage, Logic-High	V_{IH_EN}	Enable device	1.4	--	--	V
EN Input Voltage, Logic-Low	V_{IL_EN}	Disable device	--	--	0.4	V
Enable Pin Current	I_{EN}	V_{EN} = V_{IN} = 6V	--	1	10	μA
Over Temperature Protection						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	°C
Reverse Voltage Protection						
Reverse Voltage Protection Threshold	V_{TH_RVP}	V_{OUT} ramps up and above V_{IN}. (Note 5)	--	130	--	mV
Output Soft-Start Time	t_{VOUT_S}	V_{OUT} = 0.75V, V_{OUT} from 10% to 90%	55	--	345	μs
		V_{OUT} = 0.9V, V_{OUT} from 10% to 90%	65	--	400	
		V_{OUT} = 1.1V, V_{OUT} from 10% to 90%	80	--	480	
		V_{OUT} = 1.8V, V_{OUT} from 10% to 90%	120	--	650	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit

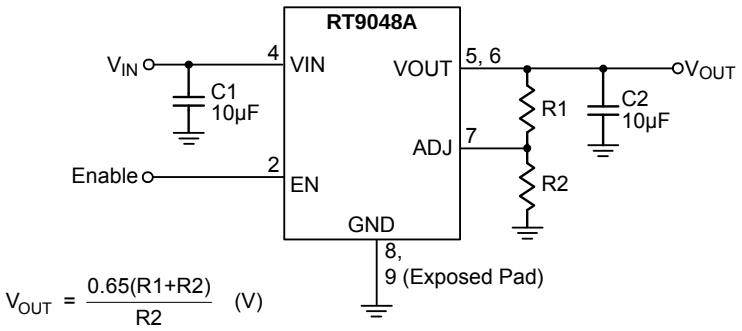
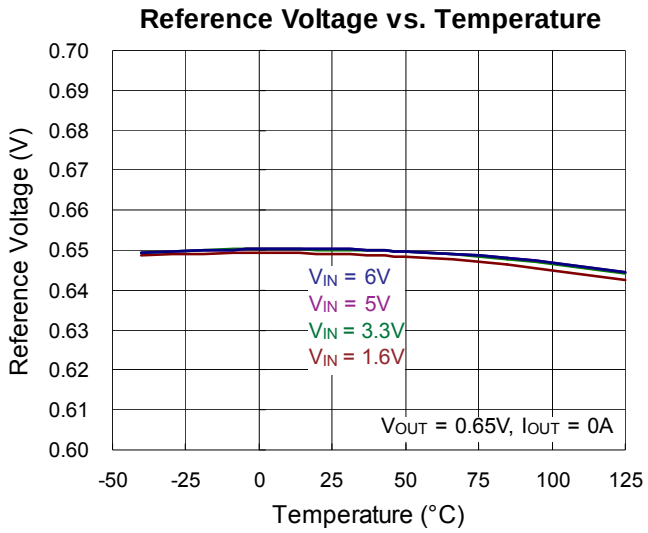
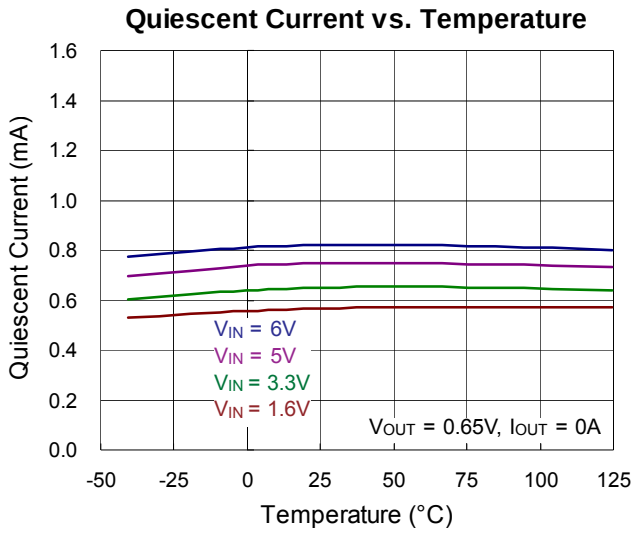
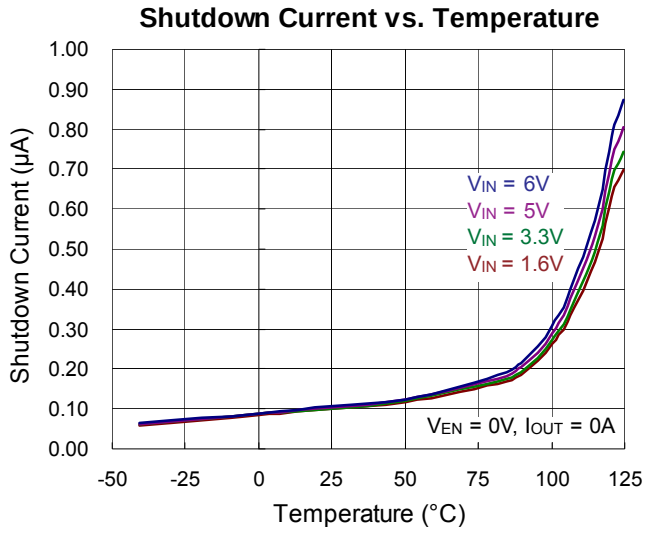


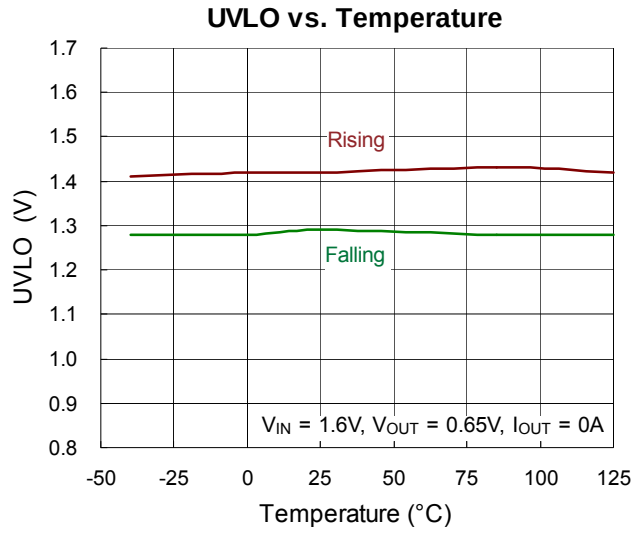
Figure 1. Adjustable Voltage Regulator

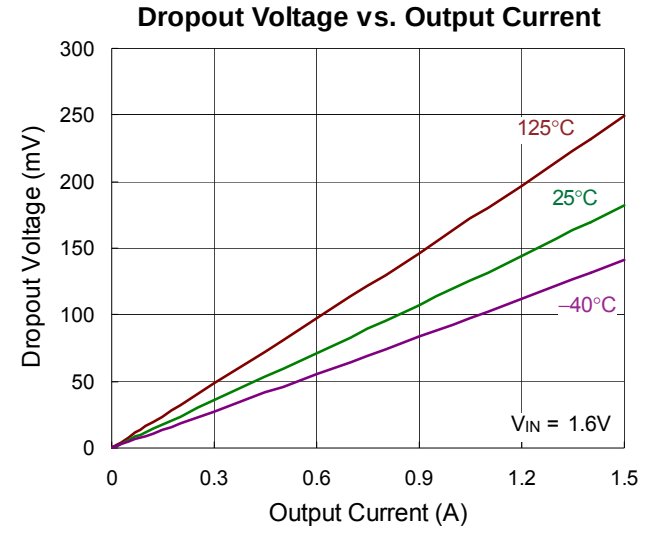
Typical Operating Characteristics

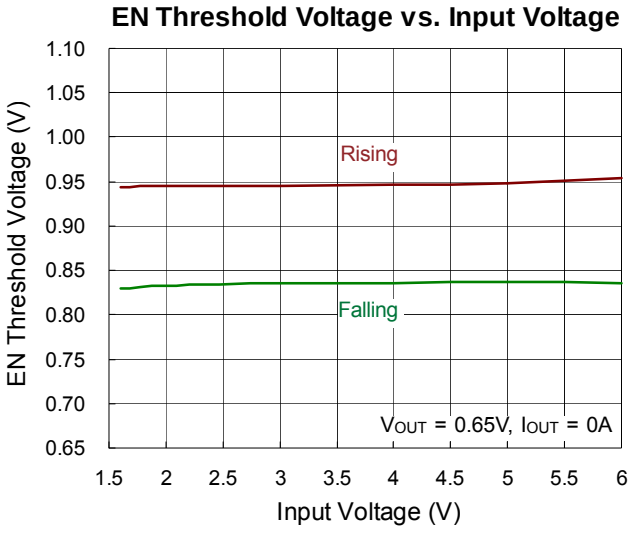




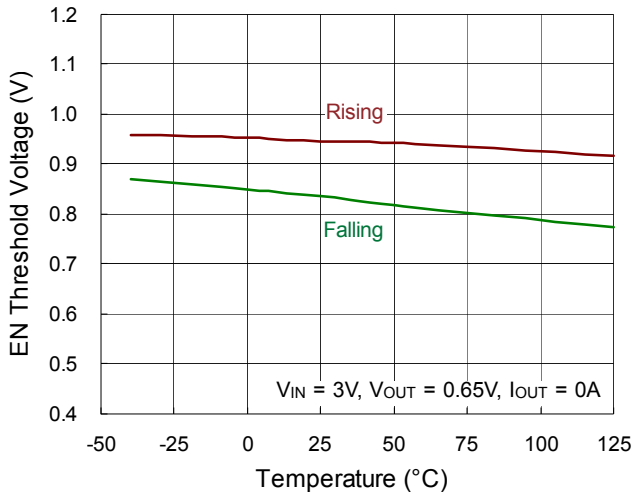




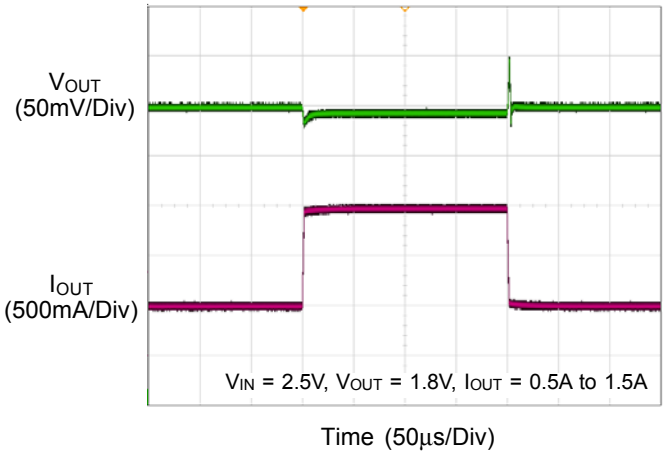




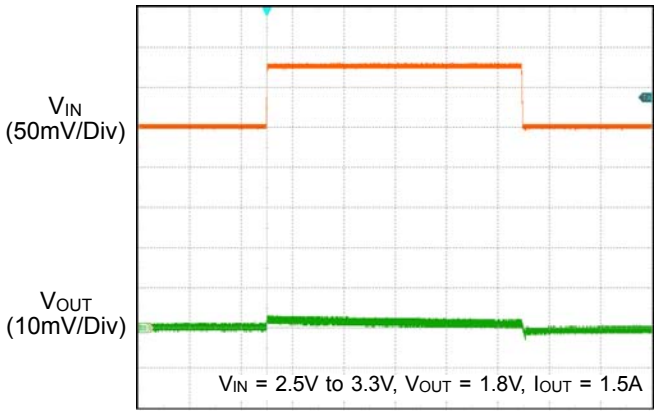
EN Threshold Voltage vs. Temperature



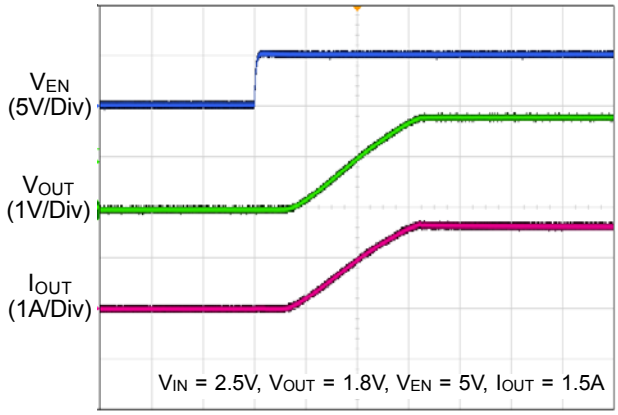
Load Transient Response



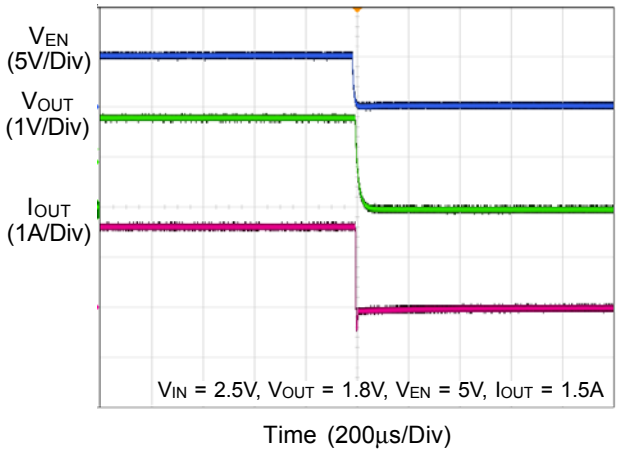
Line Transient Response



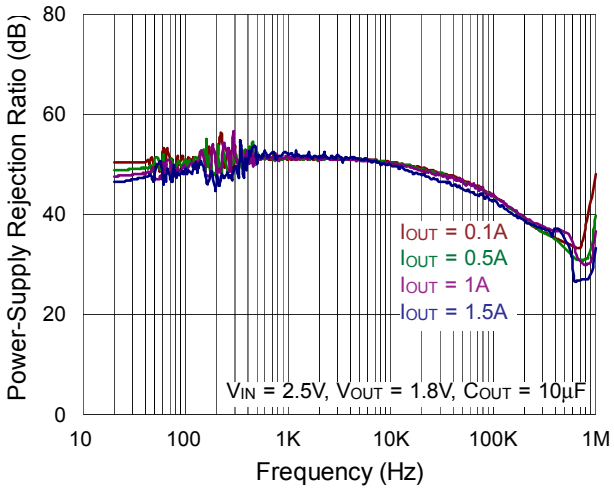
Power On from EN



Power Off from EN



PSRR



Application Information

The RT9048A is a low voltage, low dropout linear regulator. The input voltage supporting range is from 1.6V to 6V and the adjustable output voltage is from 0.65V to (V_{IN} – V_{DROP}).

Output Voltage Setting

The RT9048A output voltage is adjustable from 0.65V to V_{IN} – V_{DROP} via the external resistive voltage divider. The voltage divider resistors can have values of up to 800kΩ because of the very high impedance and low bias current of the sense comparator. The output voltage is set according to the following equation :

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{ADJ} is the reference voltage with a typical value of 0.65V.

Chip Enable Operation

The RT9048A goes into sleep mode when the EN pin is in a logic low or left open condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 0.1μA (typ.). The EN pin can be directly tied to VIN to enable the device and work normally.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as ($V_{DROP} = V_{IN} – V_{OUT} = R_{DS(ON)}$) x I_{RATED}). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response. Vice versa, while operating at the ohmic region will degrade the performance severely.

C_{IN} and C_{OUT} Selection

The RT9048A is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance range from 10μF to 47μF on the output ensures stability.

Input capacitance is selected to minimize transient input droop during load current steps. For general application, the requirement of input capacitor with a 10μF is recommended to minimize input impedance and provide the desired effect and do not affect stability.

Thermal Considerations

Thermal protection limits power dissipation in the RT9048A. When the operation junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by 30°C.

The RT9048A output voltage will be closed to zero when output short circuit occurs as shown in Figure 2. It can reduce the IC temperature and provides maximum safety to end users when output short circuit occurs.

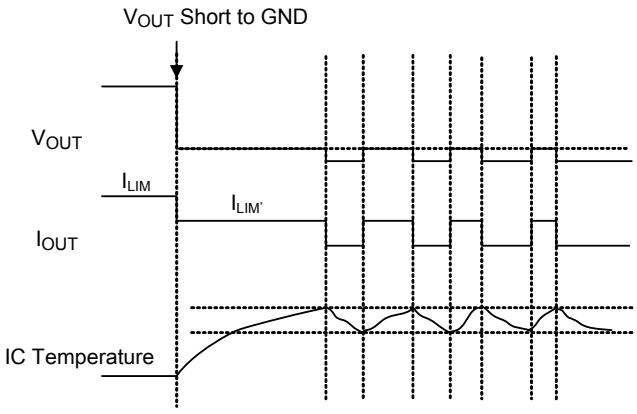


Figure 2. Short Circuit Protection when Output Short Circuit Occurs

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 3x3 package, the thermal resistance, θ_{JA}, is 31°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (31°C/W) = 3.22W for WDFN-8L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

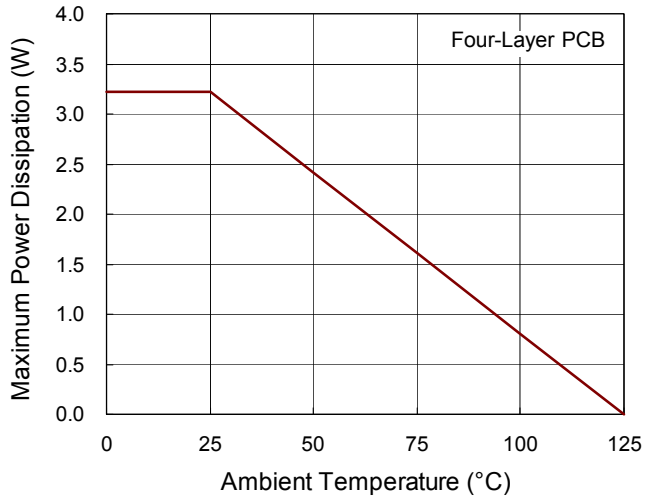


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT9048A, the PCB layout suggestions below are highly recommend. All circuit components placed on the same side and as near to the respective LDO pin as possible. Place the ground return path connection to the input and output capacitor. Connect the ground plane with a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connections is discouraged and has negative effects on performance. Figure 4 shows a layout example that reduce conduction trace loops, helping to minimize inductive parasitics and load transient effects while improving the circuit stability.

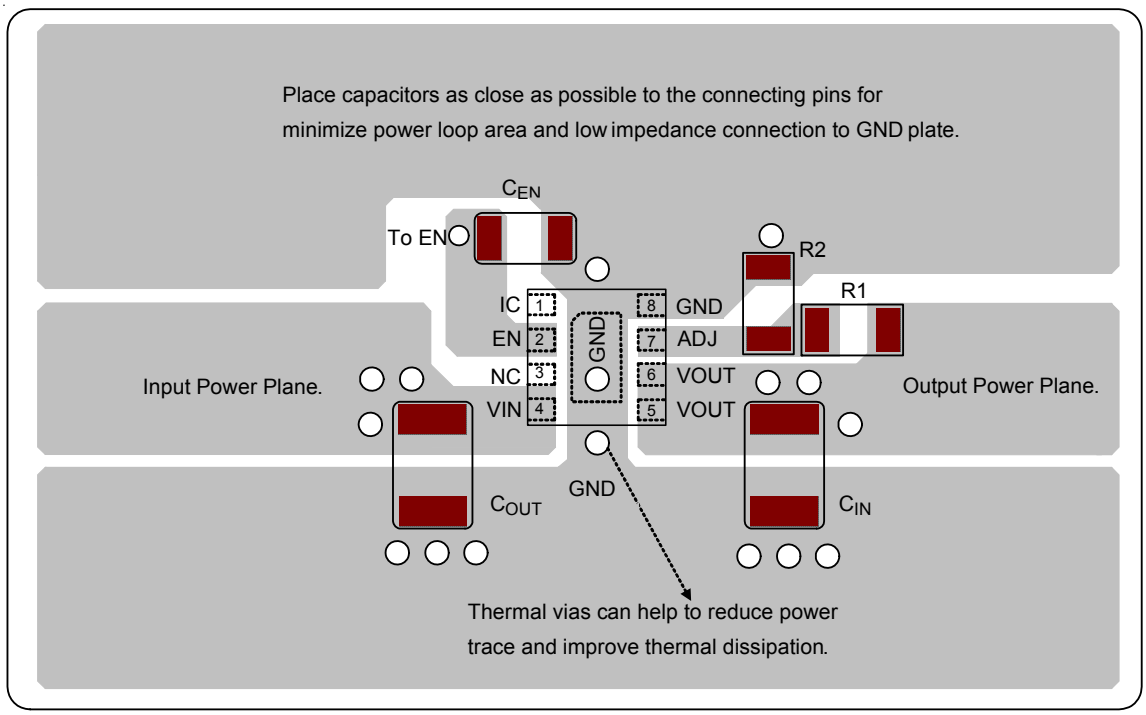
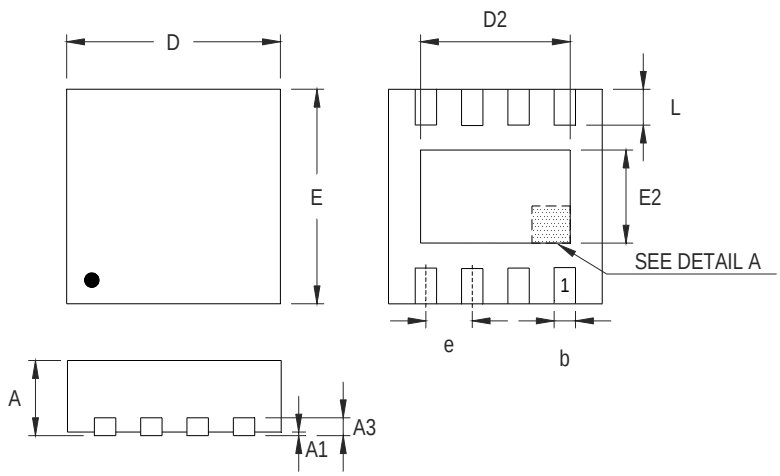
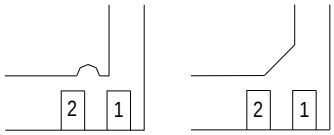


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

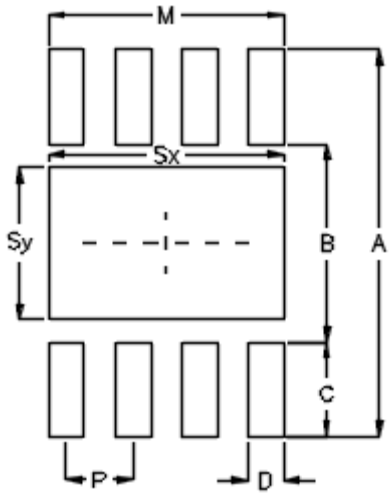
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-8	8	0.65	3.80	1.94	0.93	0.35	2.30	1.50	2.30	±0.05

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