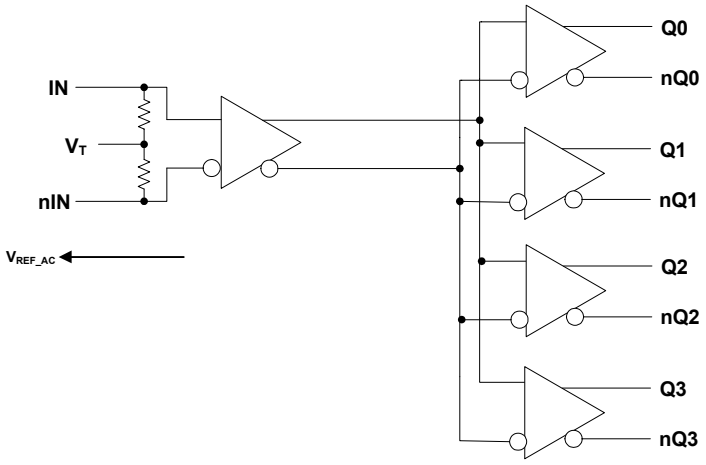
General Description

The ICS8S58021I is a high speed 1-to-4 Differential-to-LVPECL/ECL Fanout Buffer. The ICS8S58021I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVPECL and CML to be easily interfaced to the input with minimal use of external components. The ICS8S58021I is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

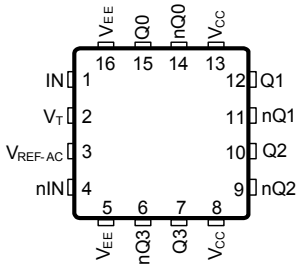
Features

- Four LVPECL/ECL outputs
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- 50Ω internal input termination to V_T
- Output frequency: 2.5GHz (maximum)
- Output skew: 30ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Additive phase jitter, RMS: 0.02ps (typical)
- Propagation Delay: 425ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to 2.375V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8S58021I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type	Description
1	IN	Input	Non-inverting LVPECL differential clock input. R_T = 50Ω termination to V_T.
2	V_T	Input	Input for termination. Both IN, nIN inputs are terminated to this pin. See Application Information section, *Differential Input with Built-In 50Ω Termination Interface.*
3	V_{REF_AC}	Output	Reference voltage for AC-coupled applications.
4	nIN	Input	Inverting differential LVPECL clock input. RT = 50Ω termination to V_T.
5, 16	V_{EE}	Power	Negative supply pins.
6, 7	nQ3, Q3	Output	Differential output pair. LVPECL/ECL interface levels.
8, 13	V_{cc}	Power	Power supply pins.
9, 10	nQ2, Q2	Output	Differential output pair. LVPECL/ECL interface levels.
11, 12	nQ1, Q1	Output	Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ0, Q0	Output	Differential output pair. LVPECL/ECL interface levels.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Input Current, IN, nIN	±25mA
V_T Current, I_{VT}	±50mA
Input Sink/Source, I_{REF_AC}	±2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				80	mA

Table 2B. Differential DC Characteristics, V_{CC} = 2.5V ± 5%, 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance; NOTE 1	(IN, nIN)		40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing			0.15		1.4	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.8	V
I_{IN}	Input Current; NOTE 1	(IN, nIN)				35	mA
V_{REF_AC}	Bias Voltage			V_{CC} – 1.52	V_{CC} – 1.37	V_{CC} – 1.17	V

NOTE 1: Guaranteed by design.

Table 2C. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.16	V_{CC} – 0.94	V_{CC} – 0.765	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 1.955	V_{CC} – 1.78	V_{CC} – 1.57	V
V_{OUT}	Output Voltage Swing		0.6		1.1	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.2	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

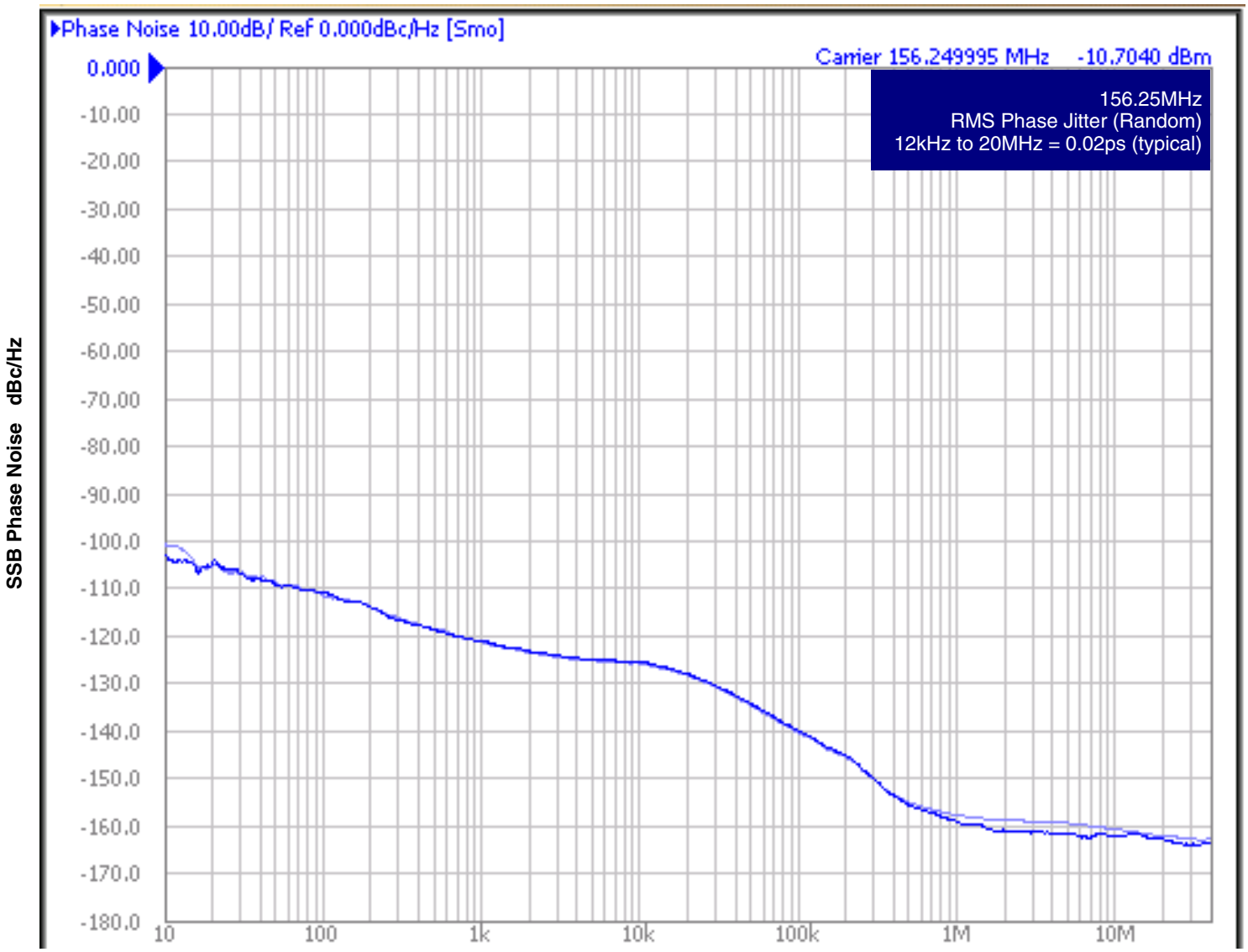
Table 3. AC Characteristics, V_{CC} = 0V; V_{EE} = -3.3V ± 5%, -2.5V ± 5% or V_{CC} = 2.5V ± 5%, 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		200		425	ps
*t*sk(o)	Output Skew; NOTE 2, 4				30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				150	ps
*t*jit	Buffer Additive Jitter; RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz – 20MHz		0.02		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	25		250	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

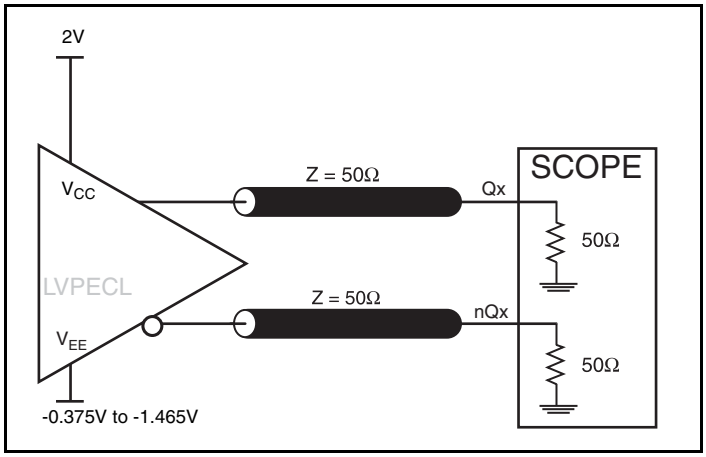
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



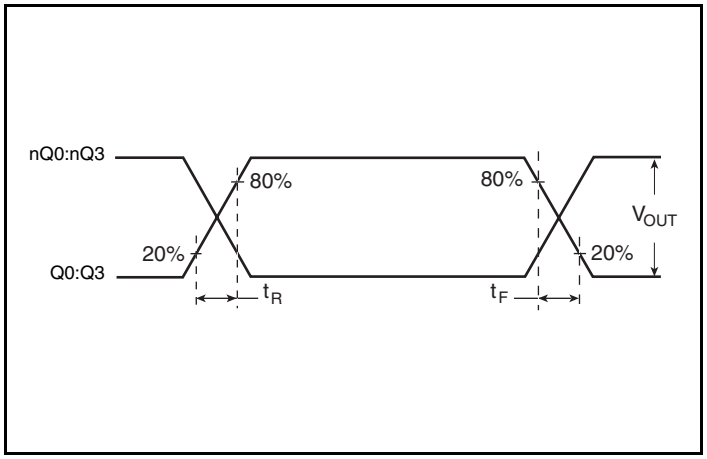
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "Rohde & Schwarz SMA 100A Signal Generator, via the clock synthesis as external input to drive the input clock IN, nIN".

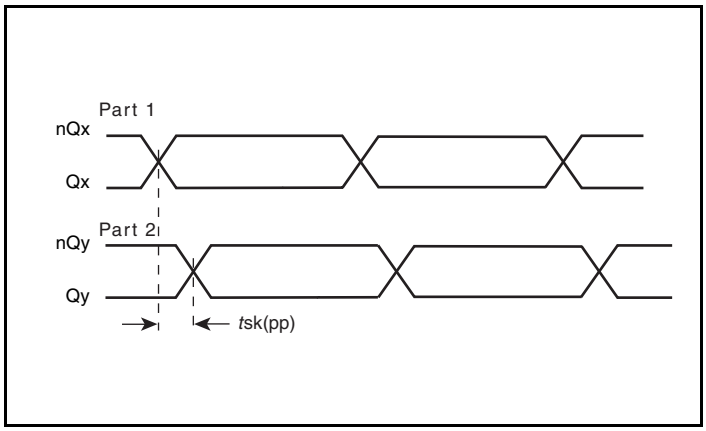
Parameter Measurement Information



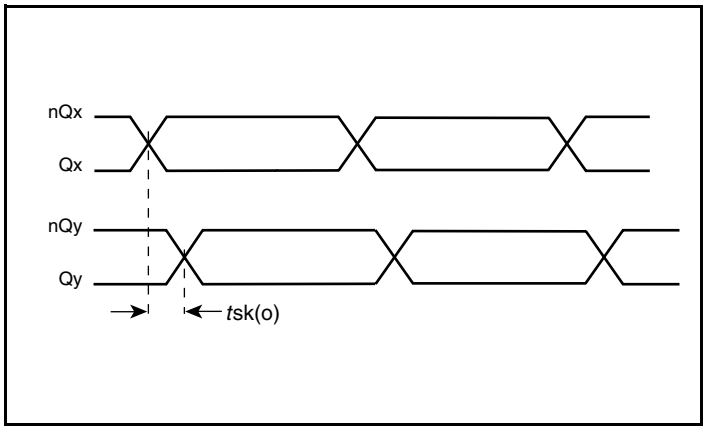
Output Load AC Test Circuit



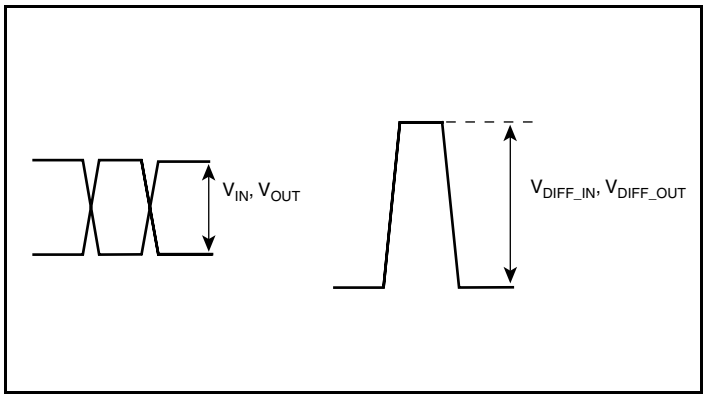
Output Rise/Fall Time



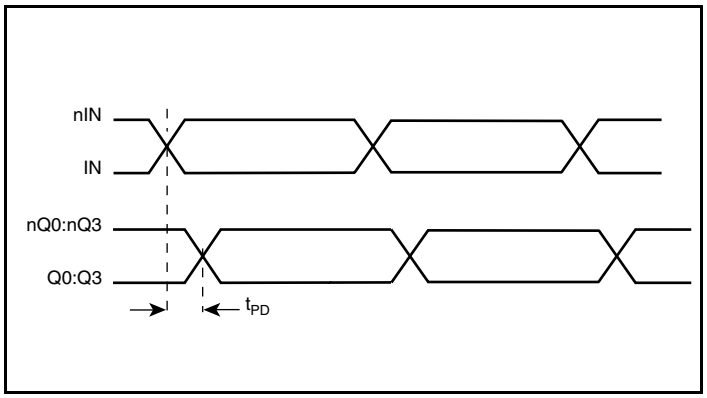
Part-to-Part Skew



Output Skew



Single-ended & Differential Input/Output Voltage Swing



Propagation Delay

Application Information

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

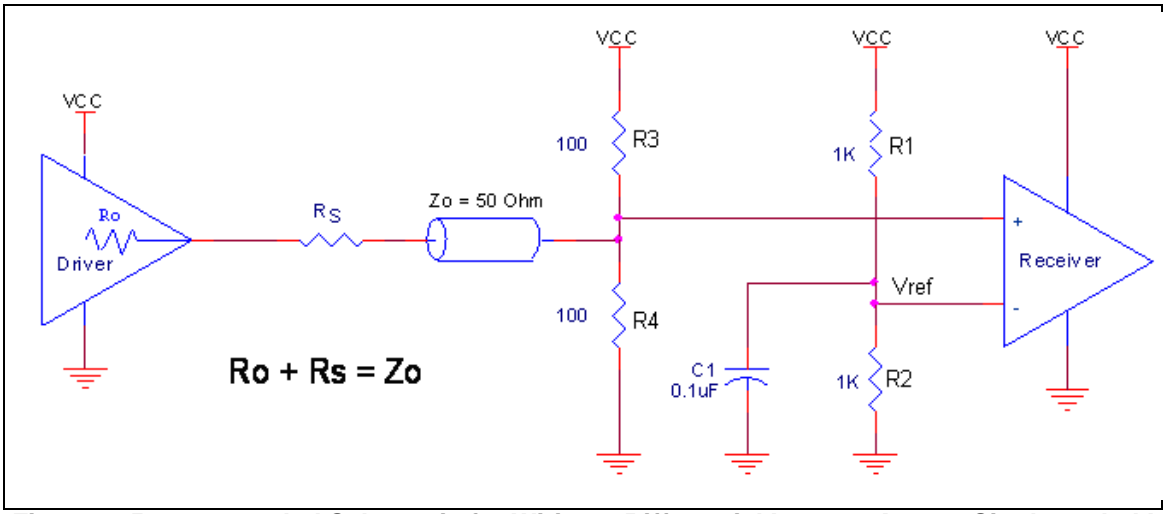


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. The differential signal must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

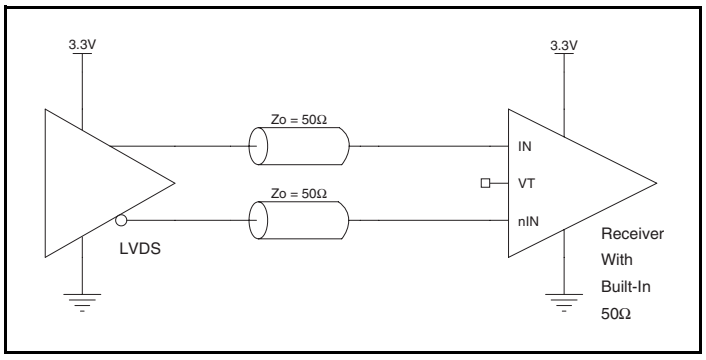


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

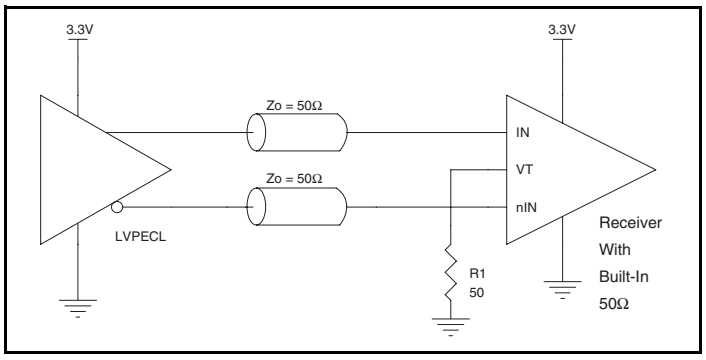


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

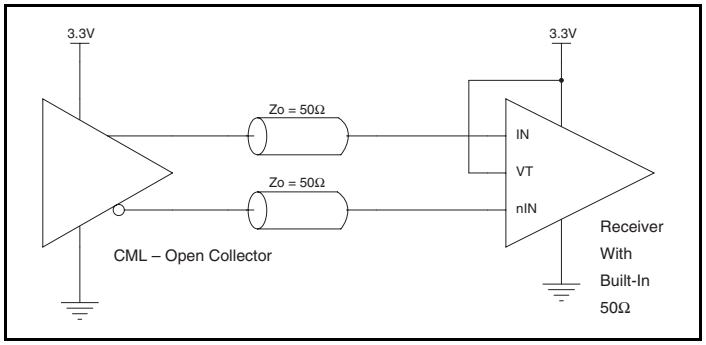


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

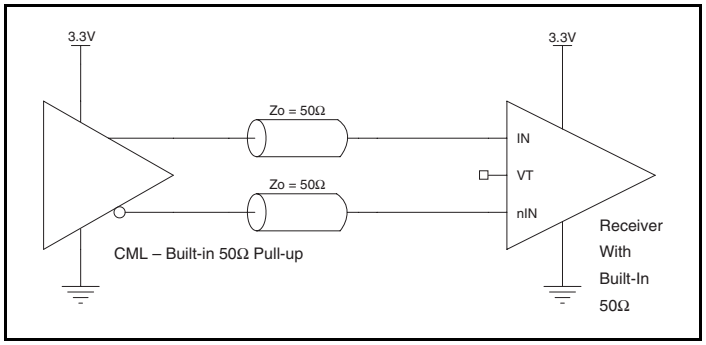


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

2.5V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. The differential signal must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

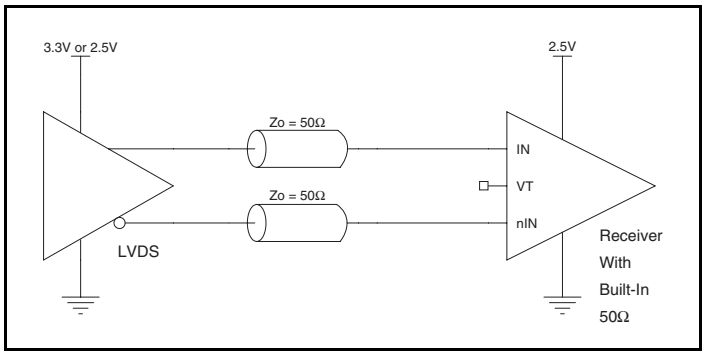


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

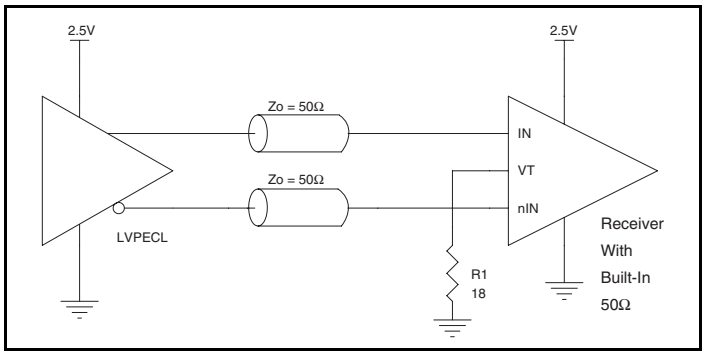


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

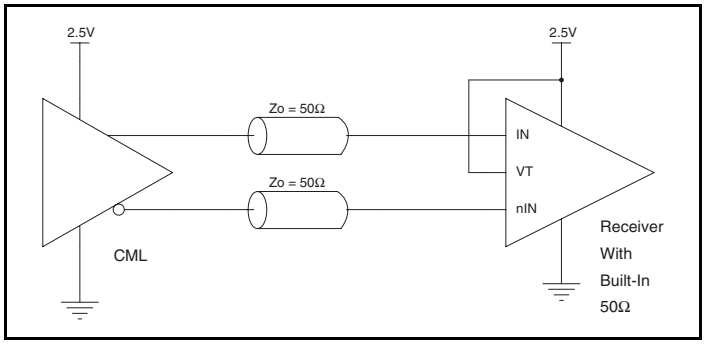


Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

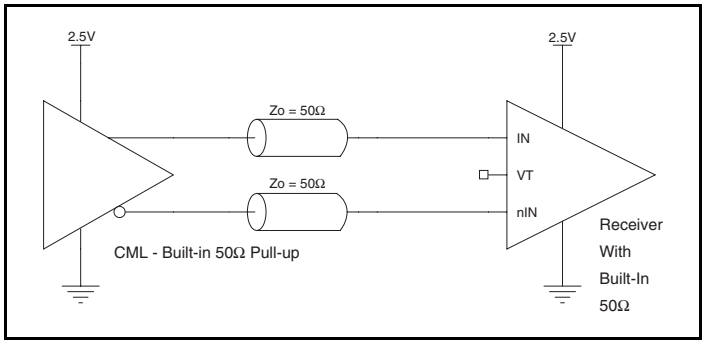


Figure 3D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

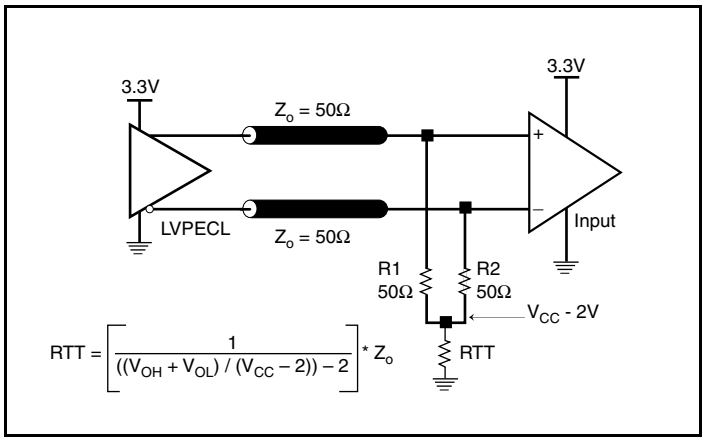


Figure 4A. 3.3V LVPECL Output Termination

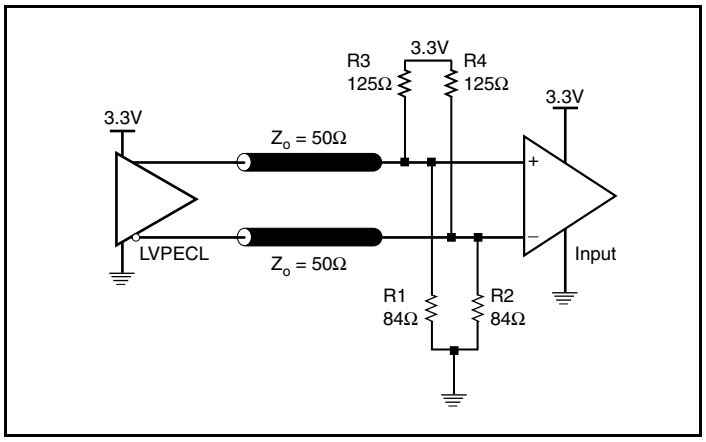


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

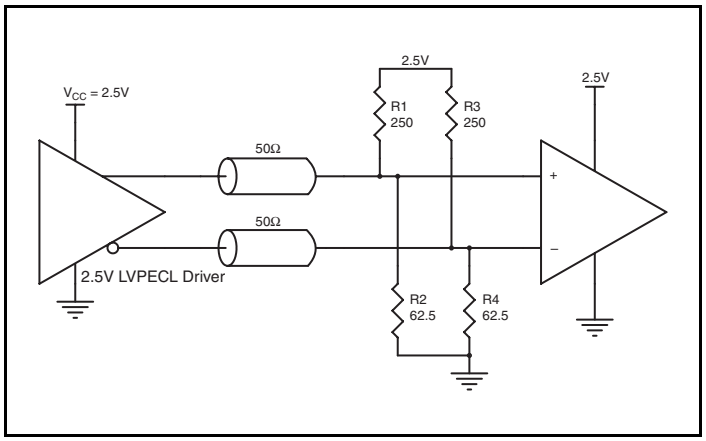


Figure 5A. 2.5V LVPECL Driver Termination Example

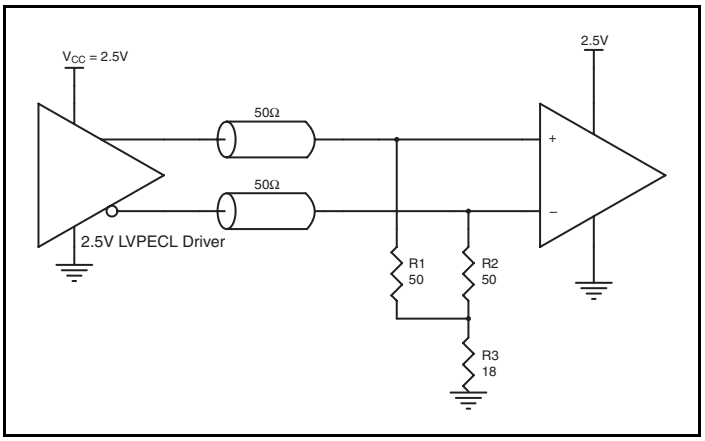


Figure 5B. 2.5V LVPECL Driver Termination Example

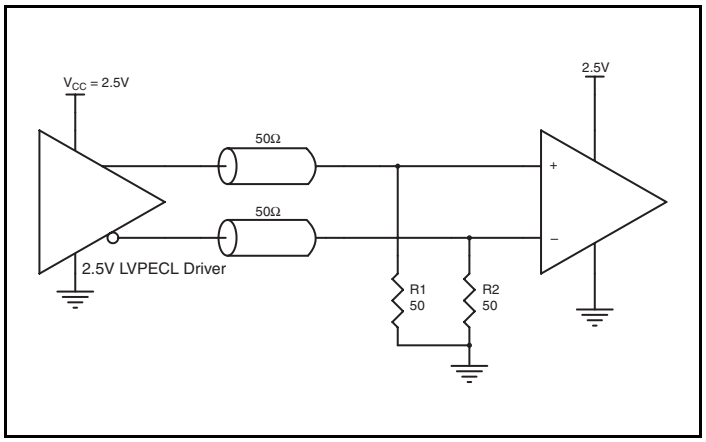


Figure 5C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

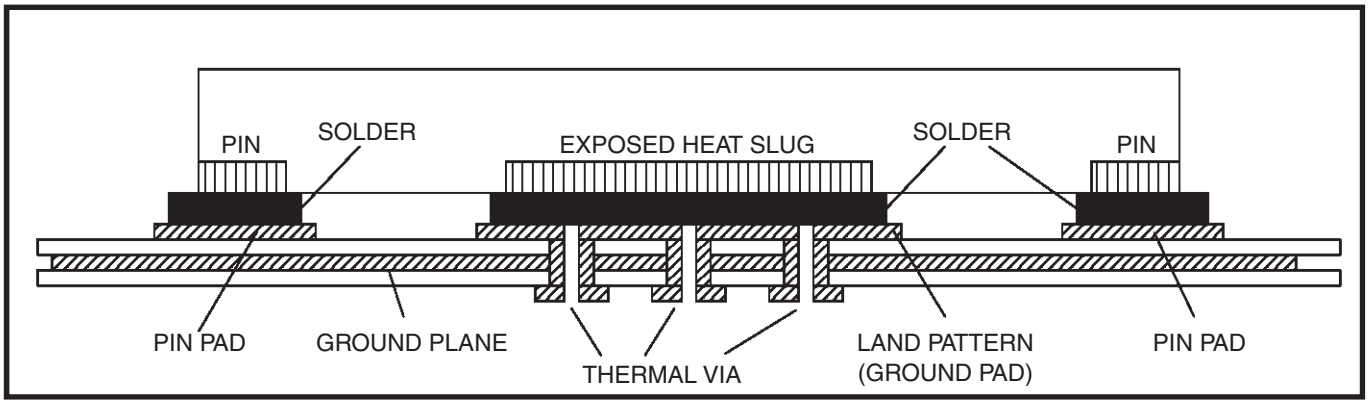


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8S58021I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8S58021I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 80mA = **277.2mW**
- Power $(outputs)_{MAX}$ = **32.4mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32.4mW = **129.6mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 277.2mW + 129.6mW = **406.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature f is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.407W * 74.7°C/W = 115.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 7.*

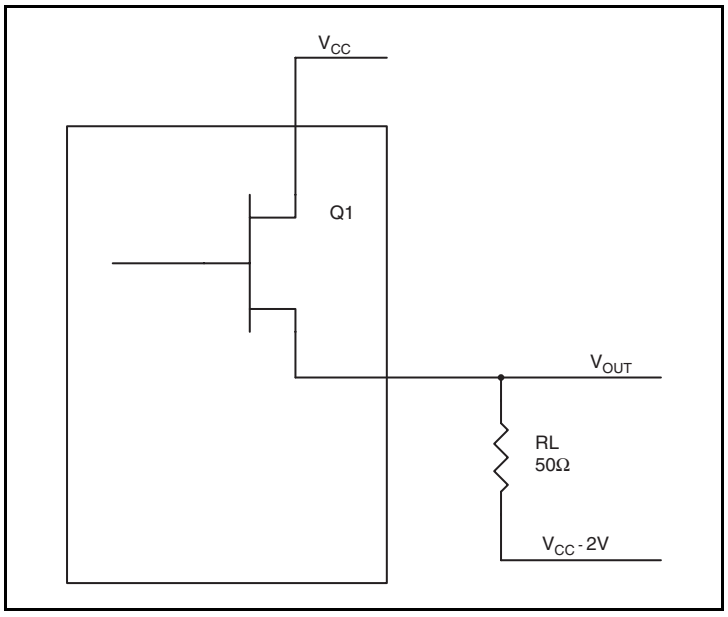


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.765V**
  ($V_{CC\_MAX} - V_{OH\_MAX}$) = **0.765V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.57V**
  ($V_{CC\_MAX} - V_{OL\_MAX}$) = **1.57V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.765V)/50\Omega] * 0.765V =$ **18.9mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.57V)/50\Omega] * 1.57V =$ **13.5mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.4mW**

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

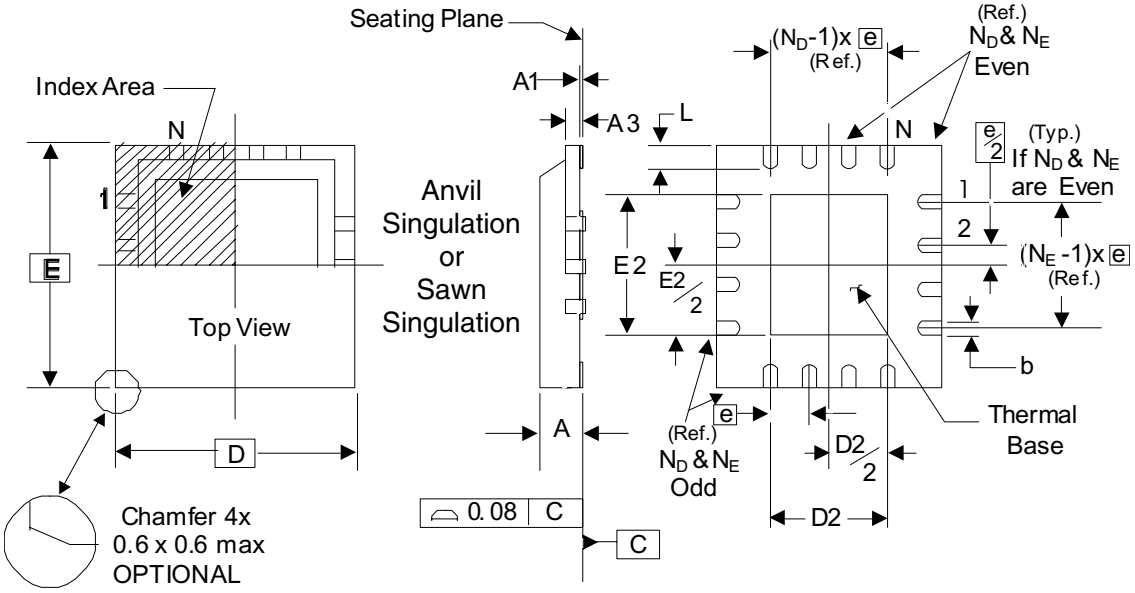
θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

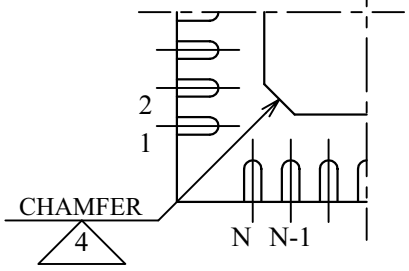
The transistor count for ICS8S58021I is: 262

Package Outline and Package Dimensions

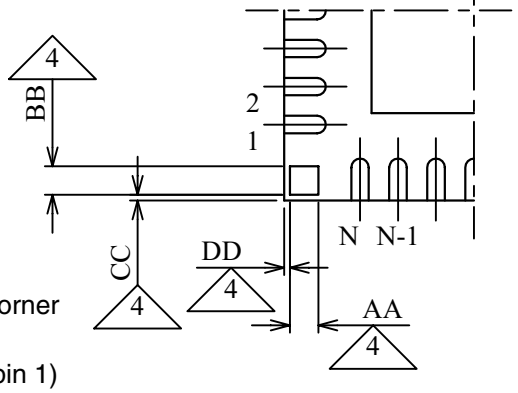
Package Outline - K Suffix for 16 Lead VFQFN



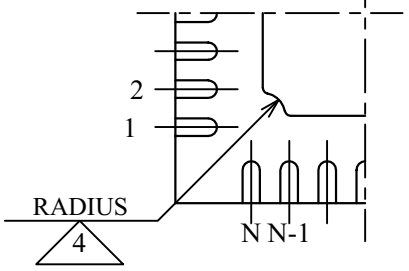
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 6. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S58021AKILF	1AIL	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S58021AKILFT	1AIL	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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(Rev.1.0 Mar 2020)

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