OPAx310 High Output Current, Fast Shutdown, Low Voltage (1.5 V to 5.5 V), RRIO, 3-MHz Operational Amplifier

1 Features

- High output current: ±150-mA typical I_{SC} at 5.5 V
- Fast enable from shutdown: 1-µs typical
- Wide operational supply voltage: 1.5 V to 5.5 V
- Low input offset voltage: ±250-µV typical
- Fail-safe inputs: No diode from inputs to V+
- Optimized quiescent current: 165-µA/ch typical
- Rail-to-rail input and output
- Gain bandwidth product: 3-MHz typical at 5.5 V
- Thermal noise floor: 16-nV/$\sqrt{Hz}$ typical
- Unity-gain stable
- Drives up to 250-pF without sustained oscillations
- Internal RFI and EMI filtered input pins
- Operating temperature range: –40°C to 125°C

2 Applications

- Optical modules
- Reference buffers, guard amplifiers
- Microphone pre-amplifiers
- Lighting and LED Drivers
- 4-20 mA loop drivers
- Programmable current source
- Low side current sensing circuitry

3 Description

The OPAx310 family of op amps includes single (OPA310), dual (OPA2310), and quad-channel (OPA4310), low-voltage (1.5 V to 5.5 V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPAx310S also features a very fast shutdown response and has a typical enable, disable time of 1 µs that allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310 family has a robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

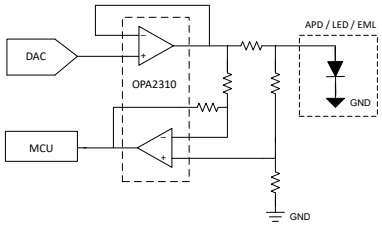
OPAx310 is offered in power pad, standard, small size package variants and has an internal current limit protection, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310 can swing very close to the rails and has a short-circuit current of 75-mA minimum across temperature at 5.5-V power supply. Additional output current capability may be achieved by carefully connecting multiple op amps in parallel. OPAx310 devices are an excellent choice for LED driver, LCD driver, laser driver, TEC driver applications and can also be used as a reference buffer, guard amplifier, or as a discrete LDO.

The robust design of the OPAx310 family simplifies circuit design. These op amps feature an integrated RFI and EMI rejection filter with no-phase reversal in input overdrive conditions. These devices also deliver excellent AC performance with a gain bandwidth of 3 MHz and can drive up to 250 pF of cap load with no sustained oscillations, enabling designers to achieve both improved performance and a lower-power consumption.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
OPA310(2)	SOT-23 (5)	1.60 mm × 2.90 mm
	SC70 (5)	1.25 mm × 2.00 mm
	X2SON (5)	0.80 mm × 0.80 mm
	SOT-5X3 (5)	1.20 mm × 1.60 mm
OPA310S(2)	SOT-23 (6)	1.60 mm × 2.90 mm
	SC70 (6)	1.25 mm × 2.00 mm
OPA2310	SOIC (8)	3.91 mm × 4.90 mm
	SOT-23 (8)(3)	1.60 mm × 2.90 mm
	WSON (8)	2.00 mm × 2.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	TSSOP (8)(3)	3.00 mm × 4.40 mm
OPA2310S(2)	X2QFN (10)	1.50 mm × 2.00 mm
	HVSSOP (10)	3.00 mm × 3.00 mm
OPA4310(2)	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	X2QFN (14)	2.00 mm × 2.00 mm
OPA4310S(2)	WQFN (16)	3.00 mm × 3.00 mm
	SOT-23 (16)	4.20 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Part number is for preview only.
(3) Package is for preview only.



APD / LED / EML Biasing With Current Sense

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (July 2022)	Page
• Changing DGK from "Preview" to "Production"	1
• Updated *Device Comparison* section to include information about shutdown	3
• Removed preview tag for the DGK package	3
• Added "shutdown section is on preview" foot note to the *Specifications* section	10
• Updated the *ESD and Electrical Overstress* section to show ESD structures on the shutdown pin	29

Changes from Revision * (April 2022) to Revision A (June 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	SHDN	PACKAGE LEADS													
			SC70 DCK	SOIC D	SOT-23 DBV	SOT-23 DDF(2)	SOT-553 DRL	SOT-23 DYY	TSSOP PW (2)	VSSOP DGK	HVSSOP DGQ	WQFN RTE	WSON DSG	X2QFN RUC	X2SON DPW	X2QFN RUG
OPA310 (1)	1	NO	5	—	5		5	—	—	—	—	—	—	—	5	—
OPA310S (1)	1	YES	6	—	6		—	—	—	—	—	—	—	—	—	—
OPA2310	2	NO	—	8	—	8	—	—	8	8	—	—	8	—	—	—
OPA2310S (1)	2	YES	—	—	—	—	—	—	—	—	10	—	—	—	—	10
OPA4310 (1)	4	NO	—	14	—	—	—	—	14	—	—	—	—	14	—	—
OPA4310S (1)	4	YES	—	—	—	—	—	16	—	—	—	16	—	—	—	—

(1) Devices are preview only.
(2) Packages are preview only.

6 Pin Configuration and Functions

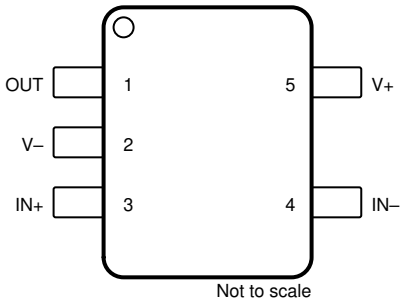


Figure 6-1. OPA310 DBV Package
5-Pin SOT-23
(Top View)

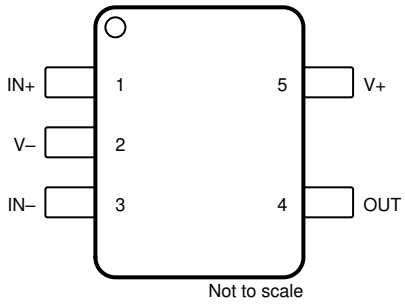


Figure 6-2. OPA310 DCK and DRL Package
5-Pin SC70 and 5-Pin SOT-5X3
(Top View)

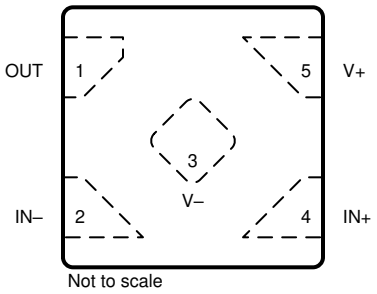


Figure 6-3. OPA310 DPW Package
5-Pin X2SON
(Top View)

Table 6-1. Pin Functions: OPA310

PIN				I/O	DESCRIPTION
NAME	SOT-23	SC70, SOT-5X3	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

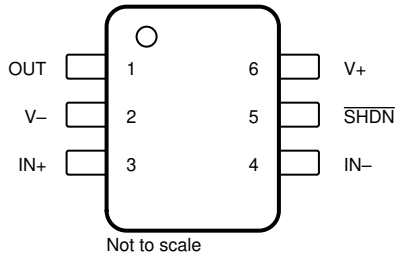


Figure 6-4. OPA310S DBV Package
6-Pin SOT-23
(Top View)

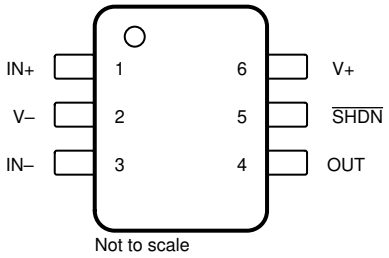


Figure 6-5. OPA310S DCK Package
6-Pin SC70
(Top View)

Table 6-2. Pin Functions: OPA310S

PIN			I/O	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{\text{SHDN}}$	5	5	I	Shutdown: low = amp disabled, high = amp enabled See *Shutdown Function* for more information
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

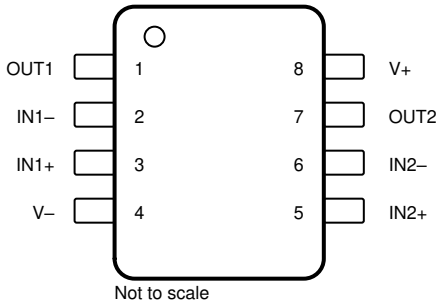
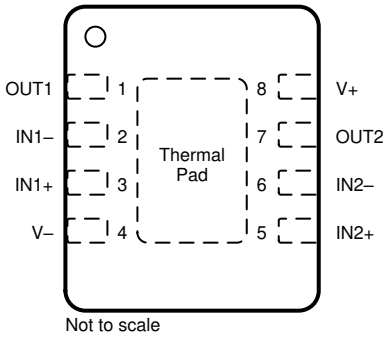


Figure 6-6. OPA2310 D, DDF, DGK, and PW Package
8-Pin SOIC, SOT-23-THIN, VSSOP, and TSSOP
(Top View)



Connect exposed thermal pad to V–. See Section 8.3.10 for more information.

Figure 6-7. OPA2310 DSG Package
8-Pin WSON with Exposed Thermal Pad
(Top View)

Table 6-3. Pin Functions: OPA2310

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

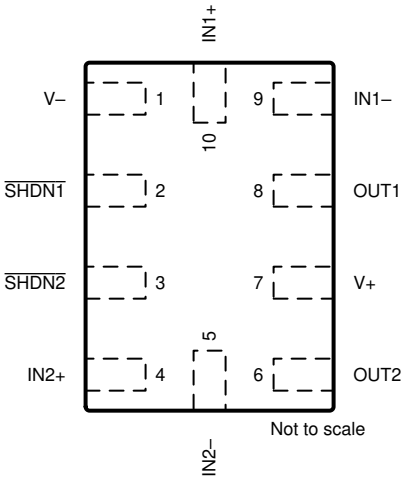


Figure 6-8. OPA2310S RUG Package
10-Pin X2QFN
(Top View)

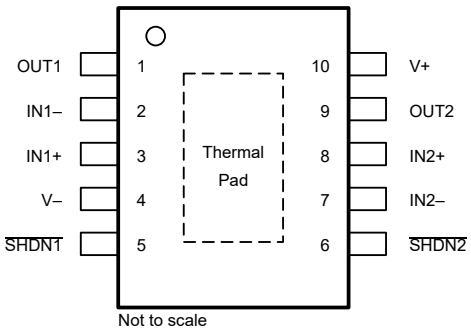


Figure 6-9. OPA2310S DGQ Package
10-Pin HVSSOP
(Top View)

Table 6-4. Pin Functions: OPA2310S

PIN			I/O	DESCRIPTION
NAME	X2QFN	HVSSOP		
IN1–	9	2	I	Inverting input, channel 1
IN1+	10	3	I	Noninverting input, channel 1
IN2–	5	7	I	Inverting input, channel 2
IN2+	4	8	I	Noninverting input, channel 2
OUT1	8	1	O	Output, channel 1
OUT2	6	9	O	Output, channel 2
$\overline{\text{SHDN1}}$	2	5	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 See *Shutdown Function* for more information
$\overline{\text{SHDN2}}$	3	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 2 See *Shutdown Function* for more information
V–	1	4	I	Negative (low) supply or ground (for single-supply operation)
V+	7	10	I	Positive (high) supply

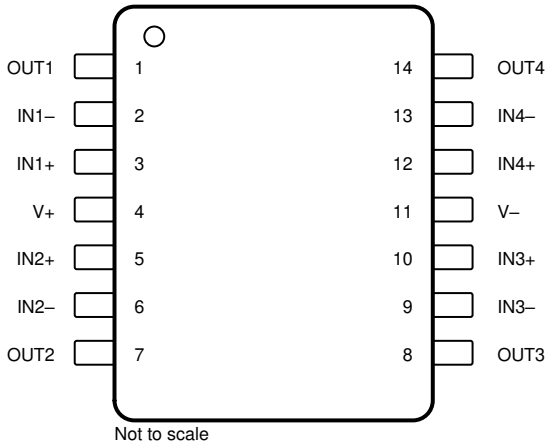


Figure 6-10. OPA4310 D and PW Package 14-Pin SOIC and TSSOP (Top View)

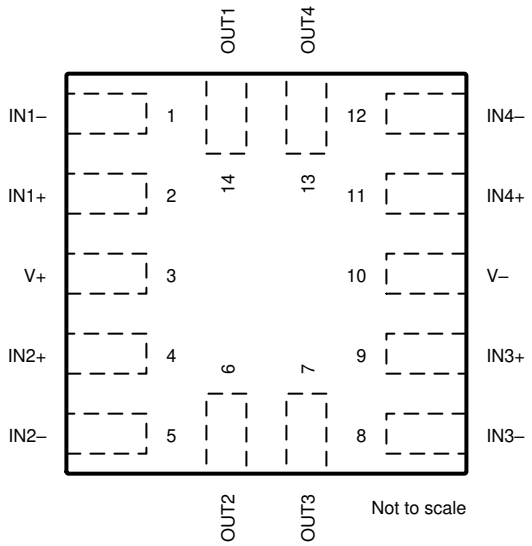
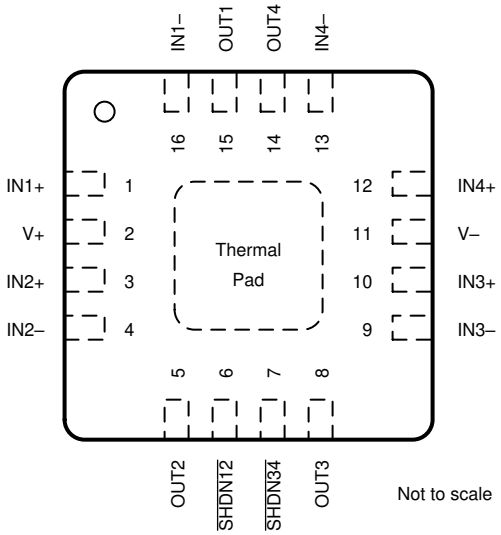


Figure 6-11. OPA4310 RUC Package 14-Pin X2QFN (Top View)

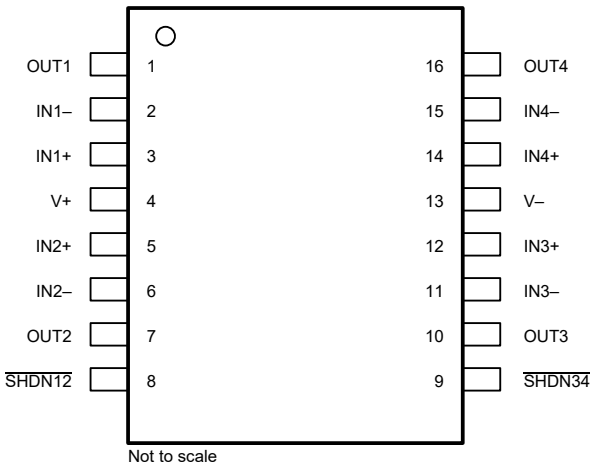
Table 6-5. Pin Functions: OPA4310

PIN			I/O	DESCRIPTION
NAME	SOIC, TSSOP	X2QFN		
IN1–	2	1	I	Inverting input, channel 1
IN1+	3	2	I	Noninverting input, channel 1
IN2–	6	5	I	Inverting input, channel 2
IN2+	5	4	I	Noninverting input, channel 2
IN3–	9	8	I	Inverting input, channel 3
IN3+	10	9	I	Noninverting input, channel 3
IN4–	13	12	I	Inverting input, channel 4
IN4+	12	11	I	Noninverting input, channel 4
OUT1	1	14	O	Output, channel 1
OUT2	7	6	O	Output, channel 2
OUT3	8	7	O	Output, channel 3
OUT4	14	13	O	Output, channel 4
V–	11	10	I	Negative (low) supply or ground (for single-supply operation)
V+	4	3	I	Positive (high) supply



A. Connect thermal pad to V–.

Figure 6-12. OPA4310S RTE Package
16-Pin WQFN With Exposed Thermal Pad
(Top View)



A. Connect thermal pad to V–.

Figure 6-13. OPA4310S DYY Package
16-Pin SOT-23-THIN
(Top View)

Table 6-6. Pin Functions: OPA4310S

PIN			I/O	DESCRIPTION
NAME	WQFN	SOT-23-THIN		
IN1+	1	3	I	Noninverting input, channel 1
IN1–	16	2	I	Inverting input, channel 1
IN2+	3	5	I	Noninverting input, channel 2
IN2–	4	6	I	Inverting input, channel 2
IN3+	10	12	I	Noninverting input, channel 3
IN3–	9	11	I	Inverting input, channel 3
IN4+	12	14	I	Noninverting input, channel 4
IN4–	13	15	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	8	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See *Shutdown Function* for more information
$\overline{\text{SHDN34}}$	7	9	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See *Shutdown Function* for more information
OUT1	15	1	O	Output, channel 1
OUT2	5	7	O	Output, channel 2
OUT3	8	10	O	Output, channel 3
OUT4	14	16	O	Output, channel 4
V–	11	13	I	Negative (low) supply or ground (for single-supply operation)
V+	2	4	I	Positive (high) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Supply voltage, V_S = (V+) – (V–)	0	7	V
Signal input pins	Common-mode voltage (2) (3)	– 0.5	6.0	V
	Differential voltage (2) (3)		±6.0	V
	Current (3)	–10	10	mA
Output short-circuit (4)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins can swing beyond (V+) as long as they stay with in 6.0 V. No diode structure from input pins to (V+).
(3) Input pins are diode-clamped to (V–). Input signals that 0.3 V below (V–) must be current-limited to 10 mA or less.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.5	5.5	V
V_I	Input voltage range	– 0.1	5.6	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information for Single Channel

THERMAL METRIC (1)		OPA310				OPA310S		UNIT
		DBV (2) (SOT-23)	DCK (2) (SC70)	DPW (2) (X2SON)	DRL (2) (X2SON)	DBV (2) (SOT-23)	DCK (2) (SC70)	
		5 PINS	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is on preview.

7.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		OPA2310					OPA2310S		UNIT
		DSG (WSON)	D (SOIC)	DDF (2) (SOT-23-8)	DGK (VSSOP)	PW (2) (TSSOP)	DGQ (2) (HVSSOP)	RUG (2) (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	139.0	TBD	187.7	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	112.1	81.2	TBD	78.1	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	82.4	TBD	109.5	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	31.3	TBD	17.9	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.3	81.6	TBD	107.9	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	31.8	N/A	TBD	N/A	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is on preview.

7.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		OPA4310			OPA4310S		UNIT
		RUC (2) (X2QFN)	D (2) (SOIC)	PW (2) (TSSOP)	RTE (2) (WQFN)	DYY (2) (SOT)	
		14 PINS	14 PINS	14 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is on preview.

7.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.25	±1.3	mV
		V_{CM} = V–	T_A = –40°C to 125°C			±1.4	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±0.5		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 1.5 V to 5.5 V , V_{CM} = V–			±10	±50	µV/V
	Channel separation	f = 10 kHz			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_S = 1.8 V and V_S = 5 V			±1	±30	pA
I_{OS}	Input offset current (1)	V_S = 1.8 V and V_S = 5 V			±0.5	±25	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10 Hz			4		μV_{PP}
e_N	Input voltage noise density	f = 100 Hz			32		$nV/\sqrt{Hz}$
		f = 1 kHz			16		
		f = 10 kHz			13		
i_N	Input current noise (3)	f = 1 kHz			10		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range (1)	V_S = 1.8 V	T_A = –40°C to 125°C	(V–)		(V+)	V
	Common-mode voltage range (1)	V_S = 5.5 V	T_A = –40°C to 125°C	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) ≤ V_{CM} ≤ (V+) – 0.6 V		75	85		dB
		V_S = 1.8 V, (V–) ≤ V_{CM} ≤ (V+) – 0.6 V	T_A = –40°C to 125°C	65	78		dB
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.6 V		83	95		dB
		V_S = 5.5 V, (V–) ≤ V_{CM} ≤ (V+) – 0.6 V	T_A = –40°C to 125°C	75	85		dB
		Full Range: V_S = 1.8 V, (V–) ≤ V_{CM} ≤ (V+)	T_A = –40°C to 125°C	57.5	70		
		Full Range: V_S = 5.5 V (V–) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.1 V	T_A = –40°C to 125°C	66.5	80		
INPUT IMPEDANCE							
Z_{ID}	Differential Input Impedance				80 || 1.4		GΩ || pF
Z_{ICM}	Common-mode Input Impedance				100 || 0.5		GΩ || pF

7.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ to V_S / 2		102	115		dB
	Open-loop voltage gain(2)	V_S = 1.8 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 2 kΩ to V_S / 2		95	105		dB
		V_S = 5.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 10 kΩ to V_S / 2		109	125		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ to V_S / 2		105	115		dB
	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C	90	100		dB
		V_S = 1.8 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 2 kΩ to V_S / 2			90		
		V_S = 5.5 V, (V–) + 0.10 V < V_O < (V+) – 0.10 V, R_L = 10 kΩ to V_S / 2			105		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ to V_S / 2		90	100		
	Open-loop voltage gain (6)	V_S = 3.3 V, (V–) + 0.25 V < V_O < (V+) – 0.25 V, I_L = ±50 mA	T_A = 25°C	80	102		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 1.8 V, G = +1, R_L = 10 kΩ, C_L = 100 pF			2.5		MHz
		V_S = 5.5 V, G = +1, R_L = 10 kΩ, C_L = 100 pF			3		MHz
SR	Slew rate	V_S = 1.8 V, G = +1, R_L = 10 kΩ			2.8		V/µs
		V_S = 5.5 V, G = +1, R_L = 10 kΩ			3		V/µs
THD+N	Total harmonic distortion + noise (4)	G = +1, V_O = 1 V_{RMS}, f = 1 kHz, R_L = 10 kΩ to V_S / 2			0.0005		%
		G = +1, V_O = 1 V_{RMS}, f = 1 kHz, R_L = 2 kΩ to V_S / 2			0.0035		%
		G = +1, V_O = 1 V_{RMS}, f = 1 kHz, R_L = 600 Ω to V_S / 2			0.0080		%
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			1.8		µs
		To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			1.3		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			2.3		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			1.6		
PM	Phase margin	G = +1, R_L = 10 kΩ connected to V_S/2, C_L = 10 pF			60		°
C_L Drive	Cap Load Drive	G = +1, R_L = 10 kΩ connected to V_S/2, Phase Margin = 40°			75		pF
		G = +1, R_L = 10 kΩ connected to V_S/2, No Sustained Oscillations			250		pF
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S			0.6		µs
EMIRR	Electro-magnetic interference rejection ratio	f = 1.8 GHz, V_{IN_EMIRR} = 100 mV			75		dB

7.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8 V, R_L = 2 kΩ to V_S / 2			10	21	mV
		V_S = 1.8 V, R_L = 10 kΩ to V_S / 2			2	11	
		V_S = 1.8 V, R_L = 2 kΩ to V_S / 2	T_A = –40°C to 125°C			51	
		V_S = 1.8 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C			26	
		V_S = 5.5 V, R_L = 2 kΩ to V_S / 2			3.5	20	
		V_S = 5.5 V, R_L = 10 kΩ to V_S / 2			0.75	9	
		V_S = 5.5 V, R_L = 2 kΩ to V_S / 2	T_A = –40°C to 125°C			30	
		V_S = 5.5 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C			14	
V_{OL}	Voltage output swing from negative rail	V_S = 1.8 V, R_L = 2 kΩ to V_S / 2			5.5	15	
		V_S = 1.8 V, R_L = 10 kΩ to V_S / 2			1.2	10	
		V_S = 1.8 V, R_L = 2 kΩ to V_S / 2	T_A = –40°C to 125°C			45	
		V_S = 1.8 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C			25	
		V_S = 5.5 V, R_L = 2 kΩ to V_S / 2			3.5	17.5	
		V_S = 5.5 V, R_L = 10 kΩ to V_S / 2			0.75	6	
		V_S = 5.5 V, R_L = 2 kΩ to V_S / 2	T_A = –40°C to 125°C			27.5	
		V_S = 5.5 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C			11	
I_{SC}	Short-circuit current (5)	V_S = 1.8 V			±20		mA
	Short-circuit current (2) (5)	V_S = 1.8 V, T_A = –40°C to 125°C		±6			mA
	Short-circuit current (5)	V_S = 5.5 V		±75	±150		mA
Z_O	Open-loop output impedance	f = 10 kHz			1000		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 1.5 V, I_O = 0 A			165	190	µA
		V_S = 1.5 V, I_O = 0 A	T_A = –40°C to 125°C		165	210	µA
		V_S = 5.5 V, I_O = 0 A			165	200	µA
			T_A = –40°C to 125°C			215	
	Power-on time	At T_A = 25°C, V_S = 5.5 V, V_S ramp rate > 0.3 V/µs			125		µs
SHUTDOWN							
I_{Q_SHDN}	Shutdown current per amplifier (8)	All amplifiers disabled, $\overline{SHDN}$ = V–			0.5	1	µA
	Shutdown current per amplifier (8)	All amplifiers disabled, $\overline{SHDN}$ = V–, T_A = –40°C to 125°C				1.5	µA
Z_{OUT_SHDN}	Output impedance during shutdown (8)	Amplifier disabled			43 || 11.5		GΩ || pF
V_{SHDN_IH}	Logic high threshold voltage (amplifier enabled) (8)			(V–) + 1.2			V
V_{SHDN_IL}	Logic low threshold voltage (amplifier disabled) (8)					(V–) + 0.2	V

7.7 Electrical Characteristics (continued)

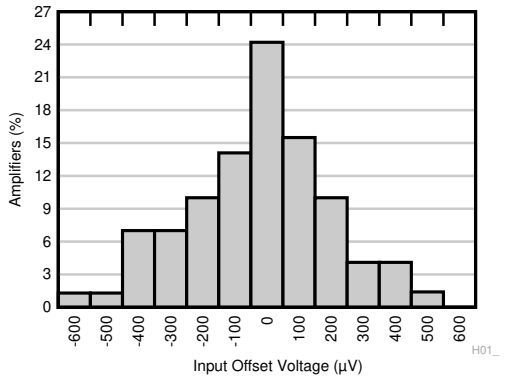
For V_S = (V+) – (V–) = 1.5 V to 5.5 V (±0.75 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Amplifier enable time (full shutdown) (7) (8)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–		1		µs
t_{OFF}	Amplifier disable time (7) (8)	G = +1, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–		1		µs
I_{B_SHDN}	$\overline{SHDN}$ pin input bias current (per pin) (8)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V		50		nA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V		100		

(1) Max data is specified based on characterization results.
(2) Min data is specified based on characterization results.
(3) Typical input current noise data is specified based on design simulation results.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.
(5) Short circuit current specified here is the average of sourcing and sinking short circuit currents.
(6) A_{OL} is measured as the difference between (V_{OSA} – V_{OSB}) / (V_{OUTA} – V_{OUTB}). V_{OSA} is the offset measured when the OUT pin is biased at (V+) - 0.25 V while the device sources 50 mA and VOSB is the offset measured when the OUT pin is biased at (V–) + 0.25 V while the device sinks 50 mA.
(7) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(8) Shutdown section is on preview.

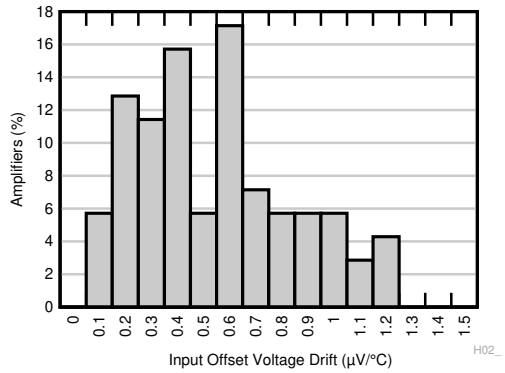
7.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



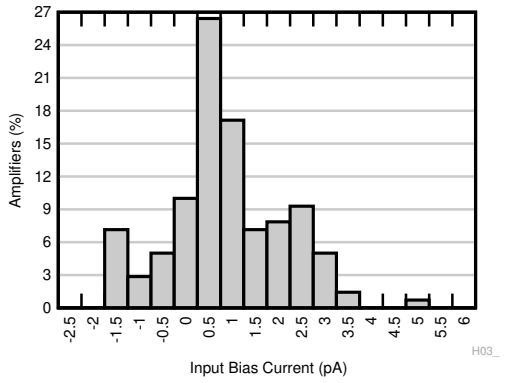
V_S = 5.5 V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 70 Mean = –36 µV Sigma = 215 µV

Figure 7-1. Offset Voltage Distribution Histogram



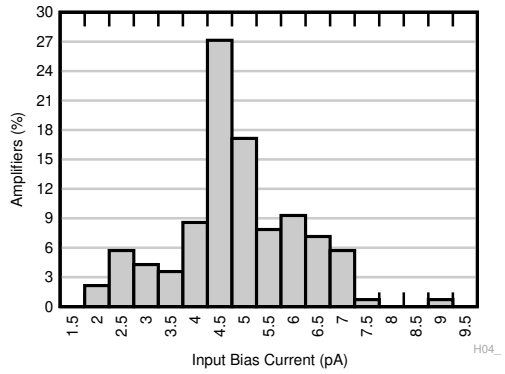
V_S = 5.5 V V_{CM} = V_S / 2 T_A = –40°C to +125°C
No. of devices = 70
Mean = 0.5 µV/°C Sigma = 0.3 µV/°C

Figure 7-2. Offset Voltage Drift Distribution Histogram



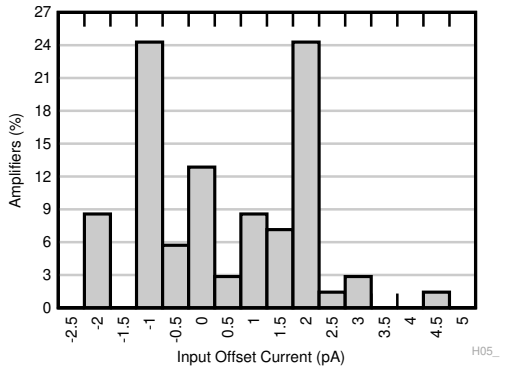
V_S = 5.5 V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 140 Mean = 0.6 pA Sigma = 1.2 pA

Figure 7-3. Input Bias Current Distribution Histogram



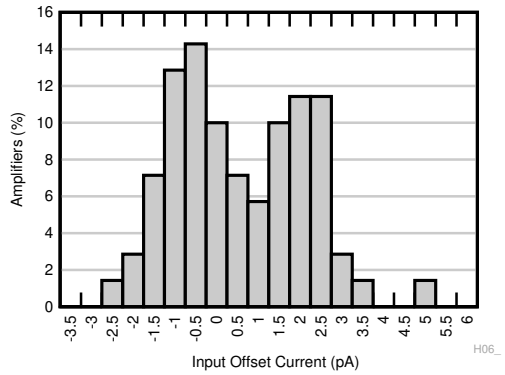
V_S = 5.5 V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 140 Mean = 4.6 pA Sigma = 1.3 pA

Figure 7-4. Input Bias Current Distribution Histogram



V_S = 5.5 V V_{CM} = V_S / 2 T_A = 25°C
No. of devices = 140 Mean = 0.2 pA Sigma = 1.5 pA

Figure 7-5. Input Offset Current Distribution Histogram

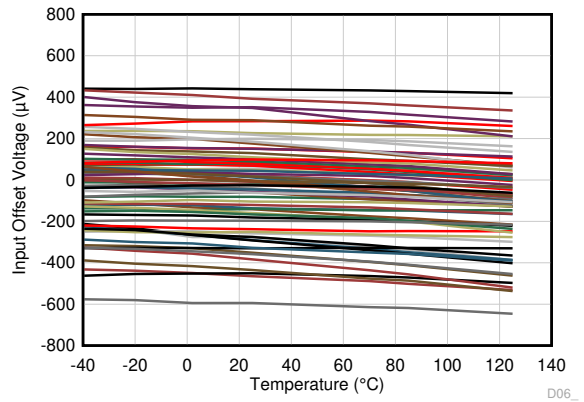


V_S = 5.5 V V_{CM} = V_S / 2 T_A = 85°C
No. of devices = 70 Mean = 0.3 pA Sigma = 1.6 pA

Figure 7-6. Input Offset Current Distribution Histogram

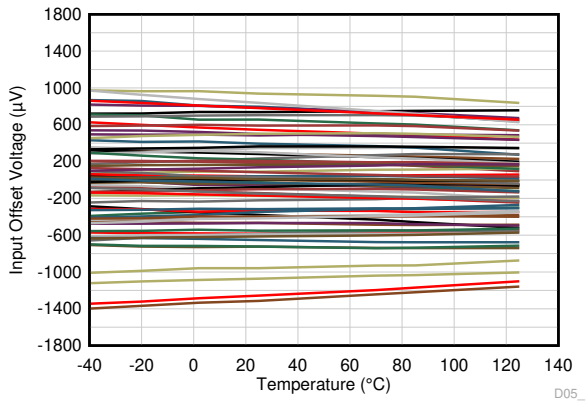
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



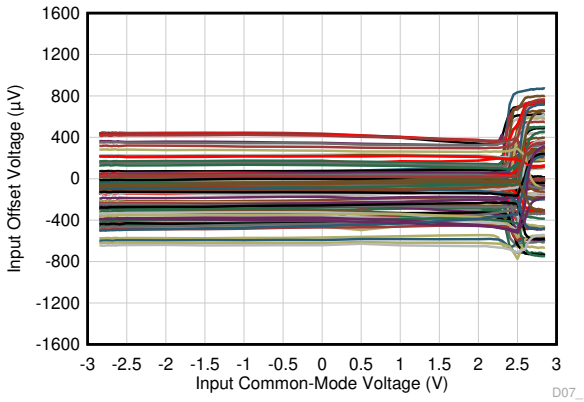
V_S = 5.5 V, V_{CM} = V– No. of devices = 72

Figure 7-7. Input Offset Voltage vs Temperature



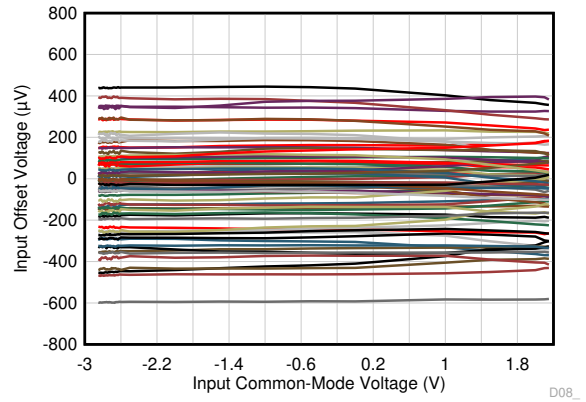
V_S = 5.5 V, V_{CM} = V+ No. of devices = 72

Figure 7-8. Input Offset Voltage vs Temperature



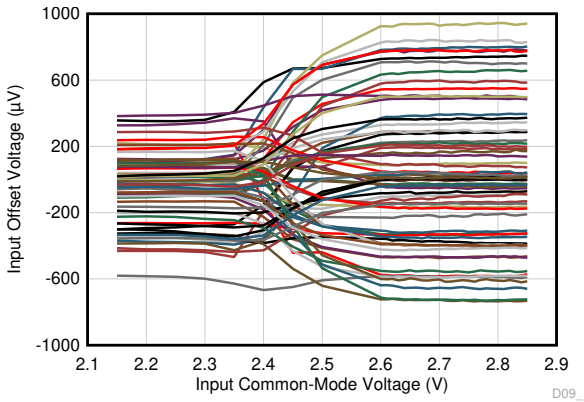
V+ = 2.75 V, V– = –2.75 V
No. of devices = 72

Figure 7-9. Offset Voltage vs Common-Mode



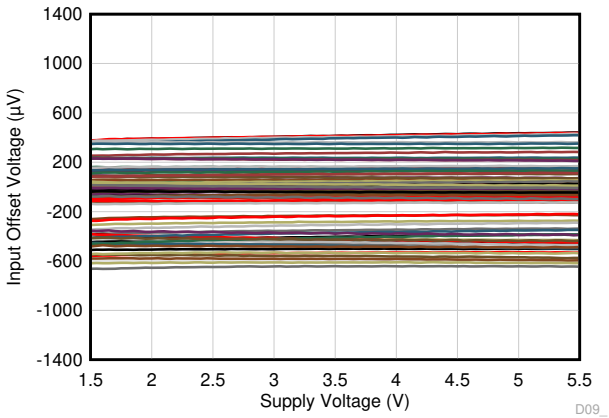
V+ = 2.75 V, V– = –2.75 V, (V–) < V_{CM} < (V+) – 0.6 V
No. of devices = 72

Figure 7-10. Offset Voltage vs Common-Mode



V+ = 2.75 V, V– = –2.75 V, V_{CM} > (V+) – 0.6 V
No. of devices = 72

Figure 7-11. Offset Voltage vs Common-Mode

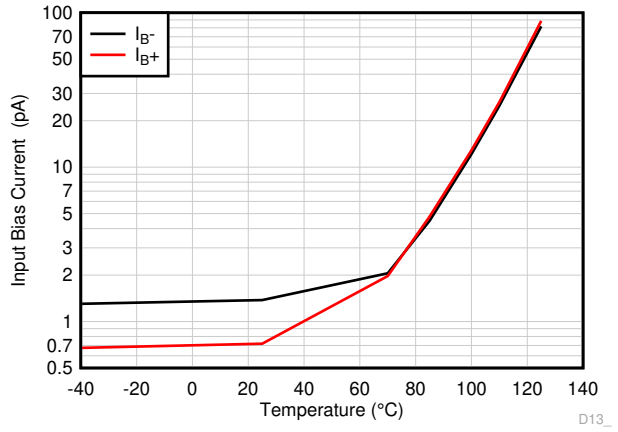


V_{CM} = (V–) No. of devices = 72

Figure 7-12. Offset Voltage vs Supply Voltage

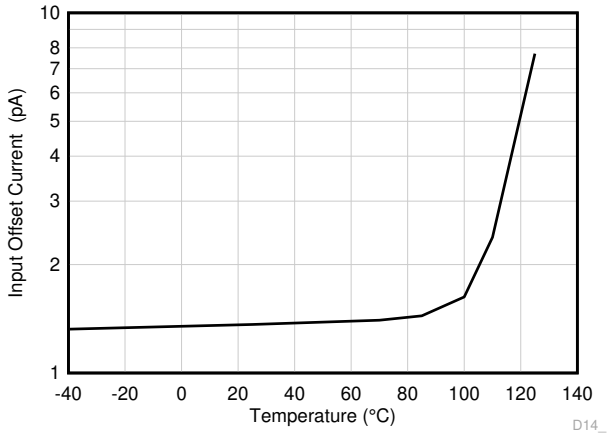
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



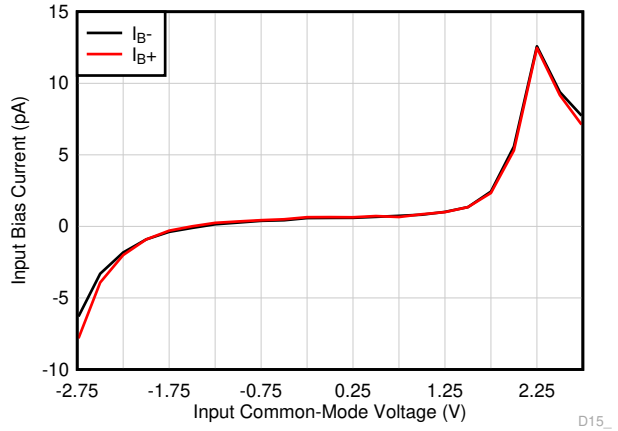
V_S = 5.5 V, V_{CM} = V_S/2

Figure 7-13. I_B vs Temperature



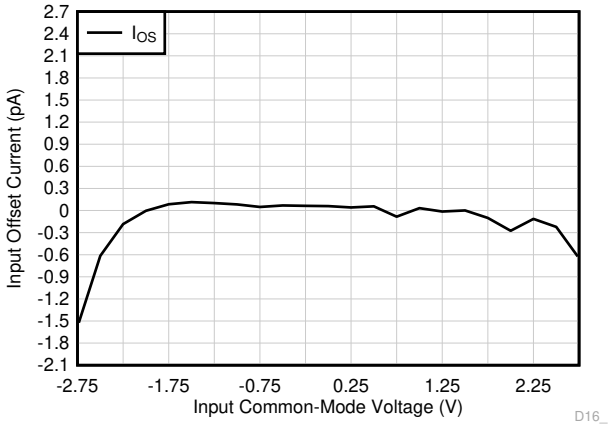
V_S = 5.5 V, V_{CM} = V_S/2

Figure 7-14. I_{OS} vs Temperature



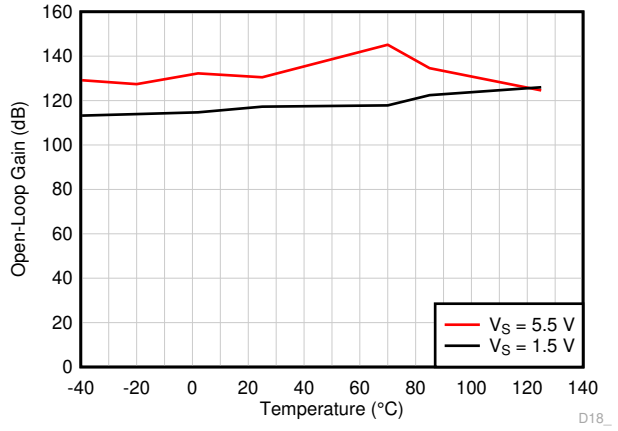
V+ = 2.75 V, V– = –2.75 V, V_{CM} = V_S/2

Figure 7-15. I_B vs Common-Mode Voltage



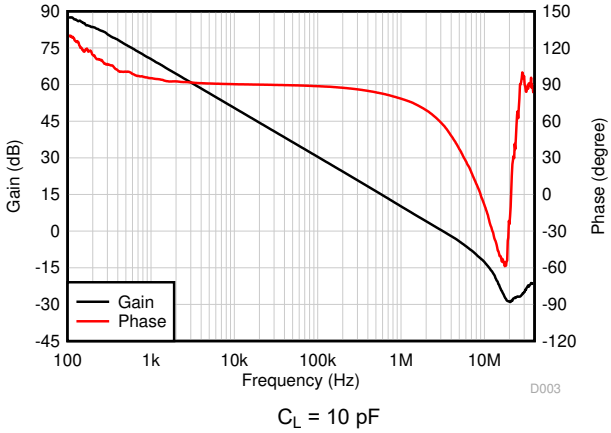
V+ = 2.75 V, V– = –2.75 V, V_{CM} = V_S/2

Figure 7-16. I_{OS} vs Common-Mode Voltage



R_L = 10 kΩ

Figure 7-17. Open-Loop Gain vs Temperature



C_L = 10 pF

Figure 7-18. Open-Loop Gain and Phase vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

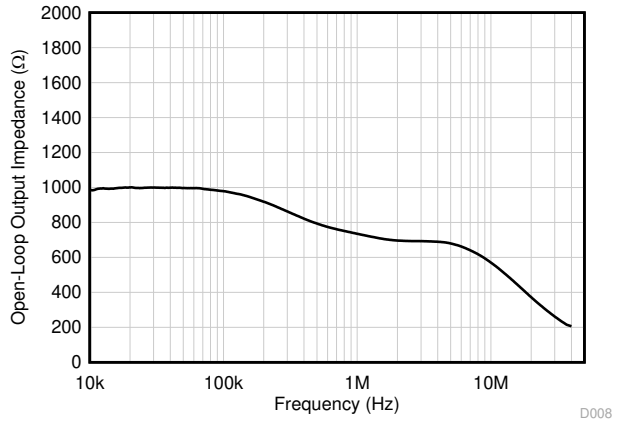
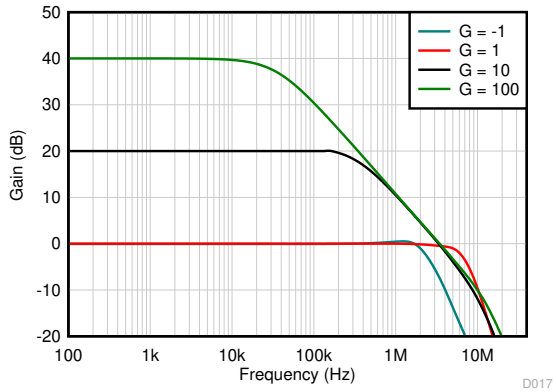
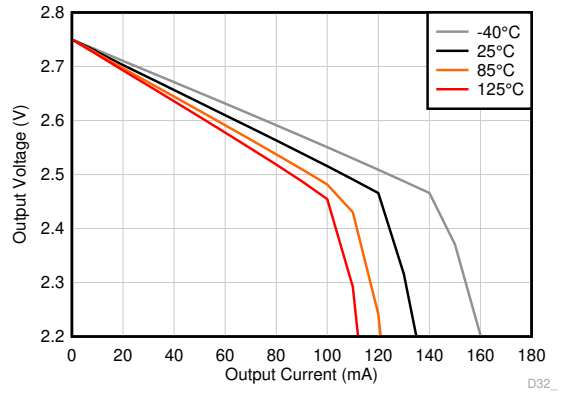


Figure 7-19. Open-Loop Output Impedance vs Frequency



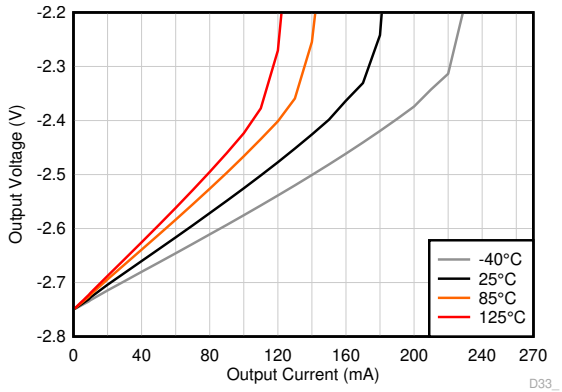
C_L = 10 pF

Figure 7-20. Closed-Loop Gain vs Frequency



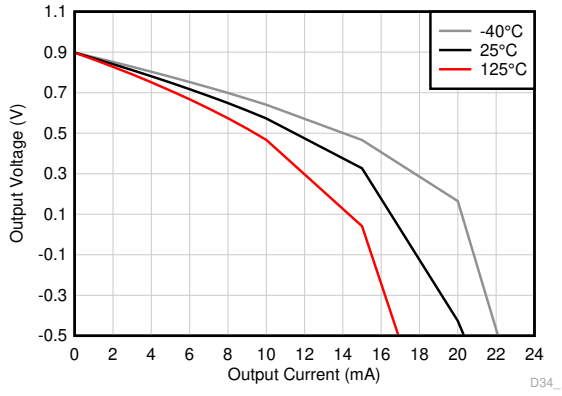
V+ = 2.75 V, V– = –2.75 V

Figure 7-21. Output Voltage Swing vs Output Current (Sourcing)



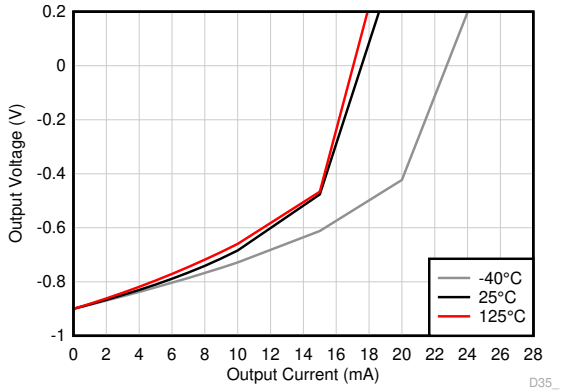
V+ = 2.75 V, V– = –2.75 V

Figure 7-22. Output Voltage Swing vs Output Current (Sinking)



V+ = 0.9 V, V– = –0.9 V

Figure 7-23. Output Voltage Swing vs Output Current (Sourcing)



V+ = 0.9 V, V– = –0.9 V

Figure 7-24. Output Voltage Swing vs Output Current (Sinking)

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

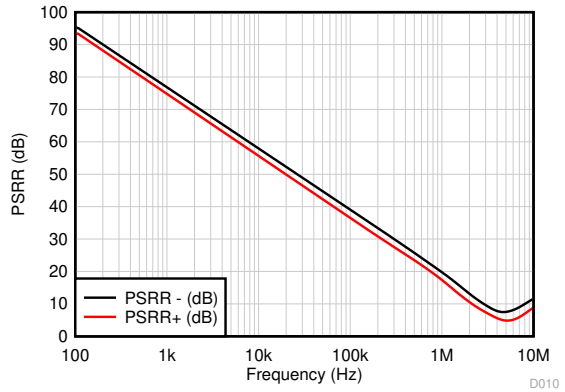
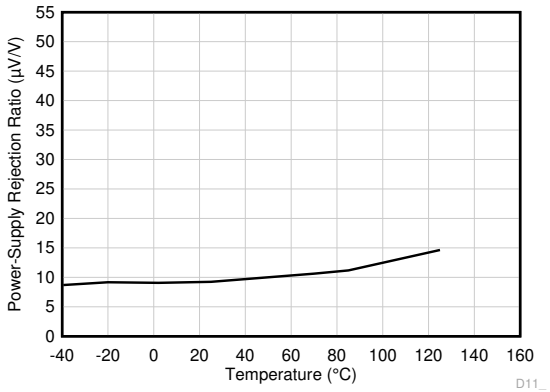


Figure 7-25. PSRR vs Frequency



V_S = 1.5 V to 5.5 V

Figure 7-26. DC PSRR vs Temperature

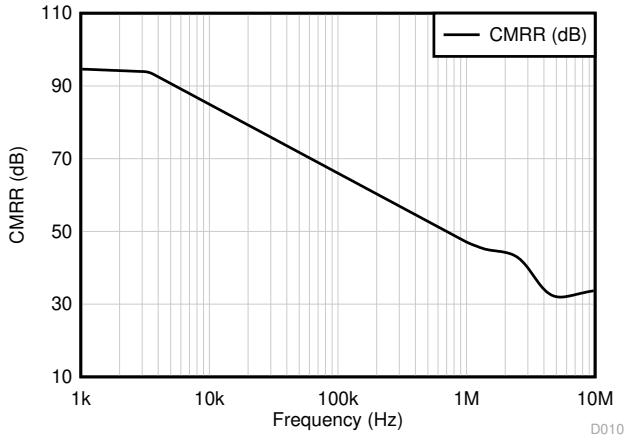
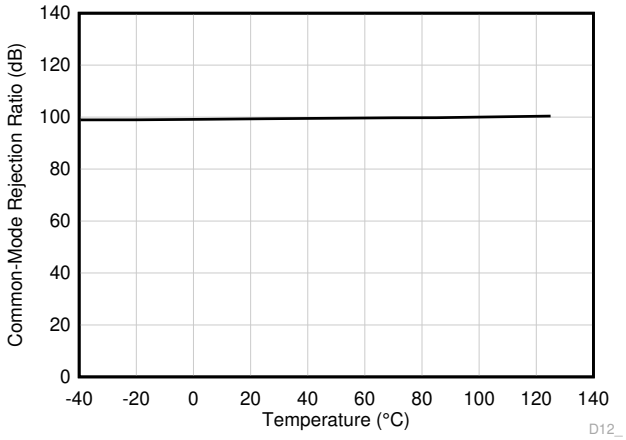


Figure 7-27. CMRR vs Frequency



V_S = 5.5 V, (V–) < V_{CM} < (V+) – 0.6 V

Figure 7-28. DC CMRR vs Temperature

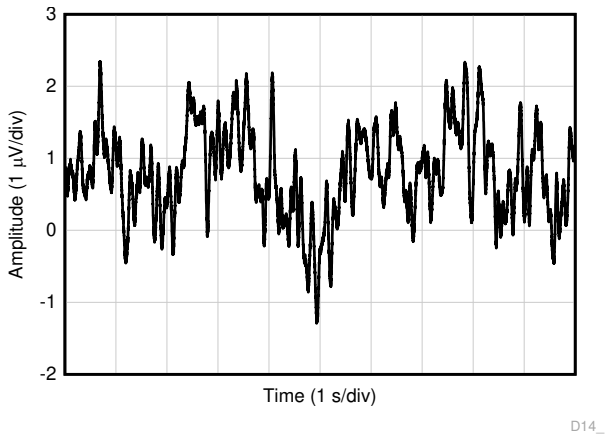


Figure 7-29. 0.1-Hz to 10-Hz Voltage Noise in Time Domain

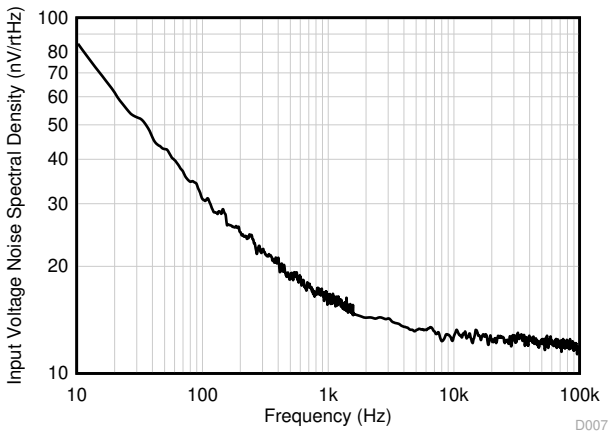
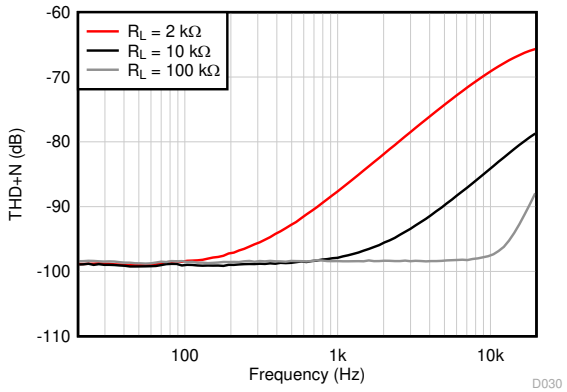


Figure 7-30. Input Voltage Noise Spectral Density

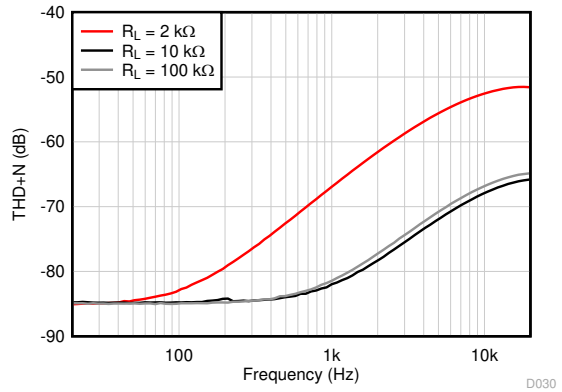
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



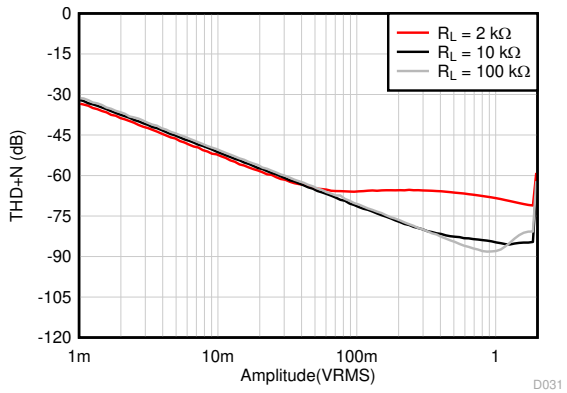
V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

Figure 7-31. THD + N vs Frequency



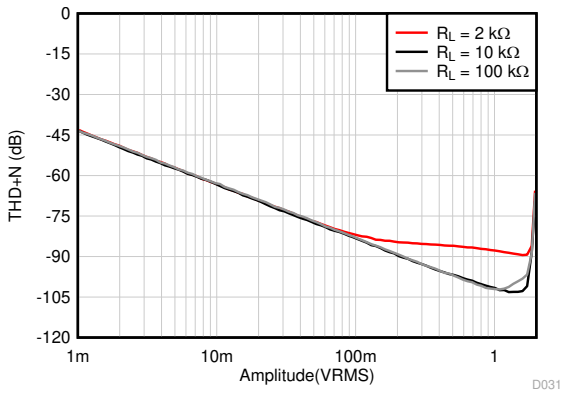
V_S = 5.5 V V_{CM} = 2.5 V G = –1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

Figure 7-32. THD + N vs Frequency



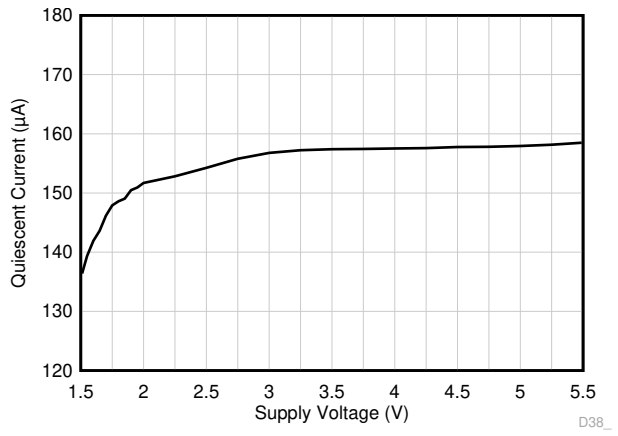
V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = 1 BW = 80 kHz

Figure 7-33. THD + N vs Amplitude



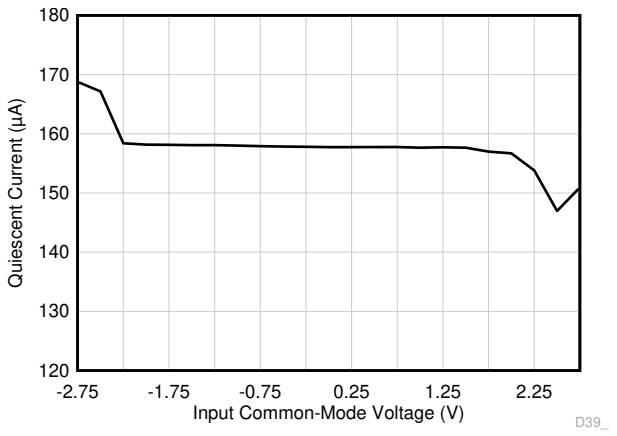
V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = –1 BW = 80 kHz

Figure 7-34. THD + N vs Amplitude



V_{CM} = V_S/2

Figure 7-35. Quiescent Current vs Supply Voltage

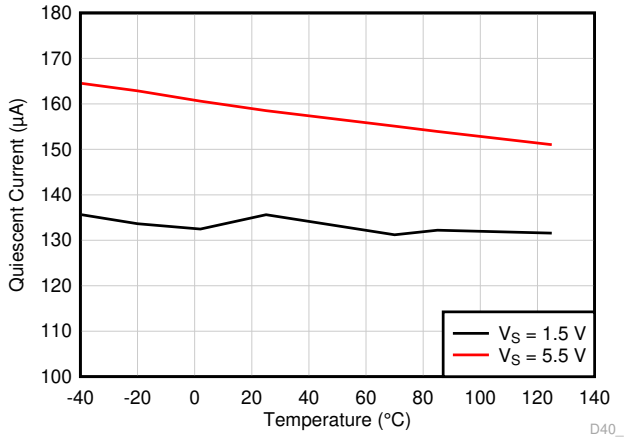


V+ = 2.75 V, V– = –2.75 V

Figure 7-36. Quiescent Current vs Common-Mode Voltage

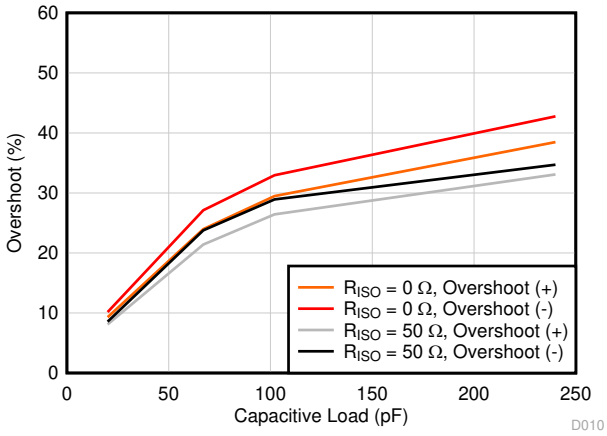
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



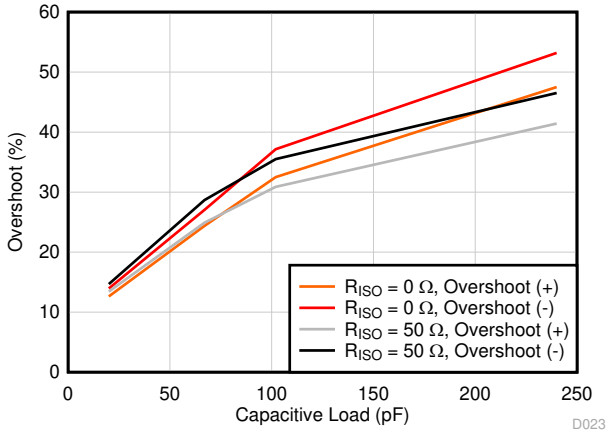
V_{CM} = V_S/2

Figure 7-37. Quiescent Current vs Temperature



G = –1 V_{IN} = 100 mVpp

Figure 7-38. Small Signal Overshoot vs Capacitive Load



G = 1 V_{IN} = 100 mVpp

Figure 7-39. Small Signal Overshoot vs Capacitive Load

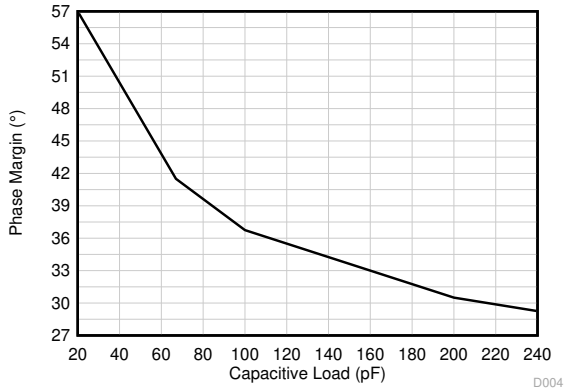
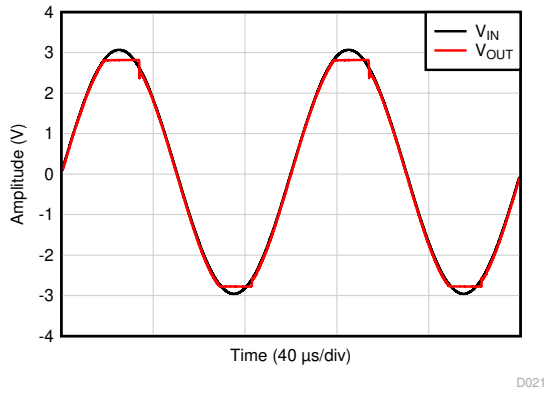
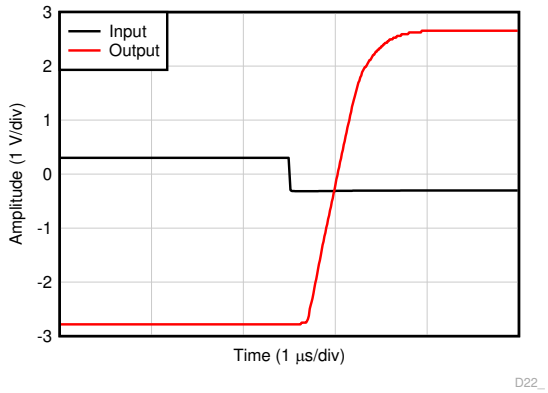


Figure 7-40. Phase Margin vs Capacitive Load



G = 1 V_{IN} = 6 V_{PP}

Figure 7-41. No Phase Reversal

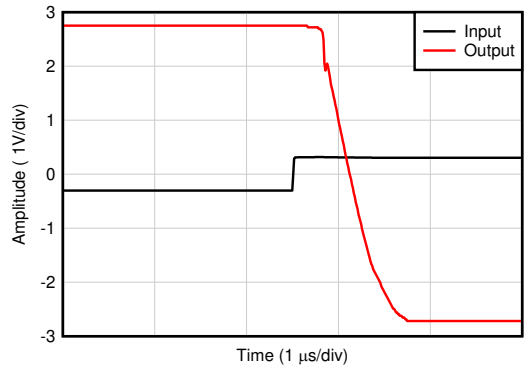


G = –10 V_{IN} = 600 mV_{PP}

Figure 7-42. Overload Recovery

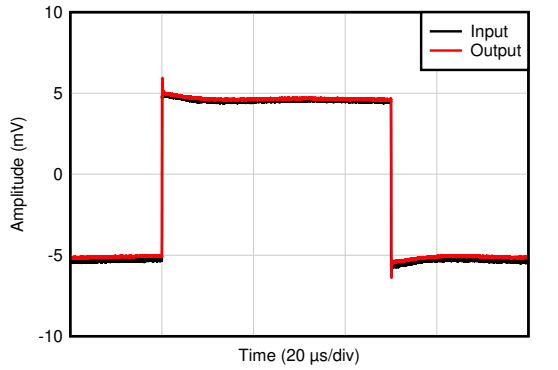
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



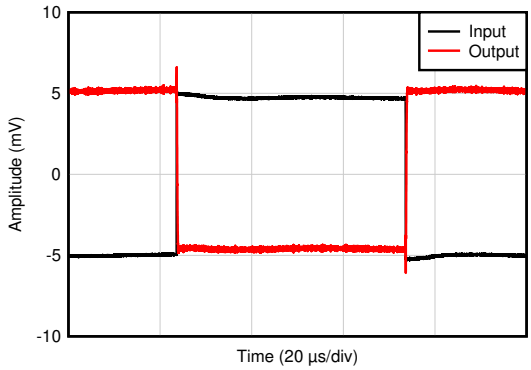
G = –10 V_{IN} = 600 mV_{PP}

Figure 7-43. Overload Recovery



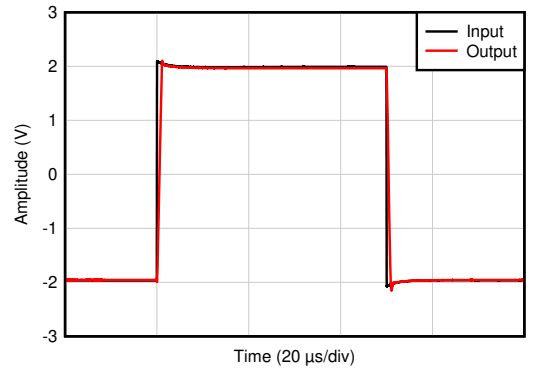
G = 1 V_{IN} = 10 mV_{PP} C_L = 10 pF

Figure 7-44. Small-Signal Step Response



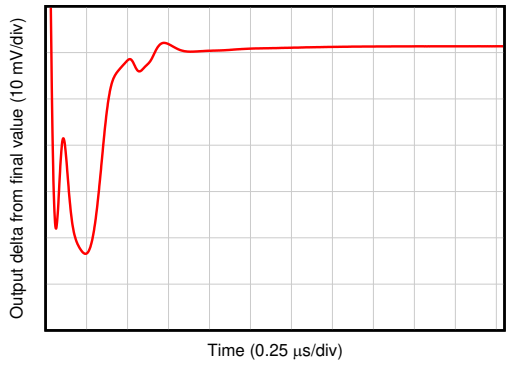
G = –1 V_{IN} = 10 mV_{PP} C_L = 10 pF

Figure 7-45. Small-Signal Step Response



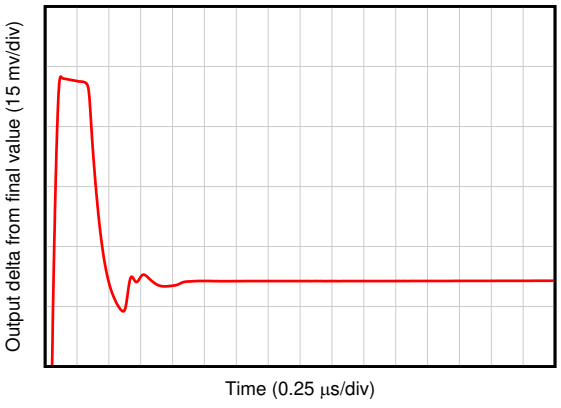
G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 7-46. Large-Signal Step Response



G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 7-47. Large-Signal Settling Time (Negative)

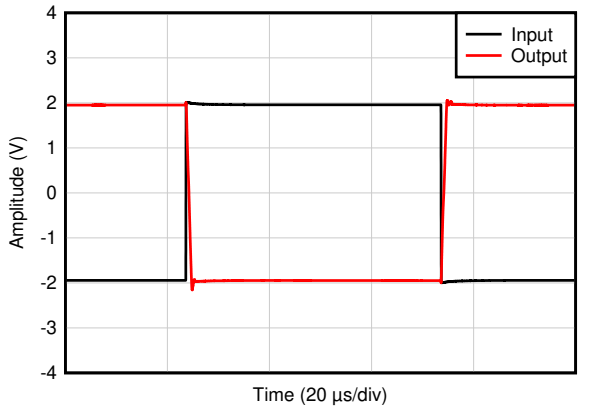


G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 7-48. Large-Signal Settling Time (Positive)

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 7-49. Large-Signal Step Response

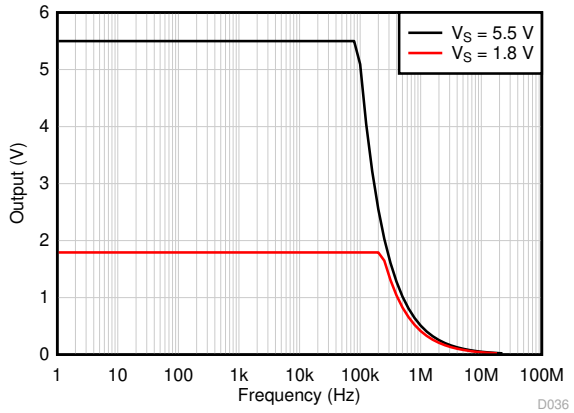
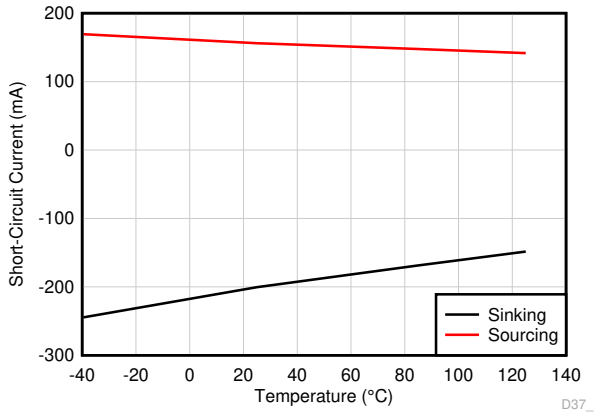


Figure 7-50. Maximum Output Voltage vs Frequency



V_S = 5.5 V

Figure 7-51. Short-Circuit Current vs Temperature

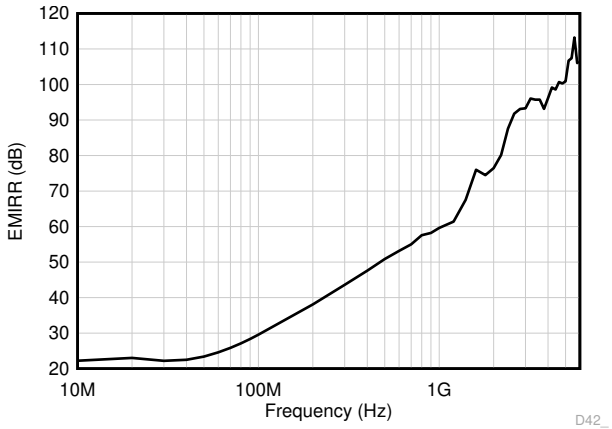


Figure 7-52. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

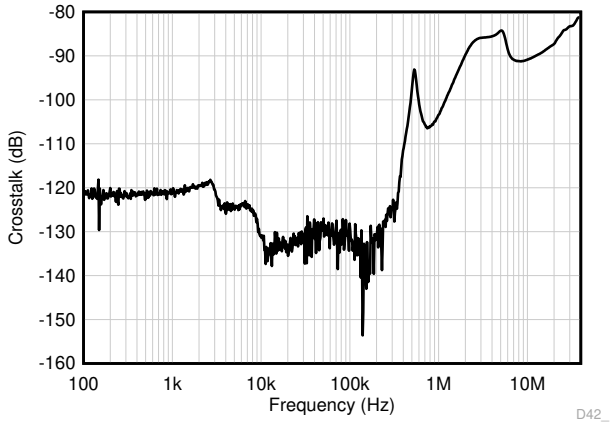


Figure 7-53. Channel Separation

8 Detailed Description

8.1 Overview

The OPAx310 family of op amps includes single (OPA310), dual (OPA2310), and quad-channel (OPA4310), ultra-low-voltage (1.5 V to 5.5 V), high output current operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. The OPAx310 also features a very fast shutdown response and has an enable, disable time specification of just 1-µs typical. This feature allows for power savings when the application involves duty cycling the amplifier signal chain. OPAx310 has robust ESD performance with fail safe input ESD structure where there are no diodes connected from inputs to the positive power supply rail.

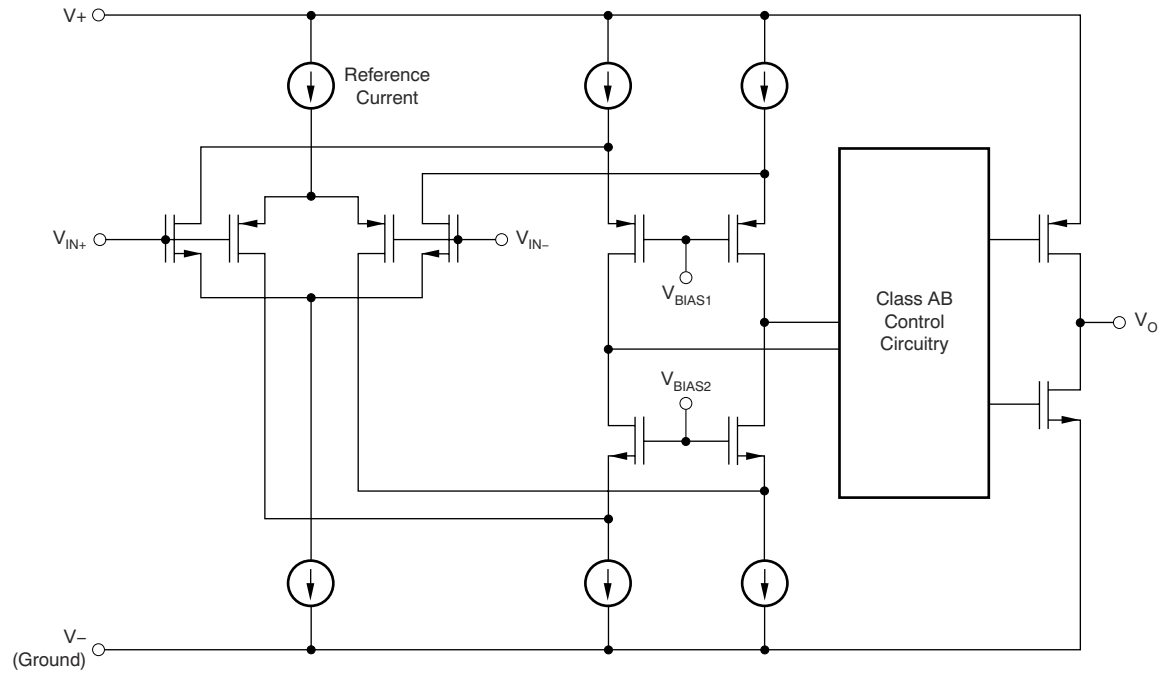
OPAx310 is offered in power pad, standard, small size packages and has an internal current limit, thermal shutdown protection that enables additional robustness when operating with high output current. OPAx310 can swing very close to the rails and has a short circuit current of ±75-mA minimum across temperature at 5.5-V power supply while consuming just 165 µA of quiescent current. This combination of low voltage, low I_Q, and high output current capability makes this device quite unique and suitable for suitable for a wide range of general-purpose and high current applications. Additional output current capability can be easily achieved by connecting multiple op amps in parallel. These devices are excellent choice for LED driver, LCD driver, Laser driver, TEC driver applications and can also be used as a reference buffer, guard amplifier or as a discrete LDO.

The input common-mode voltage range includes both rails, and allows the OPAx310 series to be used in many single-supply or dual supply configurations. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices ideal for driving low speed sampling analog-to-digital converters (ADCs). Further, the class AB output stage is capable of driving smaller resistive loads connected to any point between V+ and ground.

The OPAx310 can drive up to 75 pF with a typical phase margin of 40° and features 3 MHz gain bandwidth product, 3 V/µs slew rate with 4 μV_{p-p} integrated noise (0.1 Hz to 10 Hz) while consuming only 165 µA supply current per channel, thus providing a good AC performance at a very low power consumption. DC applications are also well served with a low input bias current (1 pA typical), a good input offset voltage (0.25 mV typical) and a good PSRR (10 µV/V typical), CMRR (80 dB typical), and A_{OL} (125 dB typical).

The robust design of the OPAx310 family simplifies circuit design. These op amps feature an integrated radio frequency immunity (RFI) and electro-magnetic interfernce (EMI) rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAx310 series of operational amplifiers is fully specified from 1.8 V to 5.5 V and ensured for amplifier operation from 1.5 V to 1.8 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics*. TI highly recommends to bypass power-supply pins with at least 0.01-µF ceramic capacitors.

8.3.2 Rail-to-Rail Input

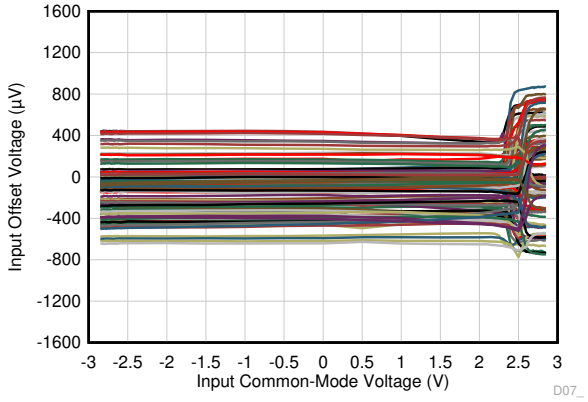
The input common-mode voltage range of the OPAx310 series extends to either supply rails. This is true even when operating at the ultra-low supply voltage of 1.5 V, all the way up to the standard supply voltage of 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to the *Functional Block Diagram* for more details.

For most amplifiers with a complementary input stage, one of the input pairs, usually the P-channel input pair, is designed to deliver slightly better performance in terms of input offset voltage, offset drift over the N-channel pair. Consequently, the P-channel pair is designed to cover the majority of the common mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. Just after the threshold voltage, both the input pairs are in operation for a small range referred to as the transition region. Beyond this region, the N-channel pair completely takes over. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. Hence, most applications generally prefer operating in the P-channel input range where the performance is slightly better.

For the OPAx310, the P-channel pair is typically active for input voltages from (V–) to (V+) – 0.4 V and the N-channel pair is typically active for input voltages from the positive supply to (V+) – 0.4 V. The transition region occurs typically from (V+) – 0.5 V to (V+) – 0.3 V, in which both pairs are on. These voltage levels mentioned above can vary with process variations associated with threshold voltage of transistors. In the OPAx310, 200-mV transition region mentioned above can vary up to 200 mV in either direction. Thus, the transition region (both stages on) can range from (V+) – 0.7 V to (V+) – 0.5 V on the low end, up to (V+) – 0.3 V to (V+) – 0.1 V on the high end.

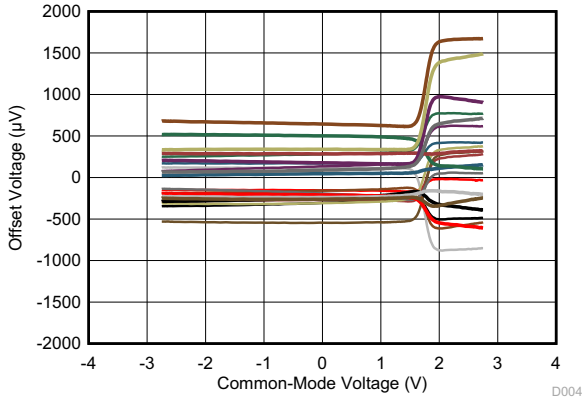
Recollecting the fact that a P-channel input pair usually offers better performance over a N-channel input pair, the OPAx310 is designed to offer a much wider P-channel input pair range, in comparison to most complimentary input amplifiers in the industry. A side-by-side comparison of the OPAx310 and the TLV900x is provided below. Note that the TLV900x assures P-channel pair operation only until 1.4 V from the positive rail while the OPAx310 assures P-channel pair operation all the way till 0.7 V from the positive rail. This additional 700 mV of P-channel input pair range for the OPAx310 is particularly useful when operating at lower supply voltages (1.5 V, 1.8 V, and so forth) where the P-channel input range usually gets limited to a great extent.

Thus the wide common mode swing of input signal can be accommodated more easily within the P-channel input pair of the OPAx310, while likely avoiding the transition region, thereby maintaining linearity.



V+ = 2.75 V, V– = –2.75 V

Figure 8-1. OPAx310 Offset Voltage vs Common-Mode



V+ = 2.75 V, V– = –2.75 V

Figure 8-2. TLV900x Offset Voltage vs Common-Mode

8.3.3 Rail-to-Rail Output

Designed as a micro-power, high output current operational amplifier, the OPAx310 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. At room temperature and for resistive loads up to 2 kΩ, the output swings to within a maximum of 20 mV of either supply rail at 5.5 V power supply. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 Capacitive Load and Stability

The OPAx310 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the OPAx310 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the OPAx310 remains stable with a pure capacitive load up to approximately 75 pF with a good phase margin of 40° typical and has no sustained oscillations up to 250 pF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in Figure 8-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

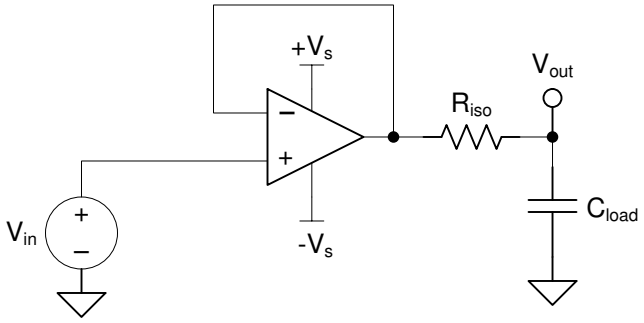


Figure 8-3. Improving Capacitive Load Drive

8.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to its linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time.

The overload recovery time for the OPAx310 family is approximately 0.75-µs typical.

8.3.6 EMI Rejection

The OPAx310 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx310 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-4 shows the results of this testing on the OPAx310. Table 8-1 shows the EMIRR IN+ values for the OPAx310 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

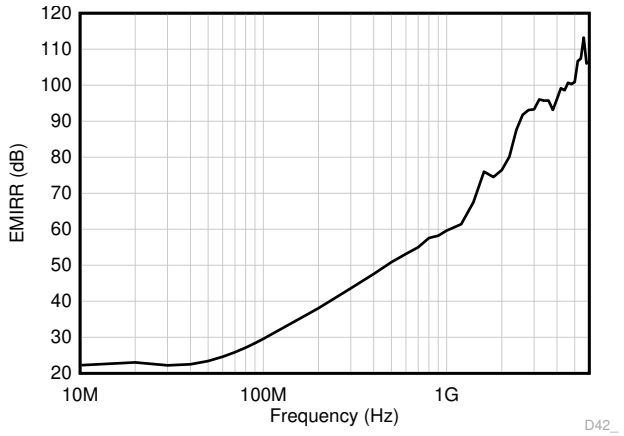


Figure 8-4. EMIRR Testing

Table 8-1. OPAx310 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	75 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	90 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	95 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	102 dB

8.3.7 ESD and Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-5 shows the ESD circuits contained in the OPAx310 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Note that the OPAx310 features no current-steering diodes connected between the input and positive power-supply pin.

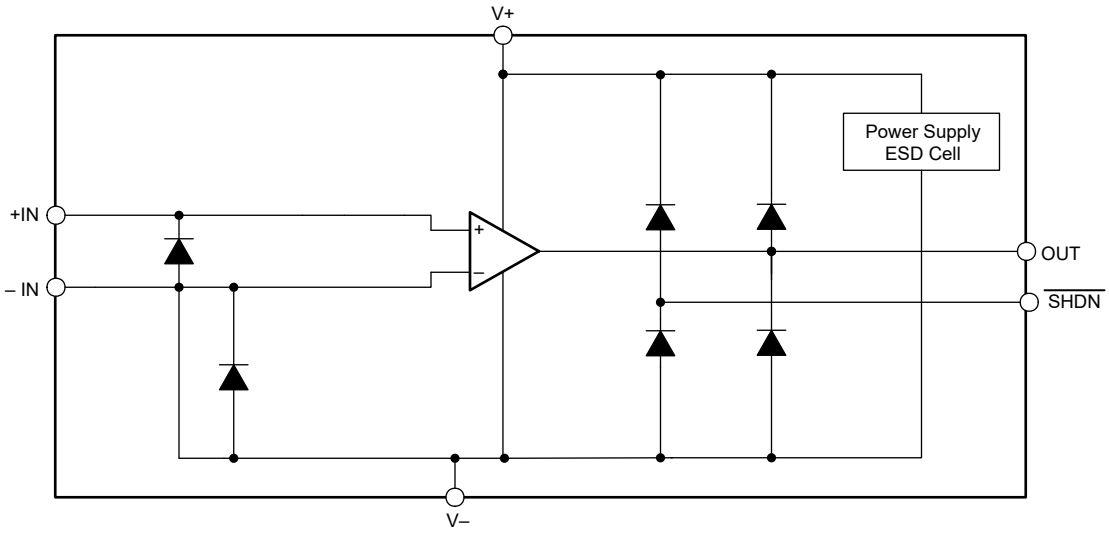


Figure 8-5. Equivalent Internal ESD Circuitry

8.3.8 Input ESD Protection

The OPAx310 family incorporates internal ESD protection circuits on all pins. For inputs, this protection primarily consists of fail safe ESD input structures which feature no current-steering diodes connected between the input and positive power-supply pin as shown in the Figure 8-5. This feature is very useful during power sequencing scenarios where input signal can be present before the positive power supply rail. A fail safe input ESD structure prevents any short between inputs and positive power supply.

8.3.9 Shutdown Function

The OPAx310 S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 500 nA at room temperature. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and (V–) + 0.2 V. A valid logic high is defined as a voltage between (V–) + 1.2 V and V+. To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. We highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level damages the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable and disable time is targeted to be under 1 µs for full shutdown of all channels. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx310S to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10 kΩ load to midsupply (V_S / 2) is required.

8.3.10 Packages with an Exposed Thermal Pad

The OPAx310 family is available in packages such as the WQFN-16 (RTE), which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must be connected to (V–). Attaching the thermal pad to a potential other then (V–) is not allowed, and the performance of the device is not assured when doing so.

8.4 Device Functional Modes

The OPAx310 devices have one functional mode. These devices are powered on as long as the power-supply voltage is between 1.5 V (±0.75 V) and 5.5 V (±2.75 V).

The OPAx310S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See *Shutdown Function* for more information.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx310 family of rail-to-rail input and output operational amplifiers is specifically designed for high output current applications. The devices operate from 1.5 V to 5.5 V, are unity-gain stable, and are also suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving small resistive loads connected to any point between V+ and V– as long as the device is not forced into short circuit mode or thermal shutdown mode. The input common-mode voltage range includes both rails and allows the OPAx310 series to be used in many single-supply or dual supply configurations.

9.2 Typical Application

9.2.1 OPAx310 Low-Side, Current Sensing Application

Figure 9-1 shows the OPAx310 configured in a low-side current sensing application.

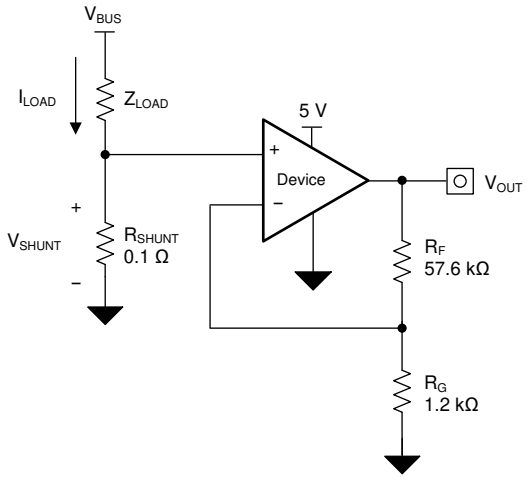


Figure 9-1. OPAx310 in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Maximum output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 9-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using Equation 2 .

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPAx310 to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the OPAx310 to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the OPAx310 to 49 V/V.

$$Gain = 1 + \frac{R_F}{R_G} \quad (4)$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. Figure 9-2 shows the measured transfer function of the circuit shown in Figure 9-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; choose an impedance that is ideal for the system parameters.

9.2.1.3 Application Curve

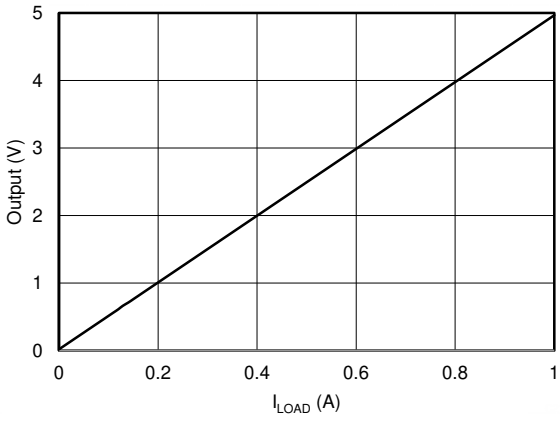


Figure 9-2. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The OPAx310 family is specified for operation from 1.5 V to 5.5 V (±0.75 V to ±2.75 V); many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

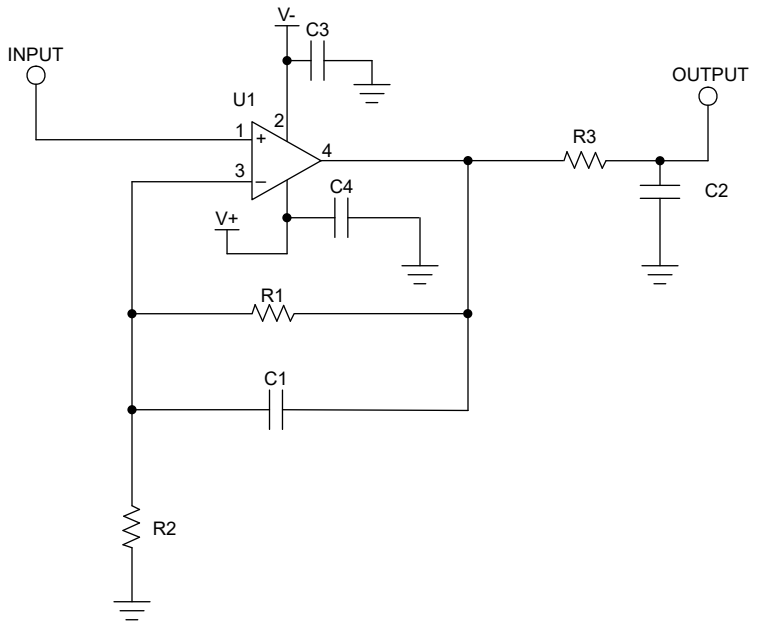


Figure 11-1. Schematic for Noninverting Configuration Layout Example

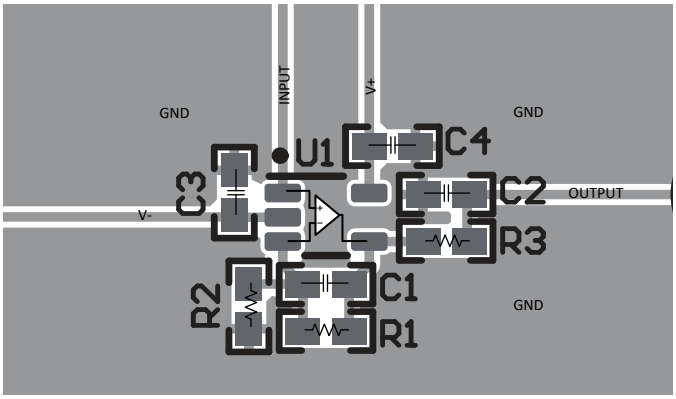


Figure 11-2. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2310IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	O231	Samples
OPA2310IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2310D	Samples
OPA2310IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O23G	Samples
POPA2310IDGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2310IDR	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
POPA2310IDSGR	ACTIVE	WSON	DSG	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

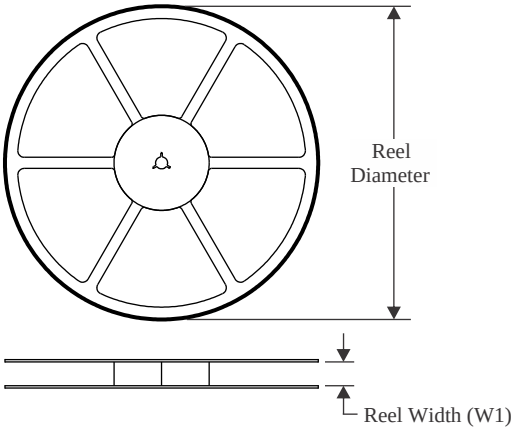
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

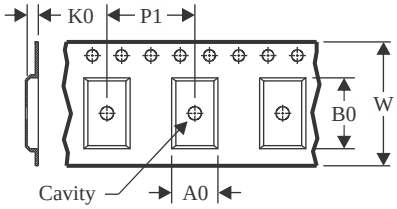
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

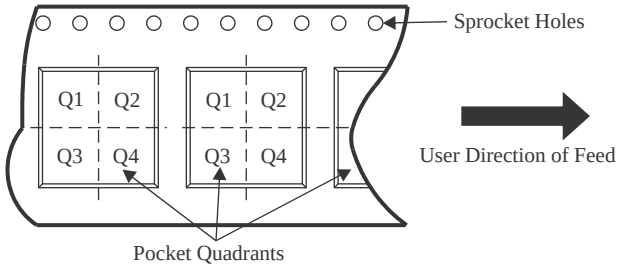


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

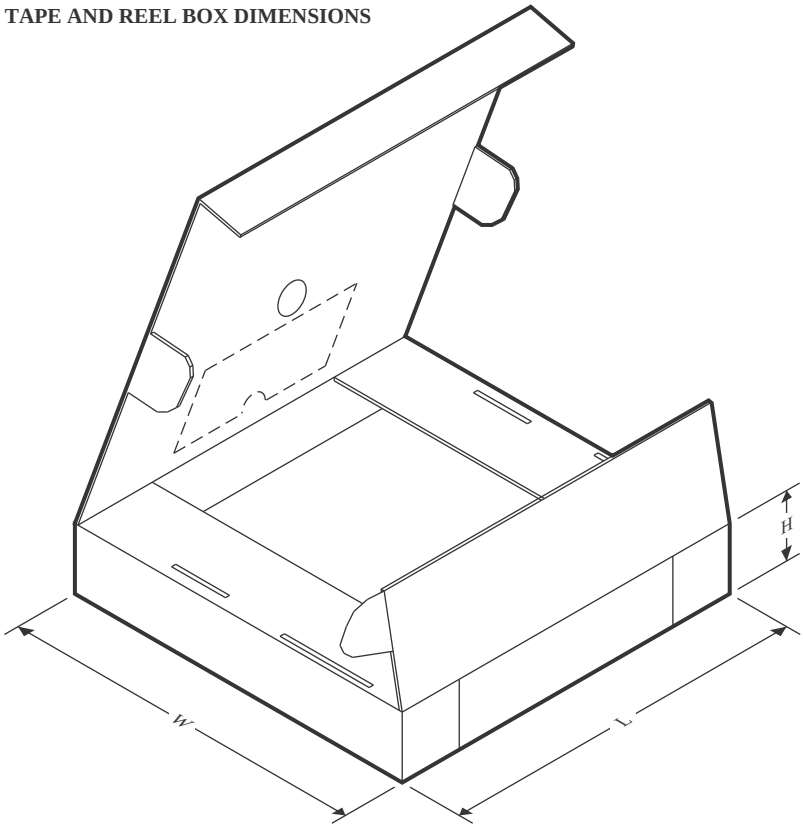
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

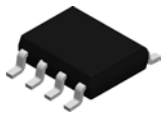
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2310IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2310IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2310IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2310IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2310IDR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2310IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0

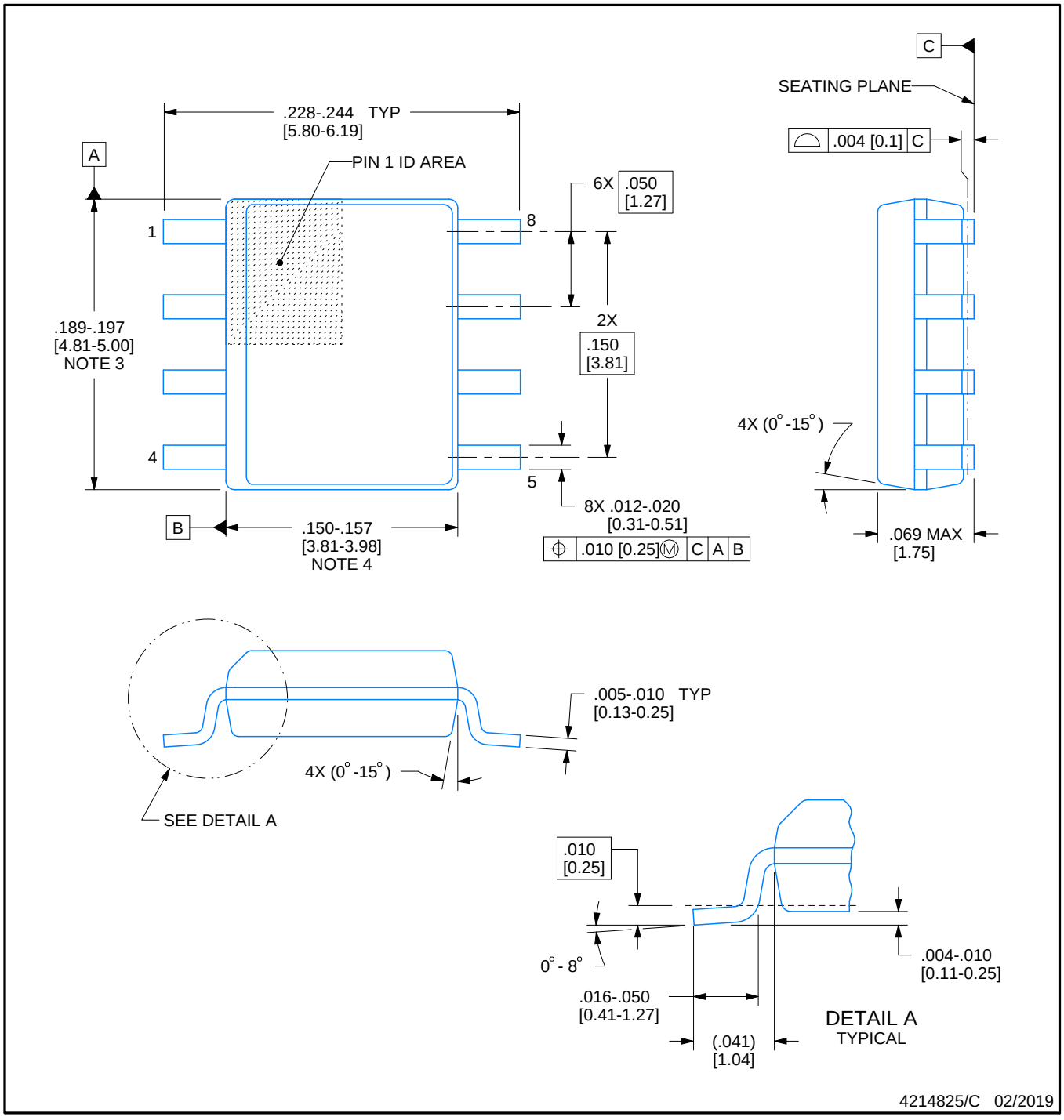


PACKAGE OUTLINE

D0008A

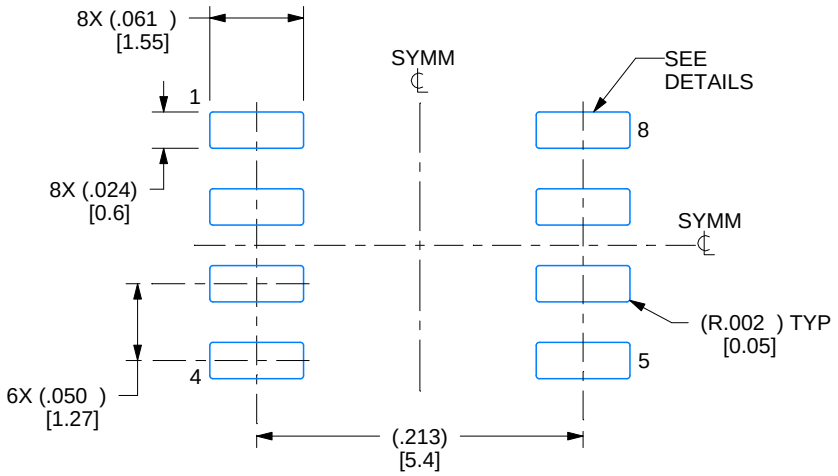
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

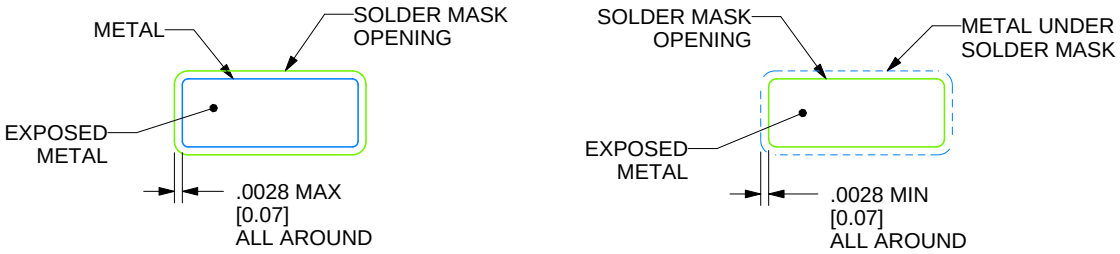


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

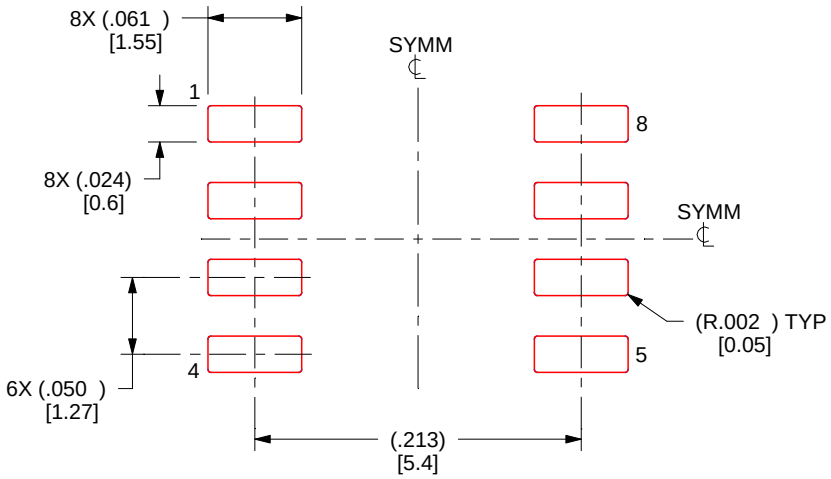
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



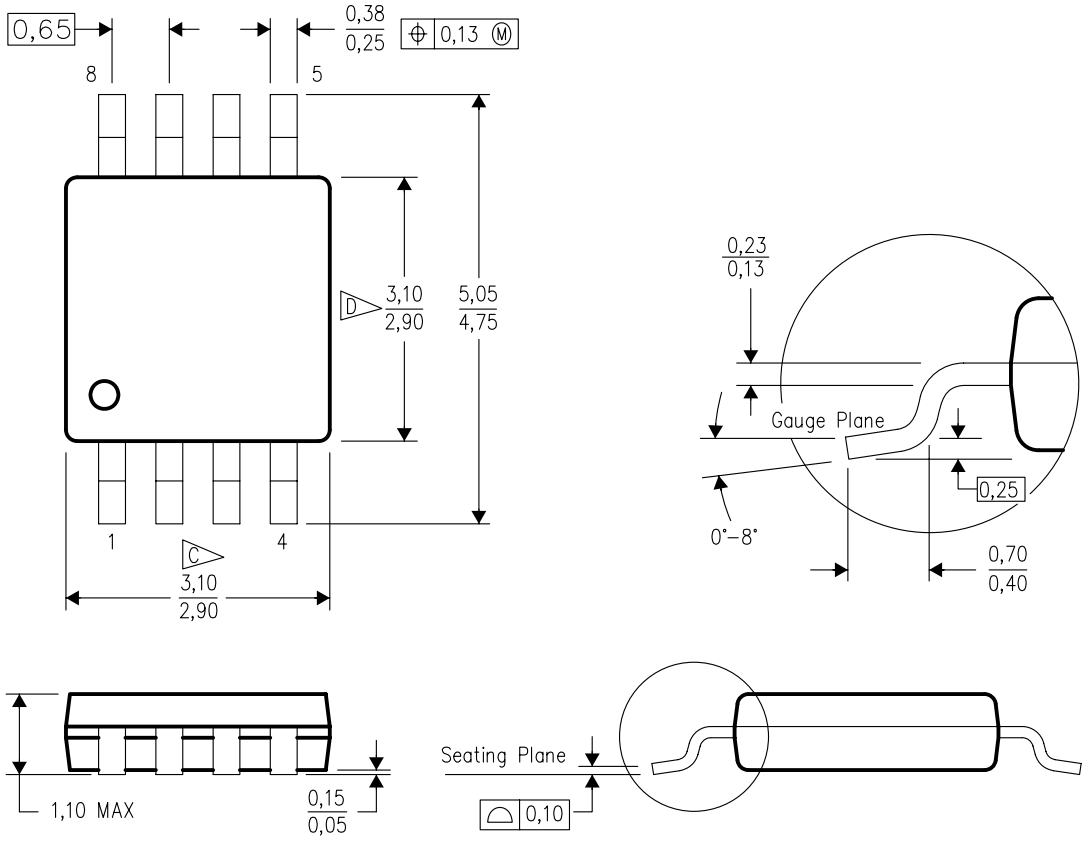
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

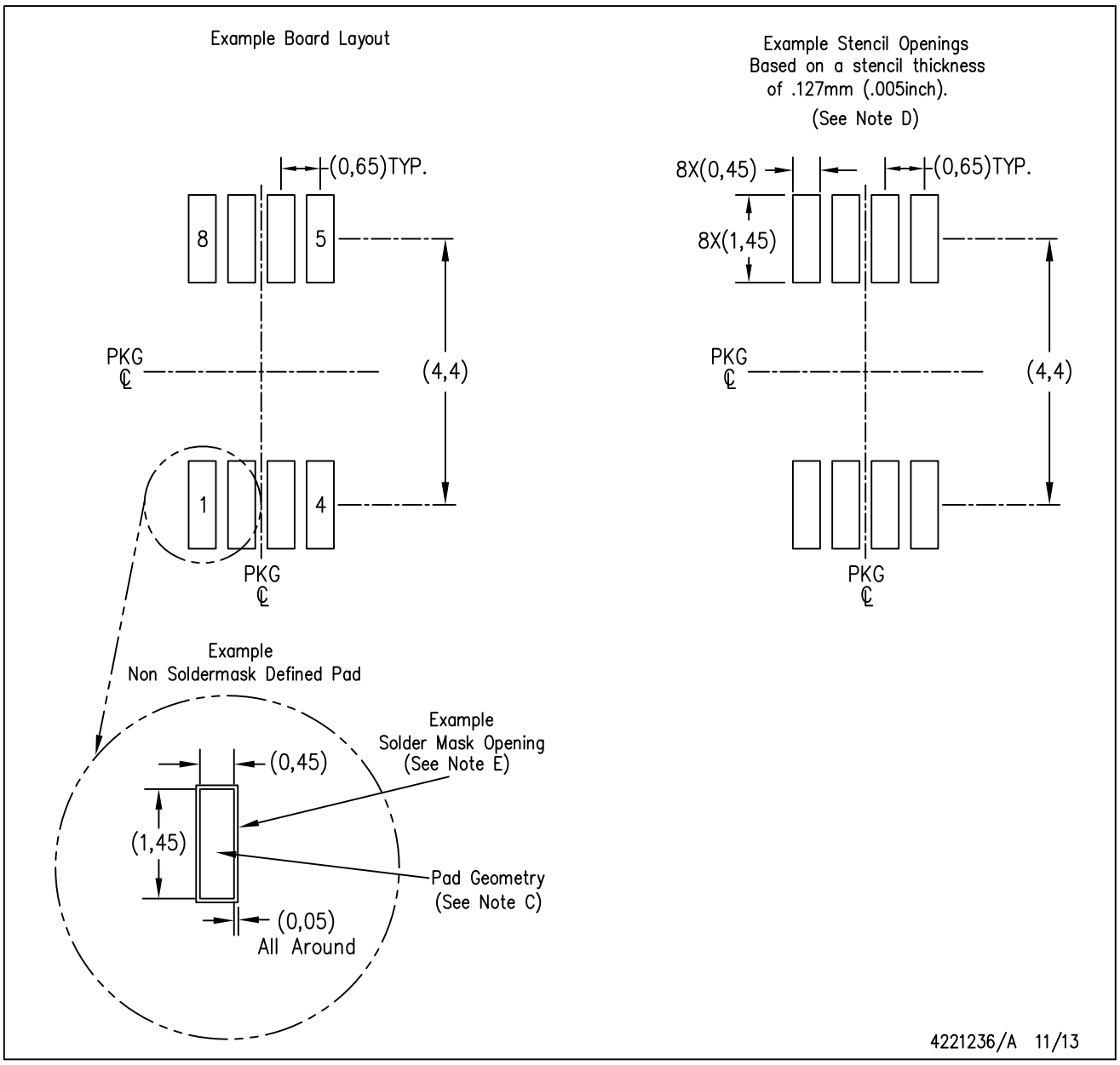
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

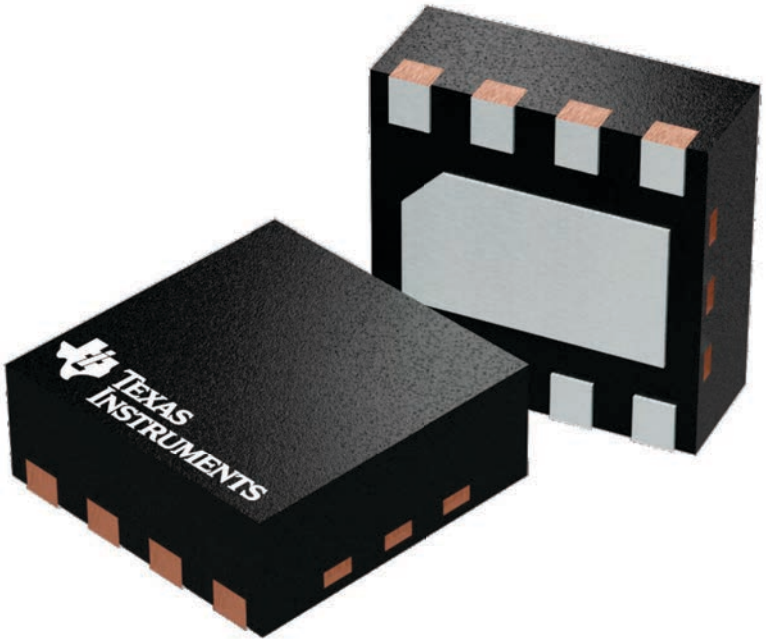
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



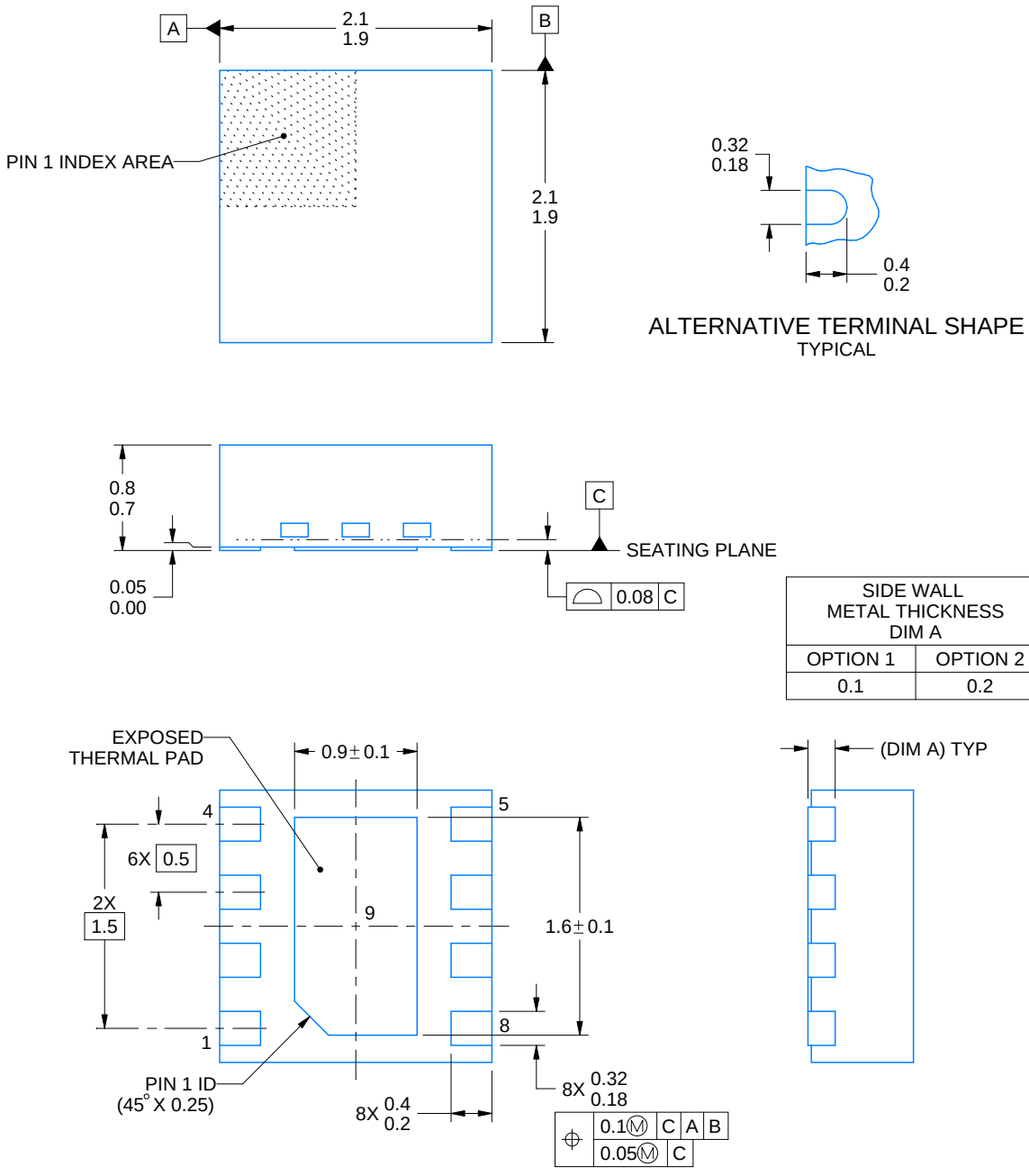
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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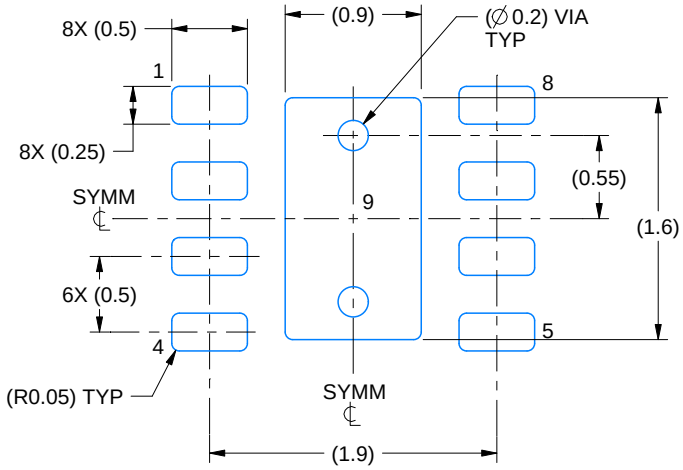
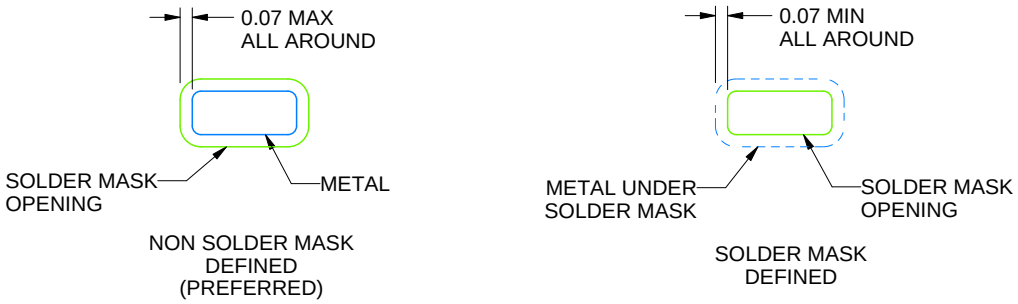
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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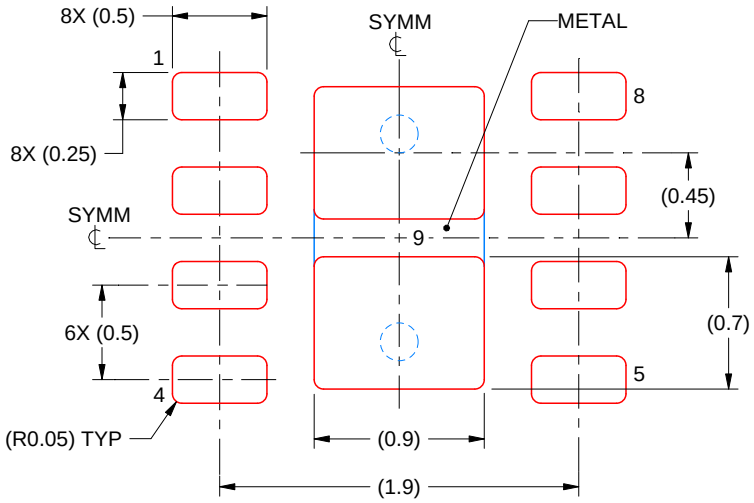
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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