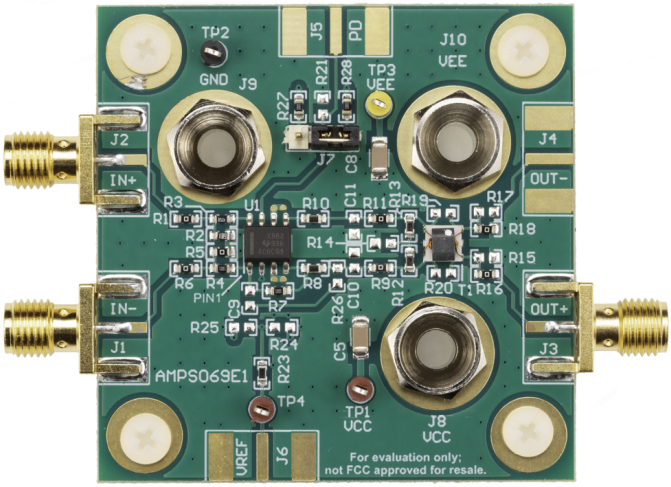
OPA862D Evaluation Module



This user's guide describes the characteristics, operation, and use of the OPA862DEVM. This evaluation module (EVM) is an evaluation and development kit for evaluating the OPA862ID, a single-ended-to-differential amplifier that interfaces single-ended sources to fully-differential amplifiers (FDAs) or differential-input, analog-to-digital converters (ADCs). A complete circuit description as well as schematic diagram and bill of materials are included in this document.

Throughout this document, the abbreviation EVM and the term evaluation module are synonymous with the OPA862DEVM.

The following related documentation is available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
OPA862 data sheet	SBOS919

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Trademarks

1 Introduction

The OPA862DEVM is an evaluation module for the single OPA862 amplifier in the D package. This evaluation module is designed to quickly and easily demonstrate the functionality and versatility of the amplifier. The EVM is ready to connect to power, signal sources, and test instruments through the use of onboard connectors. The EVM comes configured for easy connection with common 50-Ω laboratory equipment on its inputs and outputs. The amplifier is configured for a single-ended input with a gain of 4 V/V to a differential output at the device pins, which is converted to single-ended via a transformer to the output. The EVM can be easily configured for other gains and for single- or split-supply operation. The OPA862DEVM has a 2-kΩ onboard load for the amplifier. The output transformer and resistor network converts this load to a 50-Ω, single-ended output.

1.1 Features

- Configured for split-supply operation and easily modified for single supply
- Default gain of 2 configuration can easily be reconfigured for other gains
- Designed for easy connection to standard 50-Ω input/output impedance test equipment
- Inputs and outputs include subminiature version A (SMA) connectors

1.2 EVM Specifications

Table 1 lists the typical performance specifications for the OPA862DEVM.

Table 1. OPA862D EVM Specifications

Specification	Typical Value Range
Split-supply voltage range	±1.5 V to ±6.3 V
Single-supply voltage range (VEE = ground)	3 V to 12.6 V
Quiescent current (no load, split supply)	3 mA to 3.3 mA
Input voltage range	VEE + 0.5 V to VCC – 1.1 V
Output voltage range (each single-ended output)	VEE + 0.15 V to VCC – 0.15 V
Linear output current	60 mA

2 Power Connections

The OPA862DEVM is equipped with banana jacks for easy connection of power. The positive supply input is red and is labeled VCC. The negative supply input is green and is labeled VEE. Ground is black and is labeled GND.

2.1 Split-Supply Operation

To operate as split supply, apply the positive supply voltage to VCC, the negative supply voltage to VEE, and the ground reference from supply to GND.

2.2 Single-Supply Operation

To operate as single supply, connect the VEE connector and the GND connector both to ground, and apply the positive supply voltage to VCC. Inputs and outputs must be biased per data sheet specifications for proper operation. R22 must be removed and the VREF pin adjusted to give the proper output common-mode voltage.

3 Input and Output Connections

The OPA862DEVM is equipped with SMA connectors for easy connection of signal generators and analysis equipment. As shipped, the EVM is configured for a gain of 4 V/V, split-supply, single-ended input and output with 50-Ω termination. For best results, signals must be routed to and from the EVM with cables having 50-Ω characteristic impedance. By default IN+ (J2) is used for the input in a noninverting configuration and IN– (J1) is grounded through resistor R5. To use the device with an inverting input, set R5 to match the input signals characteristic impedance and adjust IN+ to set a proper output common-mode voltage. OUT+ (J3) is the output connector for single-ended output signals. The amplifier converts the single-ended input to a differential signal at its output pins. A resistor network (R8, R10, R12, and R13) and the transformer on the amplifier output convert the differential signal to single-ended, and provides a 2-kΩ load to the amplifier when terminated in 50 Ω. A 50-Ω line impedance match at OUT+ must be preserved. The termination network results in an output measurement loss, where the output attenuation is approximately –38 dB and the overall gain is approximately –26 dB. See the OPA862 data sheet applications section, schematics, and layouts for more detail and how to reconfigure the EVM.

3.1 VREF Input Connection

The VREF input (TP4 or J6) sets the common-mode voltage of the OUT– output (CMOUT–) according to the equation CMOUT– = 2 × (VREF) – CMOUT+, where CMOUT+ is the common-mode signal of OUT+ set by the input signal and gain. As shipped, the EVM is configured to accept an input signal with a common-mode voltage set to ground, and therefore the VREF pin is connected to ground by default to create an output common-mode voltage of 0 V on both pins. The VREF pin can be adjusted by removing R22 and applying a voltage at TP4 or by setting a resistor divider with R24 and R25.

3.2 Power-Down Input Connection

The PD connector (J7) allows the OPA862 to be disabled. If required, the SMA connector (J5) can be populated and a signal applied for high-speed testing. Normally jumper J7 is used to enable or disable (power-down) the amplifier when the shorting block is connected to VCC or the amplifier is powered down. When the shorting block is connected to VEE the amplifier is not powered down, and therefore the amplifier is enabled. For high-speed testing, resistor R21 is provided to terminate J5 (the power-down SMA connector). If R21 is installed, remove the shorting block from J7. The default state of the amplifier when R21 is populated is not powered on (disabled) because R21 terminates to ground. When R21 is populated, a signal must be applied to drive the signal to VEE to enable the amplifier.

3.3 Fully Differential Output Configuration

The OPA862DEVM can be reconfigured for fully differential outputs. By removing resistor R18 and transformer T1, and by populating resistors R17, R19, and R20, and SMA connector J4, the output is configured to output a fully differential signal to the J3 and J4 SMA connectors. In this configuration the differential outputs provide an impedance match of 50 Ω, differentially. If a different impedance value is needed, resistors R12 and R13 can be changed to adjust the value. The total impedance of the differential output of the EVM is equal to (R12 + R13) in parallel with (R8 + R9), and can be adjusted according to application requirements. Changing R12 and R13 also changes the total load to the amplifier and further adjustment of R8 and R9 may be necessary to obtain a specific load value.

3.4 Input Bias Current Cancellation

The input series resistors (R3 on the IN+ pin and R23 on the VREF pin) are set to try and balance the offset caused by the input bias currents of the amplifier. The value of 475 Ω was chosen for R3 to create a total impedance on IN+ of 500 Ω when connected to 50-Ω test equipment. This value matches the effective impedance of the IN– node from the parallel combination of the R_F and R_G resistors. If the feedback or gain resistor values are changed then change R3 appropriately to match the parallel combination of R_F and R_G. The VREF pin is internally connected to the positive input of an amplifier core that has 350-Ω effective impedance on the internal negative input. To balance the bias current offset on the internal amplifier core, the value of R23 is set to 348 Ω.

4 Board Layout

The layer plots of Figure 1 to Figure 9 illustrate the board layers in top to bottom order.

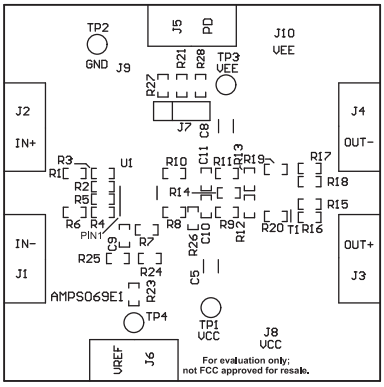

Figure 1. Top Overlay

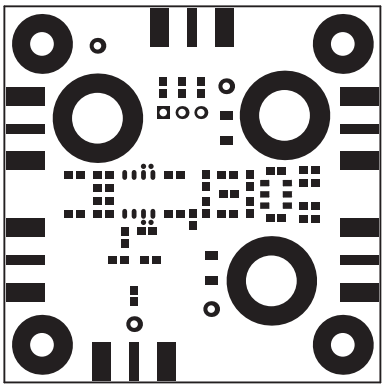

Figure 2. Top Solder

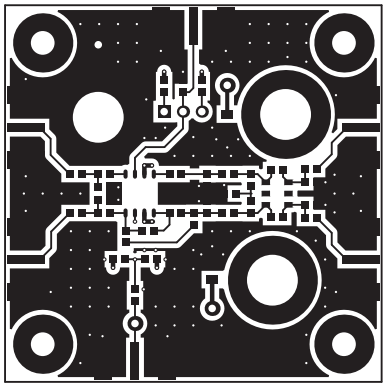

Figure 3. Top Layer

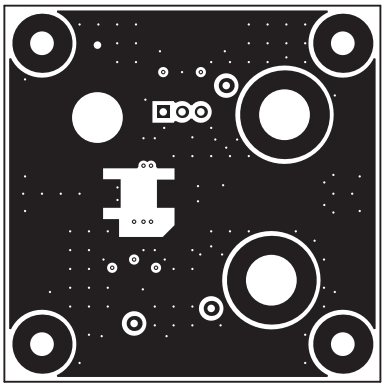

Figure 4. Ground Layer

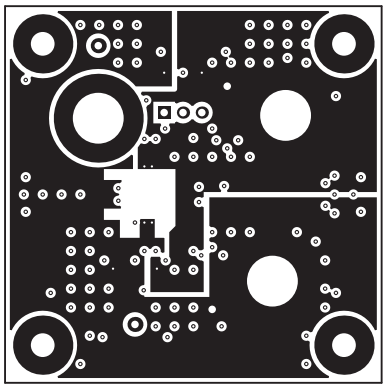

Figure 5. Power Layer

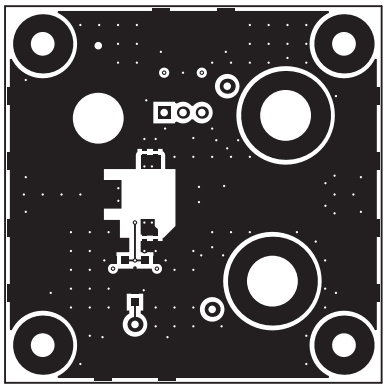

Figure 6. Bottom Layer

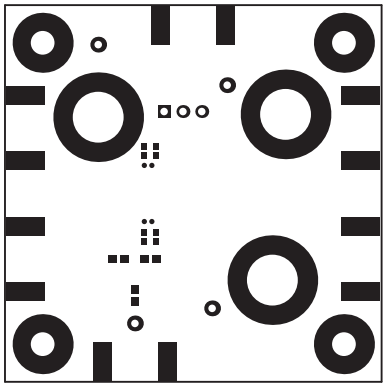

Figure 7. Bottom Solder

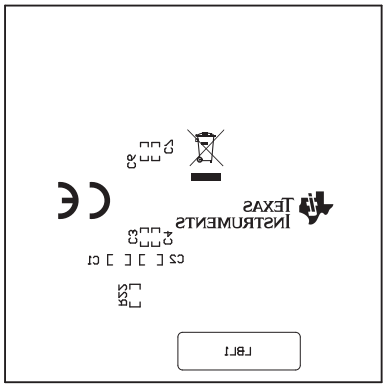

Figure 8. Bottom Overlay

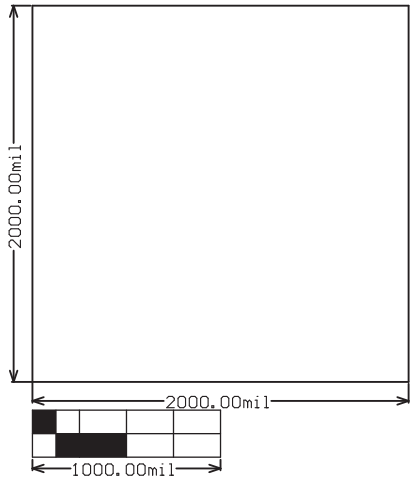

Figure 9. Board Dimensions

5 Schematic and Bill of Materials

This section provides the schematic and bill of materials (BOM) for the OPA862DEVM.

5.1 Schematic

Figure 10 shows the EVM schematic.

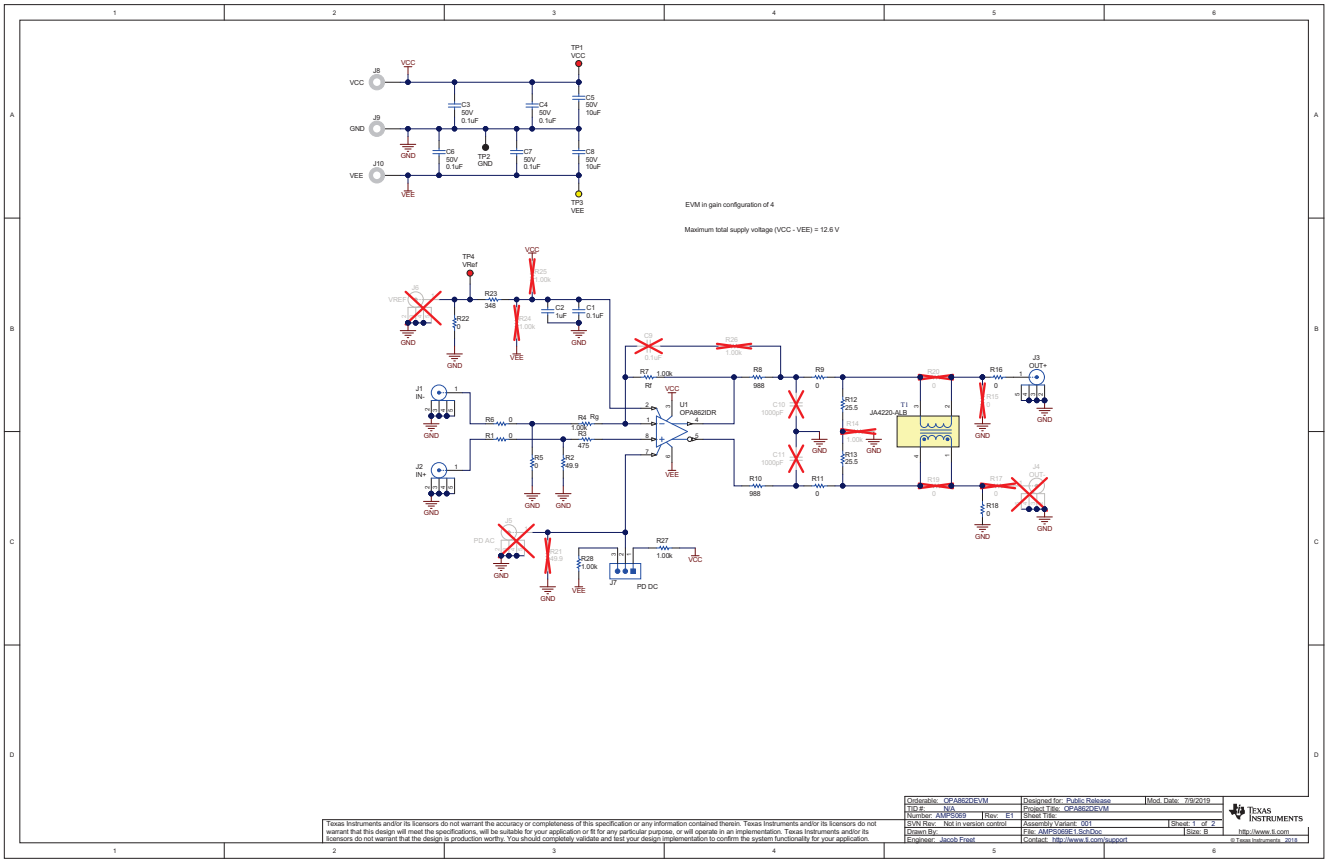

Figure 10. OPA862DEVM Schematic

5.2 Bill of Materials

Table 2 lists the EVM BOM.

Table 2. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C2	1	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	06033C105KAT2A	AVX
C3, C4, C6, C7	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
C5, C8	2	10uF	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1206_190	1206_190	CGA5L3X5R1H106K160AB	TDK
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J3	3		Connector, End launch SMA, 50 ohm, SMT	SMA End Launch	142-0701-851	Cinch Connectivity
J7	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
J8, J9, J10	3		Standard Banana Jack, Uninsulated	Keystone_6095	6095	Keystone
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R5, R6, R9, R11, R16, R18, R22	8	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R2	1	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R3	1	475	RES, 475, 1%, 0.1 W, 0603	0603	CRCW0603475RFKEA	Vishay-Dale
R4, R7, R27, R28	4	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R8, R10	2	988	RES, 988, 0.5%, 0.1 W, 0603	0603	RT0603DRE07988RL	Yageo America
R12, R13	2	25.5	RES, 25.5, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060325R5FKEA	Vishay-Dale
R23	1	348	RES, 348, 0.5%, 0.1 W, 0603	0603	RT0603DRE07348RL	Yageo America
SH-J1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
T1	1	15uH	Transformer, 15 uH, SMT	3.81x3.81mm	JA4220-ALB	Coilcraft CPS
TP1, TP4	2		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2	1		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP3	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1		Ultra Low Power, RRO, Fully Differential Amplifier, D0008A (SOIC-8)	D0008A	OPA862IDR	Texas Instruments
C9	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C10, C11	0	1000 pF	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0603	0603	06031C102KAT2A	AVX
J4, J5, J6	0		Connector, End launch SMA, 50 ohm, SMT	SMA End Launch	142-0701-851	Cinch Connectivity
R14, R24, R25, R26	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R15, R17, R19, R20	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R21	0	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale

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