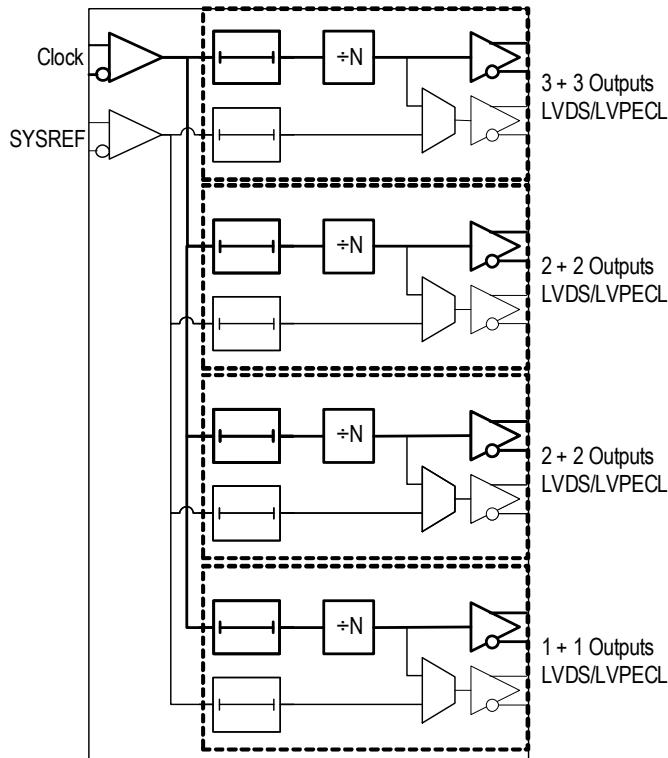


## Description

The 8V79S683 is a fully integrated, clock and SYSREF signal fanout buffer for JESD204B/C applications. It is designed as a high-performance clock and converter synchronization solution for wireless base station radio equipment boards with JESD204B/C subclass 0, 1, and 2 compliance. The main function of the device is the distribution and fanout of high-frequency clocks and low-frequency system reference signals generated by a JESD204B clock generator such as the IDT 8V19N490, extending its fanout capabilities and providing additional phase-delay. The 8V79S683 is optimized to deliver very low phase noise clocks and precise, phase-adjustable SYSREF synchronization signals. Low-skew outputs, low device-to-device skew characteristics and fast output rise/fall times help the system design to achieve deterministic clock and SYSREF phase relationship across devices.

The device distributes the input clock (CLK) and JESD204B SYSREF signals (REF) to four fanout channels. Input clock signals can be frequency divided and are fanned-out to multiple clock (QCLK\_y) and SYSREF (QREF\_r) outputs. Configurable phase-delay circuits are available for both clock and SYSREF signals. The propagation delays in all signal paths are fully deterministic to support fixed phase relationships between clock and SYSREF signals within one device. The device facilitates synchronization between frequency dividers within the device and across multiple devices, removing phase ambiguity introduced in dividers between power and configuration cycles.

## Simplified Block Diagram



## Features

- Distribution, fanout, phase-delay of clock and SYSREF signals
- Very low output noise floor: -158.8dBc/Hz noise floor (245.76MHz)
- Supports clock frequencies up to 3GHz, including clock output frequencies of 983.04MHz, 491.52MHz, 245.76MHz, and 122.88MHz
- Four output channels with a total of 16 differential outputs
- Each channel contains frequency dividers and clock phase delay circuits
- Phase alignment mode across multiple buffers with any frequency divider setting
- Flexible differential outputs (LVDS/LVPECL/amplitude configurable)
- Configuration through 3-wire SPI interface
- Supply voltage:
  - 3.3V core and signal I/O
  - 1.8V Digital control SPI I/O (3.3V-tolerant inputs)
- 64-VFQFPN package (9 × 9 × 0.85 mm)
- Ambient temperature range: -40°C to +105°C (case)

## Typical Applications

- Wireless infrastructure applications: 4G, 5G, and mmWave
- Frequency divider synchronization across multiple devices
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Radar, imaging, instrumentation and medical

## Applicable Standards

JESD204B/C, subclass 0, 1, and 2

## Features (Cont.)

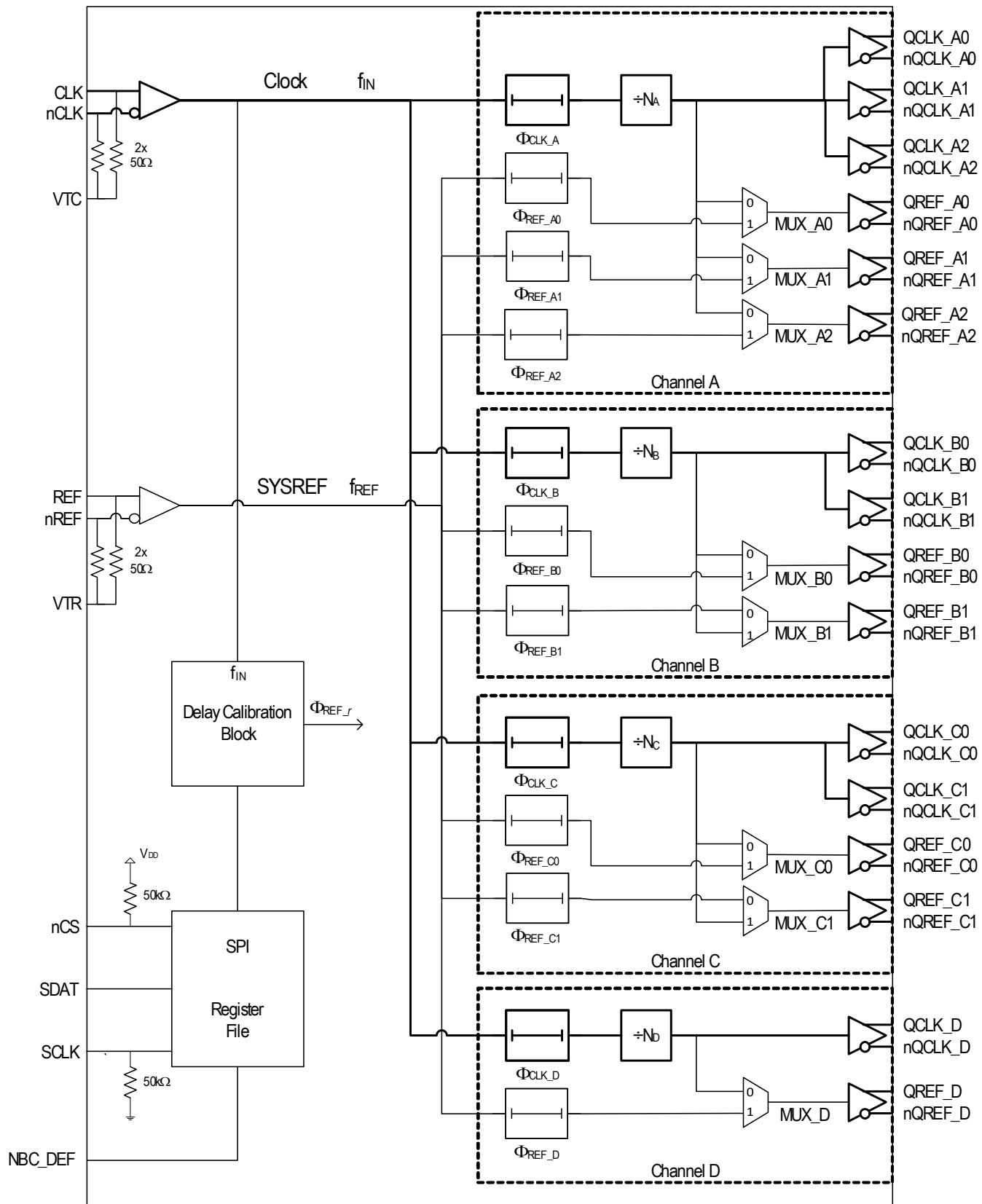
- 4 output channels with a total of 16 differential outputs, organized in:
  - 8 dedicated clock outputs
  - 8 outputs configurable as SYSREF outputs with individual phase delay stages, or configurable as additional clock outputs
  - Clock outputs are powered-on and enabled at startup
  - QREF\_r (SYSREF) outputs are disabled at startup
- Clock channel contains:
  - frequency dividers:  $\div 1, \div 2, \div 3, \div 4, \div 6, \div 8, \div 12, \div 16, \div 24$
  - clock phase delay circuits, delay unit is the clock period; 256 steps
- SYSREF: Configurable precision phase delay circuits: 8 steps of 131ps, 262ps, 393ps or 524ps
- Flexible differential outputs:
  - LVDS/LVPECL configurable
  - Amplitude configurable
  - Power-down modes for unused outputs
  - Supports DC and AC coupling
  - QREF\_r (SYSREF) output pre-bias feature to prevent glitches when turning output on or off

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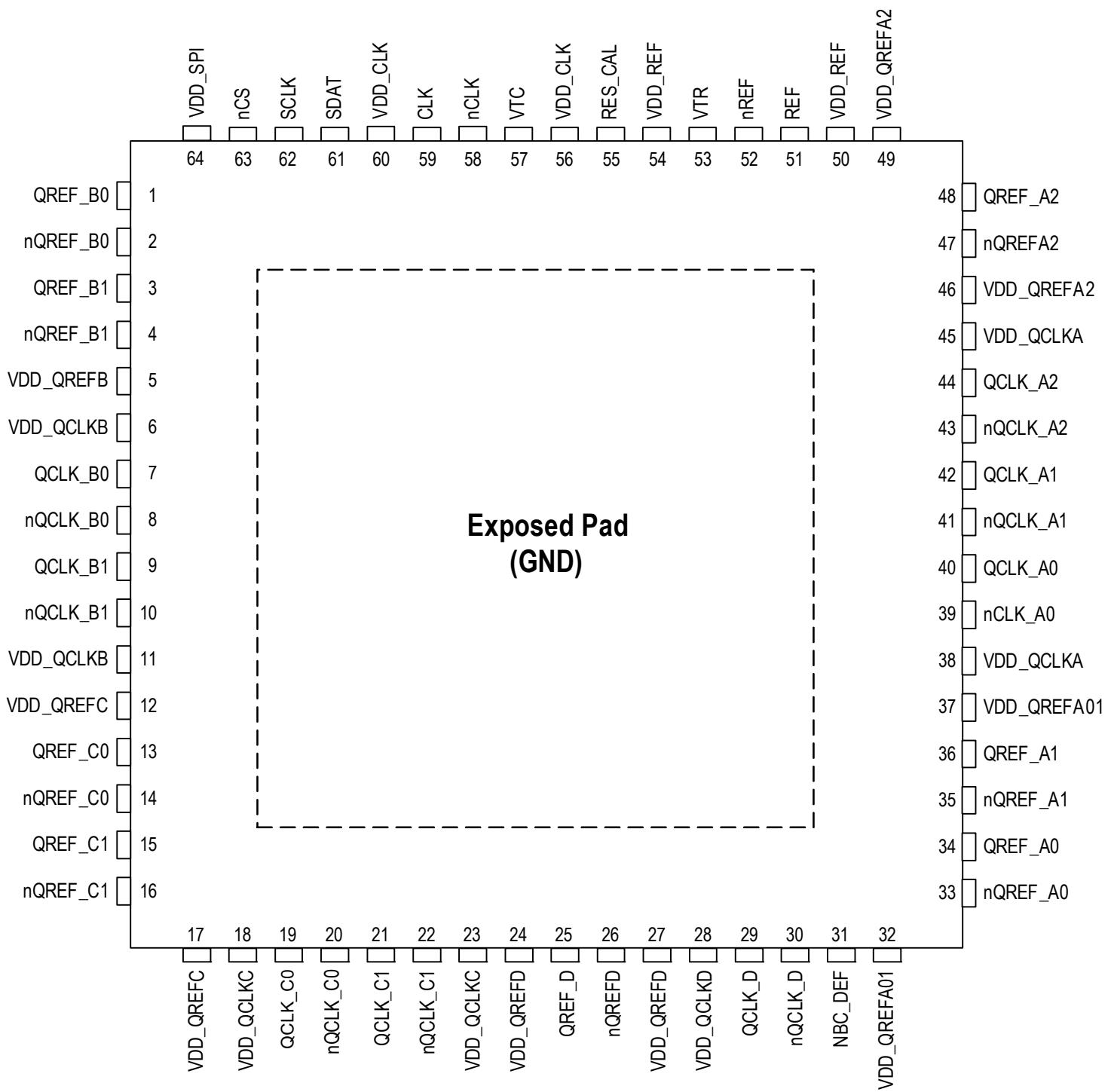
## Block Diagram

Figure 1: Block Diagram



## Pin Assignments

Figure 2: Pin Assignments 9 x 9 x 0.85 mm 64-VFQFPN Package (Top View)



## Pin Descriptions

**Table 1: Pin Descriptions**

Number	Name	Type <sup>a</sup>		Description
1, 2	QREF_B0, nQREF_B0	Output		Differential SYSREF/clock output QREF_B0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
3, 4	QREF_B1, nQREF_B1	Output		Differential SYSREF/clock output QREF_B1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
5	V <sub>DD_QREFB</sub>	Power		Positive supply voltage (3.3V) for the QREF_B[1:0] outputs.
6	V <sub>DD_QCLKB</sub>	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
7, 8	QCLK_B0, nQCLK_B0	Output		Differential clock output QCLK_B0. Configurable LVPECL/LVDS style and amplitude.
9, 10	QCLK_B1, nQCLK_B1	Output		Differential clock output QCLK_B1. Configurable LVPECL/LVDS style and amplitude.
11	V <sub>DD_QCLKB</sub>	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
12	V <sub>DD_QREFC</sub>	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
13, 14	QREF_C0, nQREF_C0	Output		Differential SYSREF/clock output QREF_C0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
15, 16	QREF_C1, nQREF_C1	Output		Differential SYSREF/clock output QREF_C1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
17	V <sub>DD_QREFC</sub>	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
18	V <sub>DD_QCLKC</sub>	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
19, 20	QCLK_C0, nQCLK_C0	Output		Differential clock output QCLK_C0. Configurable LVPECL/LVDS style and amplitude.
21, 22	QCLK_C1, nQCLK_C1	Output		Differential clock output QCLK_C1. Configurable LVPECL/LVDS style and amplitude.
23	V <sub>DD_QCLKC</sub>	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
24	V <sub>DD_QREFD</sub>	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
25, 26	QREF_D, nQREF_D	Output		Differential SYSREF/clock output QREF_D. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
27	V <sub>DD_QREFD</sub>	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
28	V <sub>DD_QCLKD</sub>	Power		Positive supply voltage (3.3V) for the QCLK_D outputs.
29, 30	QCLK_D, nQCLK_D	Output		Differential clock output QCLK_D. Configurable LVPECL/LVDS style and amplitude.
31	NBC_DEF	Input	Pullup	Sets the default (power-up) value of the N <sub>B</sub> and N <sub>C</sub> frequency dividers.
32	V <sub>DD_QREFA01</sub>	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.
33, 34	nQREF_A0, QREF_A0	Output		Differential SYSREF/clock output QREF_A0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
35, 36	nQREF_A1, QREF_A1	Output		Differential SYSREF/clock output QREF_A1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.

**Table 1: Pin Descriptions (Continued)**

Number	Name	Type <sup>a</sup>		Description
37	V <sub>DD_QREFA01</sub>	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.
38	V <sub>DD_QCLKA</sub>	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
39, 40	nQCLK_A0, QCLK_A0	Output		Differential clock output QCLK_A0. Configurable LVPECL/LVDS style and amplitude.
41, 42	nQCLK_A1, QCLK_A1	Output		Differential clock output QCLK_A1. Configurable LVPECL/LVDS style and amplitude.
43, 44	nQCLK_A2, QCLK_A2	Output		Differential clock output QCLK_A2. Configurable LVPECL/LVDS style and amplitude.
45	V <sub>DD_QCLKA</sub>	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
46	V <sub>DD_QREFA2</sub>	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
47, 48	nQREF_A2, QREF_A2	Output		Differential SYSREF/clock output QREF_A2. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
49	V <sub>DD_QREFA2</sub>	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
50	V <sub>DD_REF</sub>	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
51, 52	REF, nREF	Input		SYSREF inverting and non-inverting differential input. Compatible with LVPECL and LVDS signals. REF and nREF are internally 50Ω terminated to the VTR pin
53	VTR	–		Internal termination for the differential clock input REF, nREF. Both REF and nREF inputs are internally terminated 50Ω to this pin. See input termination information in <a href="#">Section "Application Information"</a> .
54	V <sub>DD_REF</sub>	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
55	RES_CAL	Analog		Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.
56	V <sub>DD_CLK</sub>	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
57	VTC	–		Internal termination for the differential clock input CLK, nCLK. Both CLK and nCLK inputs are internally 50Ω terminated to the VTR pin. See input termination information in <a href="#">Section "Application Information"</a> .
58, 59	nCLK, CLK	Input		Device clock inverting and non-inverting differential clock input. Compatible with LVPECL and LVDS signals. CLK and nCLK are internally terminated to VTC through 50Ω.
60	V <sub>DD_CLK</sub>	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
61	SDAT	Input/ Output		Serial Control Port SPI Mode Data Input and Output. 1.8V LVC MOS/LVTTL interface levels. 3.3V tolerant when input.
62	SCLK	Input	PD	Serial Control Port SPI Mode Clock Input. 1.8V LVC MOS/LVTTL interface levels. 3.3V-tolerant when input.
63	nCS	Input	PU	Serial Control Port SPI Chip Select Input. 1.8V LVC MOS/LVTTL interface levels and 3.3V tolerant.
64	V <sub>DD_SPI</sub>	Power		Positive supply voltage (3.3V) for the SPI interface.
Exposed Pad (EP)	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

a. Internal pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. [See Table 25](#) for values.

## Principles of Operation

### Overview

The 8V79S683 is a JESD204B/C Fanout Buffer with Configurable Phase Delay. The device supports the division, phase-delay and distribution of high-frequency clocks (input: CLK, nCLK) and the fanout and phase-delay of low-frequency synchronization (SYSREF) signals (input: REF/nREF). Clock and SYSREF signal paths are independent and are organized in channels, with each channel consisting of several clock and SYSREF outputs. Outputs are configurable with support for LVPECL, LVDS and four amplitude settings. Individual channels and unused circuit blocks support a powered-down state for reduced power consumption operation. The register map, accessible through a SPI interface with read-back capability controls the main device settings.

### Signal Flow

The device offers four channels with the names A, B, C, and D. Each channel supports individual frequency-division, phase-delay and fan-out functions of the input clock to a total of eight QCLK\_y clock outputs; each channel also distributes the SYSREF input signal to multiple QREF\_r outputs with individual per-output phase delay capability.

The central clock distribution ensures low skew clock outputs within each channel; outputs are synchronous across channels (independent on the divider setting) on the incident rising clock edge for all outputs with equal phase delay settings.

SYSREF output are synchronous with each other for equal phase-delay settings. QCLK\_y and QREF\_r outputs will be phase-locked to each other if the CLK and REF inputs are phase-locked. The phase-delay capability in each signal path can be used to establish repeatable and deterministic clock to SYSREF phase relationships at the outputs.

The CLK and QREF signal paths are optimized for channel isolation. allowing high-speed clocks of 983.04MHz, 1474.56MHz or 1966.08MHz (up to 3GHz) and lower-speed SYSREF signals at e.g. 7.68MHz or 9.6MHz with a minimum of signal crosstalk and spurious signals.

### Clock Channel Divider

Each of the four independent frequency dividers  $N_A$ - $N_D$  can be individually set to the divider values  $\div 1$ ,  $\div 2$ ,  $\div 3$ ,  $\div 4$ ,  $\div 6$ ,  $\div 8$ ,  $\div 12$ ,  $\div 16$  and  $\div 24$ . The dividers are synchronous and have an equal propagation delay on the incident edge. See [Table 2](#) for the supported frequency divider settings. The default (power-up) divider value for channel A and D is  $\div 1$ , the default divider value for channel B and C is set by the state of pin 31 (NBC\_DEF).

**Table 2:  $N_{A-D}$  Frequency Divider Settings**

$N_{A-D}$	Clock Divider
0000	$\div 1$ Divider bypass and powered down
0001	$\div 2$
0010	$\div 3$
0011	$\div 4$
0100	$\div 6$
0101	$\div 8$
0110	$\div 12$
0111	$\div 16$
1000	$\div 24$

**Table 3: Frequency Divider Default Settings**

Divider	Default Clock Divider	
	NBC_DEF = 0	NBC_DEF = 1 <sup>a</sup>
$N_A, N_D$	$\div 1$	
$N_B, N_C$	$\div 3$	$\div 4$

a. NBC\_DEF can be left open (reads logic 1)

## Phase Delay

Output phase delay is independently supported on each clock channel and each SYSREF output. The delay unit of the clock channel phase-delay circuits  $\Phi_{CLK\_x}$  is a function of the frequency  $f_{IN}$  applied to CLK input:  $1 \div f_{IN}$ .

The delay unit of the SYSREF phase-delay circuits  $\Phi_{REF\_r}$  is a function of an internal oscillator frequency  $f_{DCO}$  and the DLC multiplier setting. The oscillator is fully self-contained and located in delay calibration block (DCB). At startup, this oscillator is calibrated with the input frequency  $f_{IN}$  as reference. After the calibration, the oscillator is turned-off to save power and to eliminate noise. See [Table 4](#) for details on the delay unit, number of available steps and the delay range.

**Table 4: Delay Circuit Characteristics**

Delay Circuit	Unit	Steps	Range
Clock channel $\Phi_{CLK\_x}$	$1 \div f_{IN}$ 1.017ns at $f_{IN} = 983.04\text{MHz}$	256	$256 \div f_{IN}$ <sup>a</sup> 0 to 259.3ns at $f_{IN} = 983.04\text{MHz}$
SYSREF $\Phi_{REF\_r}$	$T_{DCB}$ <sup>b</sup> DLC = 0: 131ps DLC = 1: 262ps DLC = 2: 393ps DLC = 3: 524ps	8	0...7 * $T_{DCB}$ <sup>c</sup> DLC = 0: 0 to 0.917ns DLC = 1: 0 to 1.834ns DLC = 2: 0 to 2.751ns DLC = 3: 0 to 3.668ns

a. At  $f_{IN} = 983.04\text{MHz}$ , the clock channel delay range is equal to 260.416ns and encompasses 32 periods of a 122.88MHz clock signal.

b.  $T_{DCB} \sim DLC \div (8 \cdot f_{DCO})$ .  $f_{DCO} = 983.04\text{MHz}$ . DLC = 1, 2, 3 or 4.

c. SYSREF phase delay supports  $\geq 8$  delay stops within one input reference period for  $f_{IN} = 254.76\text{MHz}$  to  $f_{IN} = 983.04\text{MHz}$ .

## Delay Calibration Block (DCB)

The DCB sets the SYSREF delay unit by providing a reference signal to the QREF\_r delay circuits. [Figure 3](#) shows the functional diagram. The DCB requires configuration and calibration. Verification of the calibration is optional.

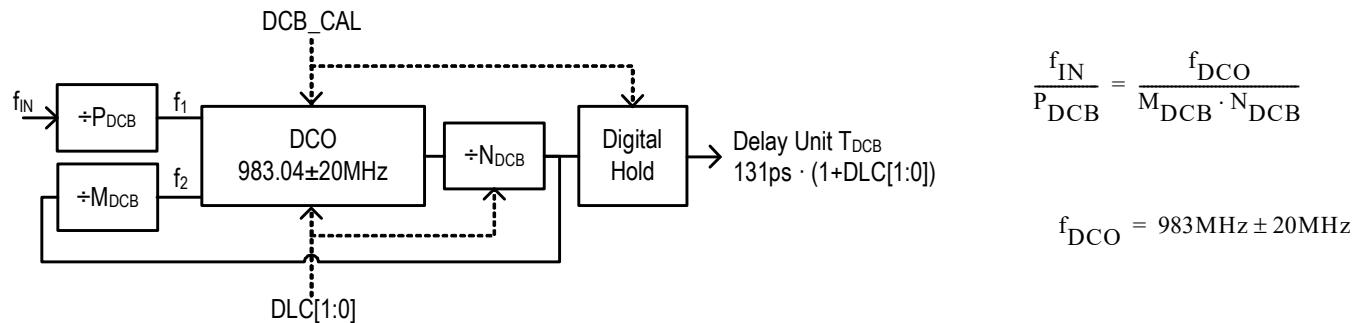
**Description.** The DCB consists of an internal DCO running at  $f_{DCO} = 983.04 \pm 20\text{MHz}$ , three frequency dividers  $P_{DCB}$ ,  $M_{DCB}$  and  $N_{DCB}$  and a digital hold circuit. The DCB input frequency is the device input frequency  $f_{IN}$  at the differential CLK, nCLK input. The input frequency acts as a reference to lock the oscillator to a stable and known frequency.

The output of the DCB is the effective delay unit  $T_{DCB}$  which is approx. one eighth of the oscillator period multiplied by the DLC multiplier. The DLC multiplier extends the delay unit by a factor of 1, 2, 3 or 4. For instance, at a DCO frequency of 983.04MHz, DLC = 1 sets the SYSREF delay unit to 131ps; DLC = 2 sets the delay unit to 262ps, etc.

**Configuration.** Select a desired delay unit and corresponding DLC multiplier from [Table 5](#). DLC[1:0] also sets the  $N_{DCB}$  divider. Then, find a  $P_{DCB}$  and  $M_{DCB}$  divider configuration to locate the oscillator frequency into the range of  $f_{DCO} = 983.04\text{MHz}$  according to the formula in [Figure 3](#). The DCO lock condition is  $f_1 = f_2$  while both  $f_1$  and  $f_2$  must be lower than 200MHz. For instance, if  $f_{IN} = 245.76\text{MHz}$  and the smallest possible SYSREF delay unit is desired, set DLC = 1 (DLC[1:0] = 00; also sets  $N_{DCB} = \pm 1$ ). Then, set  $P_{DCB} = \div 24$  and  $M_{DCB} = \div 96$ . As a result,  $f_1 = f_2 = 10.24\text{MHz}$ ,  $f_{DCO} = 983.04\text{MHz}$ . This example configuration results in a delay unit of measured: 131ps. [Figure 6](#) shows more configuration examples.

**Calibration.** Calibration requires a valid DCB configuration with the DCO locking to an input frequency. Setting DCB\_CAL = 1 starts an automatic calibration. At the end, the DCB\_CAL bit will clear, the delay unit value is stored digitally and the DCO,  $P_{DCB}$ ,  $M_{DCB}$  and  $N_{DCB}$  frequency dividers turn off. The QREF\_r delay circuits now use the stored constant delay unit. The delay unit remains digitally stored until the next power cycle. The DCB calibration must run once as part of the device startup procedure and must be re-run after each input frequency or DCB configuration change.

**Verification.** Verify a successful calibration by reading the DAC\_CODE value.  $0 < \text{DAC\_CODE} < 32767$  indicates a successful calibration. If  $\text{DAC\_CODE} = 0$  or  $\text{DAC\_CODE} = 32767$ , the DCB calibration should be re-run with an alternative  $P_{DCB}$ ,  $M_{DCB}$  setting while maintaining the desired  $M_{DCB} \cdot N_{DCB}/P_{DCB}$  ratio for locking the DCO to the input frequency.

**Figure 3: DCB Functional Diagram****Table 5: DCB Delay Unit at  $f_{DCO} = 983.04\text{MHz}$** 

$T_{DCB}$ Delay Unit (ps)	DLC		$N_{DCB}$
	DLC[1:0] Setting	Numeric Value	
131	00	1	1
262	01	2	2
393	10	3	3
524	11	4	4

**Table 6: DCB Divider Configuration Examples<sup>a</sup>**

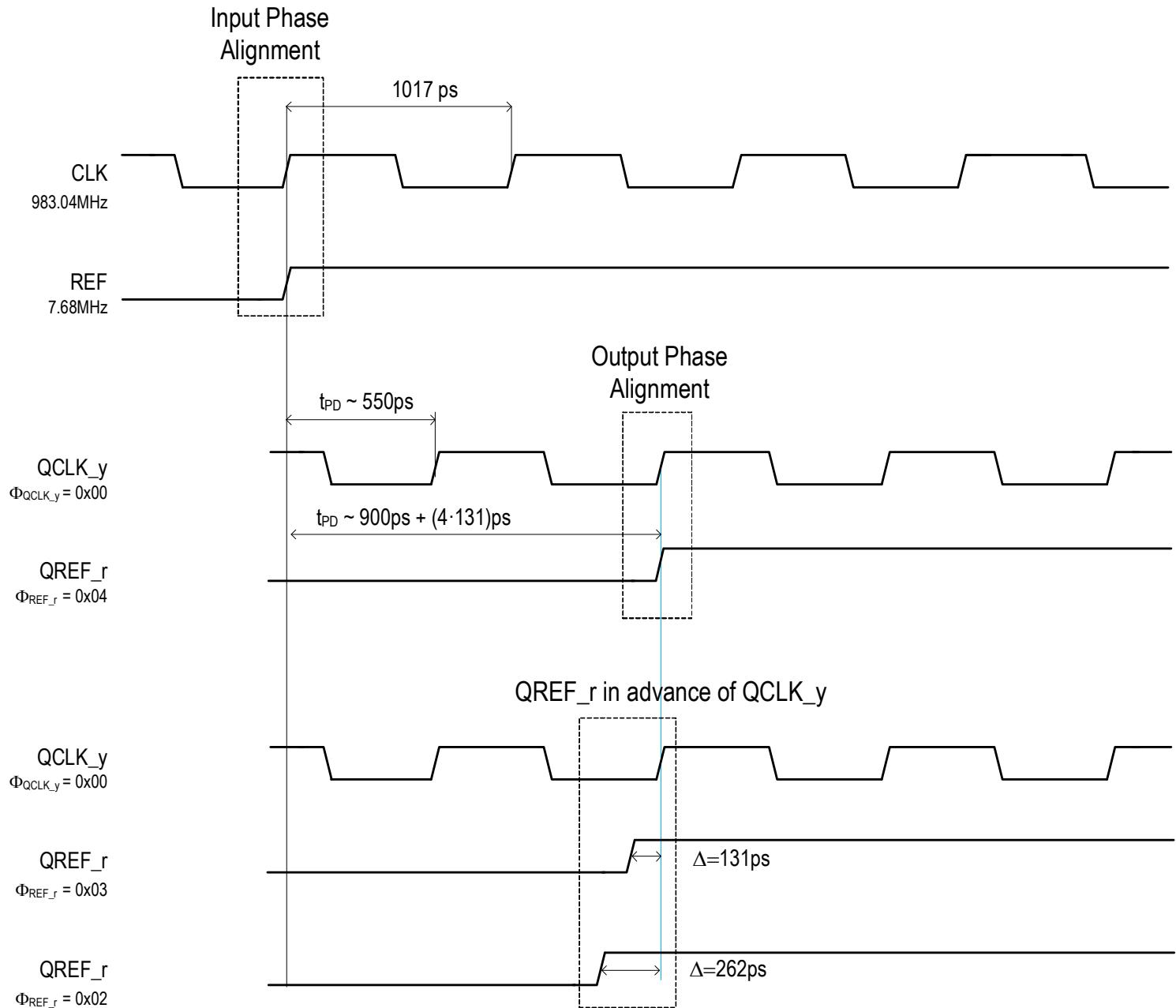
$f_{IN}$ (MHz)	$T_{DCB}$ Delay Unit in ps	DLC	$P_{DCB}$	$M_{DCB}$
245.76	131	1	24	96
	262	2	24	48
	393	3	24	32
	524	4	24	24
491.52	131	1	48	96
	262	2	48	48
	393	3	48	32
	524	4	48	24
983.04	131	1	96	96
	262	2	96	48
	393	3	96	32
	524	4	96	24

a.  $f_{DCO} = 983.04\text{MHz}$

## QCLK\_y to SYSREF Phase Alignment

**Single Device:** To achieve an output phase alignment between the QCLK\_y clock and the QREF\_r SYSREF outputs, the CLK and REF input signals must be phase aligned or have a known, deterministic phase relationship. [Figure 4](#) shows an example output phase alignment for aligned clock and SYSREF inputs. The closest (smallest phase error) output alignment is achieved by setting the clock phase delay register  $\Phi_{QCLK\_Y}$  to 0x00 (clock) and the SYSREF phase delay register  $\Phi_{QCLK\_Y}$  to 0x04. With a SYSREF phase delay setting of 0x03 or less, the QREF\_r output phase is in advance of the QCLK\_y phase, which is applicable in JESD204B/C application. Phase delay settings and propagation delays are independent on the clock and SYSREF frequencies. [Table 7](#) shows recommended phase delay setting several device configurations.

**Figure 4: QCLK\_y to QREF Phase Alignment**



**Table 7: Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment<sup>a</sup>**

Divider Configuration	$\Phi_{CLK\_y}$	$\Phi_{REF\_r}$
$N = \div 1$	0x00	0x04

a. QCLK\_y and QREF outputs are aligned on the incident edge.

### **QCLK\_y and QREF\_r Phase Alignment Across Multiple 8V79S683 Devices**

The device architecture supports phase aligned QCLK\_y and QREF\_r output signals across multiple 8V79S683NLGI devices. For applications that use the frequency dividers of  $\div 2, \div 3, \div 4, \div 6, \div 8, \div 12, \div 16$  or  $\div 24$ , or any combination of these dividers, all devices participating in the output phase alignment must go through a specific alignment procedure at device startup

#### **Pre-conditions**

- Each 8V79S683NLGI device must be driven by a clock device that keeps clock and SYSREF signals aligned at the CLK and REF inputs (see setup and hold time specification)
- The frequency on the REF input must be smaller than any QCLK\_y output frequency
- A valid input frequency must be applied to the CLK input, for instance 491.52MHz

#### **Alignment Method**

- Phase alignment is achieved by driving the all REF inputs with a rising edge signal at the same time with respect to the CLK input signal
- During the alignment process, the output period of the divided clock signal (on QCLK\_y outputs) will have longer periods until output alignment is achieved
  - Example: input CLK frequency is 491.52MHz, output divider is  $\div 4$ , output frequency is 122.88MHz. During the alignment procedure started by REF, the QCLK\_y output period changes from 8.138ns to 10.172ns for multiple cycles. The device facilitates the period of the input signal (2.034ns) to “stretch” the output period:  $8.138\text{ ns} + 2.034\text{ ns} = 10.172\text{ ns}$

#### **Alignment Procedure**

- Set the MD\_ALIGN\_Φ bit to enable the alignment procedure
  - wait for  $\geq 5\text{ }\mu\text{s}$  before applying a signal to the REF input
- Apply an alignment signal (rising edge) to the REF input
  - place the rising edge REF signal before the rising edge of the CLK signal that is shared between all participating buffers
  - REF to CLK setup and hold time specification must be met
  - a single REF rising edge is sufficient for starting the alignment
- Output behavior during alignment:
  - QCLK\_y outputs in  $\div 1$  divider mode work normally as expected without cycle slips or period increases
  - QCLK\_y outputs in  $\div 2, \div 3, \div 4, \div 6, \div 8, \div 12, \div 16$  or  $\div 24$  divider mode expose longer periods as described above
  - REF outputs always buffer out the REF input signal (when QREF\_r outputs are powered on and are enabled)

#### **Result**

- The procedure aligns the output phases (rising incident edge) of all QCLK\_y output signals across participating buffers. This includes the output phases of the frequency-divided clock signals and the outputs divided by 1
- The input to output delay is the same across all participating buffer devices (measured on the incident edge)
- The alignment procedure has a maximum duration of  $48 \times (1/f_{IN})$
- After alignment is achieved, the device auto-clears the MD\_ALIGN\_Φ register bit

The alignment procedure can be repeated at any time after setting the MD\_ALIGN\_Φ bit.

**Table 8: MD\_ALIGN\_Φ Multi-Device Phase Alignment Function Table**

MD_ALIGN_Φ	Operation	Comment
0 (default)	Multi-buffer phase alignment is disabled	SYSREF signals at the REF input are buffered out to the SYSREF outputs when output buffers are enabled.
1	A rising edge at the REF input will start an output phase alignment procedure	Requires a valid clock signal at the CLK input. REF to CLK setup and hold time specifications have to be met. This bit auto-clears after alignment is achieved.

## Differential Outputs

**Table 9: Output Features**

Output	Style	Amplitude <sup>a</sup>	Disable	Power Down	DC Bias	Termination
QCLK_y <sup>b</sup> , QREF_r <sup>c</sup> (Clock)	LVPECL	350-1000mV 3 steps	Yes	Yes	–	50Ω to V <sub>T</sub> <sup>d</sup>
	LVDS	350, 750mV 2 steps				100Ω differential <sup>e f</sup>
QREF_r (SYSREF)	LVPECL	350-1000mV 3 steps	Yes	Yes	–	50Ω to V <sub>T</sub> <sup>d</sup>
	LVDS	350, 750mV 2 steps			Yes <sup>g</sup>	100Ω differential <sup>e f</sup>

a. Amplitudes are measured single-ended. Differential amplitudes supported are 700mV, 1500mV and 2000mV.

b. y = A0, A1, A2, B0, B1, C0, C1 and D.

c. r = A0, A1, A2, B0, B1, C0, C1 and D.

d. V<sub>T</sub> = V<sub>DD\_V</sub> – 1.6V (350mV amplitude setting), V<sub>DD\_V</sub> – 2.0V (750mV amplitude setting), V<sub>DD\_V</sub> – 2.25V (1000mV amplitude setting).

e. AC coupling and DC coupling supported.

f. See [Application Information](#) for output termination information.

g. In JESD204B/C applications, it is recommended to use QREF\_r (SYSREF) outputs configured to LVDS and 350mV amplitude. AC-coupling and DC-coupling is supported.

**Table 10: Individual Clock Output (QCLK\_y) Settings<sup>a</sup>**

PD	STYLE	EN	A[1:0]	Output Power	Termination <sup>b</sup>	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential (LVDS) or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable <sup>c</sup>	X
		1	00			Enable	350
		01					750
		0	XX		50Ω to V <sub>T</sub> (LVPECL)	Disable	X
	1	0	00				350
		01				Enable	750
		10					1000
		11					1000

a. Applicable to clock outputs: QCLK\_y and QREF\_r outputs in clock mode (MUX\_r = 0).

b. See [Application Information](#) for output termination information.

c. Differential output is disabled in static low state: QCLK\_y = L, nQCLK\_y = H.

**Table 11: Individual SYSREF Output (QREF\_r) Settings<sup>a</sup>**

PD	STYLE	Enable	A[1:0]	BIAS	Output Power	Termination <sup>b</sup>	State	Amplitude (mV)	
1	X	X	X	X	Off	100Ω differential or no termination	Off	X	
0	0	0	XX	0	On	100Ω differential (LVDS)	Disable <sup>c</sup>	X	
		00		0			Enabled	350	
		01		0			See <a href="#">Table 12</a>	750	
		1		1			Enabled		
	1	0	XX	0		50Ω to V <sub>T</sub> (LVPECL)	Disable	X	
		00						350	
		01					Enable	750	
		10						1000	
		11						1000	

a. Applicable QREF\_r outputs when configured as SYSREF output (MUX\_r = 1).

b. See [Application Information](#) for output termination information.

c. Differential output is disabled in static low state: QCLK\_y = L, nQCLK\_y = H.

**Table 12: QREF\_r Setting for JESD204B/C Applications**

BIAS_TYPE	BIAS_r	QREF_r Outputs (LVDS)			Application
		Initial	Active Rising Edge on the REF Input	SYSREF Completed	
0	0	Static Low (QREF = L, nQREF_r = H)	Start switching for the number of received SYSREF pulses	Released to static low (QREF = L, nQREF_r = H)	QREF_r DC coupled
	1	Static Low (QREF = L, nQREF_r = H)			
1	0	Static LVDS crosspoint level (QREF = nQREF_r = VOS)	Start switching for the number of received SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_r = VOS)	QREF_r AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_r = VOS)			

## Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to its default value. The default divider value of the NB and NC frequency dividers is set by the state of the NBC\_DEF pin. After internal POR, the device will initialize internal circuits and for 2ms before it accepts an external clock signal at the CLK input (the CLK input is internally turned off during that time).

In the default configuration the QCLK\_y outputs are enabled, QREF outputs are disabled at startup.

Recommended configuration sequence (in order):

1. (Optional) set the value of the CPOL register bit to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Verify the completion of internal power-up by reading the ST\_READY status bit in register 0x6E, bit D1. ST\_READY is set to 1 by the device at the end of the internal power-up procedure. Continue the device startup once ST\_READY is set to 1.
3. Configure the channel circuits and the outputs to the desired values and configure the DCB:
  - For synchronization between multiple devices: See section [QCLK\\_y and QREF\\_r Phase Alignment Across Multiple 8V79S683 Devices](#). After the MD\_ALIGN\_Φ bit is set, the device will wait for a REF rising edge input to start the phase alignment. After alignment is completed, the MD\_ALIGN\_Φ bit will auto-clear. The multi-device alignment requires a valid clock signal to be applied to the CLK input.
  - Output source MUX\_r, output divider N<sub>A-D</sub>, clock delay Φ<sub>A-D</sub>; MUX-output style, amplitude and power down mode for QCLK\_y and QREF\_r outputs
  - (Optional) the global BIAS\_TYPE bit and BIAS\_r for each QREF\_r in preparation for JESD204B/C SYSREF operation
  - Phase delay for Φ<sub>REF\_r</sub> values for the QREF\_r outputs
  - Setup the DCB settings DLC, P<sub>DCB</sub> and M<sub>DCB</sub> as described in the paragraph *Configuration*, see [Delay Calibration Block \(DCB\)](#)
4. If not already applied: apply a valid input frequency to CLK. Set the PB\_CAL bit and the DCB\_CAL bit to start the calibration of the precision bias current circuit and the DCB calibration. Both bits will auto-clear. See paragraph *Configuration* in section [Delay Calibration Block \(DCB\)](#).
  - (Optional): verify the success of the DCB calibration by reading the DAC\_CODE value. See paragraph *Verification* in section [Delay Calibration Block \(DCB\)](#)
5. (Only for using the clock delay circuits): Set the initialization bit INIT\_CLK to initiate the ΦCLK\_x delay circuits. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state.
6. Enable or disable outputs as desired by accessing the output-enable registers 0x74 and 0x76.
7. At this point, the configuration of the registers should be completed and the SPI transfer ended. Set nCS to high level.

Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

## Changing Frequency Dividers and Phase Delay Values

### Clock Frequency Divider and Delay

Following procedure has to be applied for a change of a clock divider and phase delay value  $N_{A-D}$ , and  $\Phi_{CLKA-D}$ :

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) disable the outputs whose frequency divider or delay value is changed
3. Configure the  $N_{A-D}$  dividers and the delay circuits  $\Phi_{CLKA-D}$  to the desired new values
4. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state
5. (Optional) Enable the outputs whose frequency divider was changed

### SYSREF Delay

Following procedure has to be applied for a change of any SYSREF phase delay value  $\Phi_{REF\_r}$ :

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Configure any delay circuits  $\Phi_{REF\_r}$  to their desired new values. During configuration of  $\Phi_{REF\_r}$  outputs are not stopped or interrupted.

## SPI Interface

The 8V79S683 has a 3-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output), and nCS (chip select) pins. A data transfer consists of any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each. If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the 8V79S683 is disabled. In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

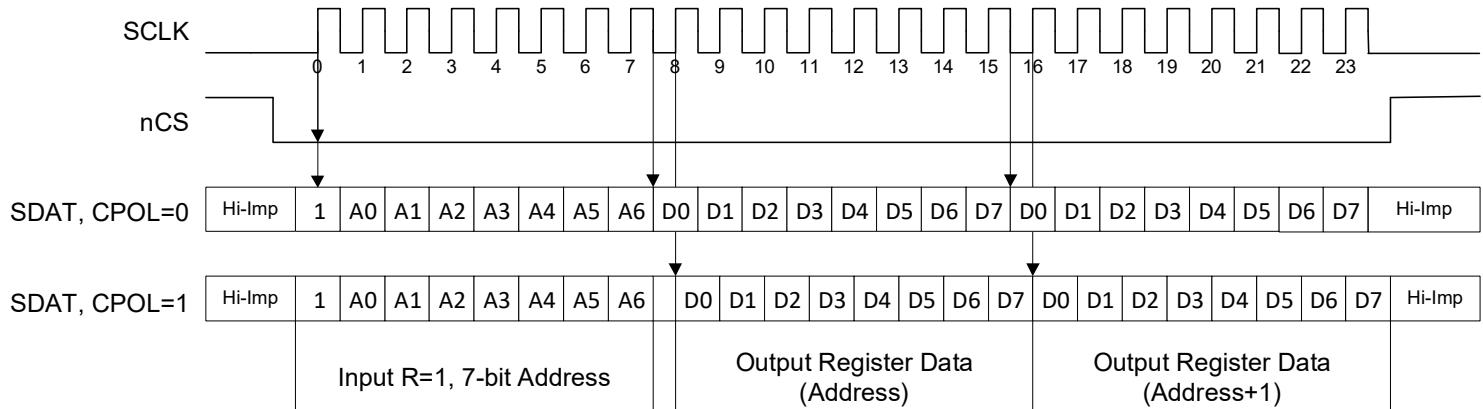
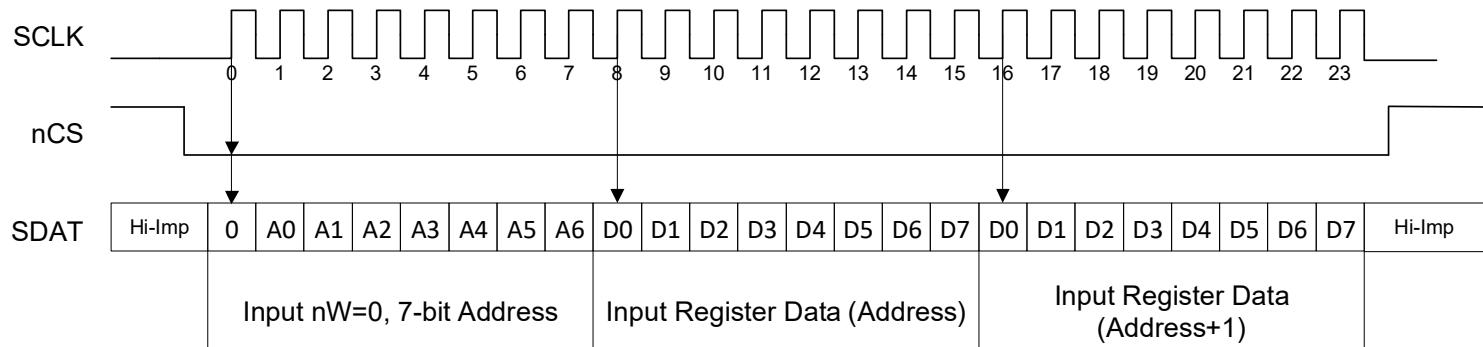
**Starting a data transfer** requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

**Read operation** from an internal register: a read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the rising edge of SCLK. The first bit is the direction bit R/nW which must be to 1 to indicate a read transfer, followed by 7 address bits A[0:6]. After the first 8 bits are clocked into SDAT, the SDAT I/O changes to output: the register content addressed by A[0:6] is loaded into the shift register and the next 8 SCLK falling clock cycles (if CPOL = 0) will then present the loaded register data on the SDAT output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes in a single block read.

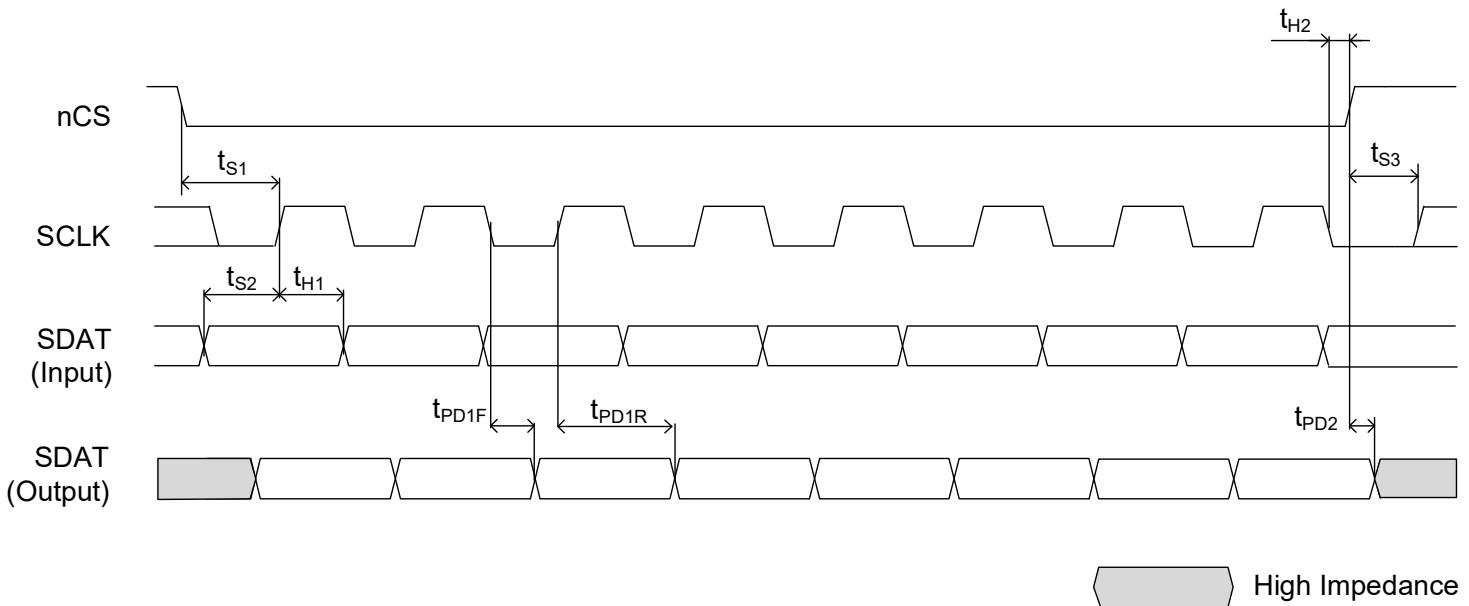
**Write operation** to a 8V79S683 register: During a write transfer, a SPI master transfers one or more bytes of data into the internal registers of the 8V79S683. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

**End of transfer:** After de-asserting nCS, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram ([Figure 5](#)) and WRITE diagram ([Figure 6](#)) displaying the transfer of two bytes of data from and into registers

**Registers 0x78 to 0xFF:** Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

**Figure 5: Logic Diagram: READ Data from 8V79S683 Registers for CPOL = 0 and CPOL = 1****Figure 6: Logic Diagram WRITE Data into 8V79S683 Registers****Table 13: SPI Read / Write Cycle Timing Parameters**

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
$f_{SCLK}$	SCLK frequency			20	MHz
$t_{S1}$	Setup time, nCS (falling) to SCLK (rising)		5		ns
$t_{S2}$	Setup time, SDAT (input) to SCLK (rising)		5		ns
$t_{S3}$	Setup time, nCS (rising) to SCLK (rising)		5		ns
$t_{H1}$	Hold time, SCLK (rising) to SDAT (input)		5		ns
$t_{H2}$	Hold time, SCLK (falling) to nCS (rising)		5		ns
$t_{PD1F}$	Propagation delay, SCLK (falling) to SDAT	CPOL = 0		12	ns
$t_{PD1R}$	Propagation delay, SCLK (rising) to SDAT	CPOL = 1		12	ns
$t_{PD2}$	Propagation delay, nCS to SDAT disable			12	ns
$t_{R, F}$	Rise, Fall Time, SPI Inputs SCLK, SDAT		1	10	ns

**Figure 7: SPI Timing Diagram**

## Register Descriptions

This section contains a list of all addressable registers and a register description, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, but with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields will be unaffected by writes and are undefined on reads.

**Table 14: Configuration Registers**

Register Address	Register Description
0x00 - 0x17	Reserved
0x18 - 0x1B	SYSREF, DCB and Phase Alignment Control
0x1C - 0x1F	Reserved
0x20	Channel A, Output Divider
0x21	Channel A Delay $\Phi$ CLK_A
0x22	Channel A PD
0x23	Reserved
0x24	Output State QCLK_A0
0x25	Output State QCLK_A1
0x26	Output State QCLK_A2
0x27	Reserved
0x28	$\Phi$ REF_A0 Delay, MUX

**Table 14: Configuration Registers (Continued)**

Register Address	Register Description
0x29	$\Phi_{REF\_A1}$ Delay, MUX
0x2A	$\Phi_{REF\_A2}$ Delay, MUX
0x2B	Reserved
0x2C	Output State QREF_A0
0x2D	Output State QREF_A1
0x2E	Output State QREF_A2
0x2F	Reserved
0x30	Channel B, Output Divider
0x31	Channel B Delay $\Phi_{CLK\_B}$
0x32	Channel B PD
0x33	Reserved
0x34	Output State QCLK_B0
0x35	Output State QCLK_B1
0x36 - 0x37	Reserved
0x38	$\Phi_{REF\_B0}$ Delay, MUX
0x39	$\Phi_{REF\_B1}$ Delay, MUX
0x3A-0x3B	Reserved
0x3C	Output State QREF_B0
0x3D	Output State QREF_B1
0x3E-0x3F	Reserved
0x40	Channel C, Output Divider
0x41	Channel C Delay $\Phi_{CLK\_C}$
0x42	Channel C PD
0x43	Reserved
0x44	Output State QCLK_C0
0x45	Output State QCLK_C1
0x46-0x47	Reserved
0x48	$\Phi_{REF\_C0}$ Delay, MUX
0x49	$\Phi_{REF\_C1}$ Delay, MUX
0x4A-0x4B	Reserved
0x4C	Output State QREF_C0
0x4D	Output State QREF_C1
0x4E-0x4F	Reserved
0x50	Channel D, Output Divider

**Table 14: Configuration Registers (Continued)**

Register Address	Register Description
0x51	Channel D Delay $\Phi$ CLK_D
0x52	Channel D PD
0x53	Reserved
0x54	Output State QCLK_D
0x55-0x57	Reserved
0x58	$\Phi$ REF_D Delay, MUX
0x59-0x5B	Reserved
0x5C	Output State QREF_D
0x5D-0x6B	Reserved
0x6C-0x73	General Control
0x74	Output State QCLK
0x75	Reserved
0x76	Output State QREF
0x77	Reserved
0x78	Do not use
0x79	Do not use
0x7A	Do not use
0x7B	Do not use
0x7C-0x7D	Do not use
0x7E	Do not use
0x7F	Do not use
0x80-0xFF	Do not use

## Channel and Clock Output Registers

The content of the channel register and clock output registers set the clock divider, output style, amplitude, power down state, enable state and the clock phase delay.

**Table 15: Channel and Clock Output Register Bit Field Locations**

Bit Field Location															
Register Address	D7	D6	D5	D4	D3	D2	D1	D0							
0x20	Reserved	Reserved	Reserved	Reserved	N_A[3:0]										
0x30					N_B[3:0]										
0x40					N_C[3:0]										
0x50					N_D[3:0]										
0x21	ΦCLK_A[7:0]														
0x31	ΦCLK_B[7:0]														
0x41	ΦCLK_C[7:0]														
0x51	ΦCLK_D[7:0]														
0x22	PD_A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved							
0x32	PD_B														
0x42	PD_C														
0x52	PD_D														
0x24: QCLK_A0	PD_A0	Reserved	Reserved	STYLE_A0A1	A_A0A1[1:0]		Reserved								
0x25: QCLK_A1	PD_A1			Reserved	Reserved										
0x26: QCLK_A2	PD_A2			STYLE_A2	A_A2[1:0]										
0x34: QCLK_B0	PD_B0	Reserved	Reserved	STYLE_B0B1	A_B0B1[1:0]		Reserved								
0x35: QCLK_B1	PD_B1			Reserved	Reserved										
0x44: QCLK_C0	PD_C0	Reserved	Reserved	STYLE_C0	A_C0[1:0]		Reserved								
0x45: QCLK_C1	PD_C1			STYLE_C1	A_C1[1:0]										
0x54: QCLK_D	PD_D	Reserved	Reserved	STYLE_D	A_D[1:0]		Reserved								
0x74	EN_QCLK_A0	EN_QCLK_A1	EN_QCLK_A2	EN_QCLK_B0	EN_QCLK_B1	EN_QCLK_C0	EN_QCLK_C1	EN_QCLK_D							

**Table 16: Channel and Clock Output Register Descriptions<sup>a</sup>**

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
N_x[3:0]	R/W	N_A = 0000 (÷1) N_B = 001[NBC_DEF] (÷4/÷3) N_C = 001[NBC_DEF] ÷4/÷3 N_D = 0000 (÷1)	Output Frequency Divider N
			N_x[2:0] Frequency Divider
			0000 ÷1 (Divider bypassed and powered-down)
			0001 ÷2
			0010 ÷3
			0011 ÷4
			0100 ÷6
			0101 ÷8
			0110 ÷12
			0111 ÷16
			1000 ÷24
			The default value of the N_B and N_C divider is set by pin 31 (NBC_DEF). See <a href="#">Table 3</a> .
PD_x	R/W	0 Value: Power up	0 = Channel x is powered up 1 = Channel x is powered down
PD_y	R/W	0 Value: Power up	0 = Output QCLK_y is powered up 1 = Output QCLK_y is powered down
ΦCLK_x[7:0]	R/W	0000 0000 Value: 0ns	CLK_x Phase Delay
			ΦCLK_x[7:0] Phase Delay in units of the input period: ΦCLK_x[7:0] ÷ f <sub>IN</sub> (256 steps).
			0000 0000 0ps
			0000 0001 1 ÷ f <sub>IN</sub>
			... 1111 1111 255 ÷ f <sub>IN</sub>

**Table 16: Channel and Clock Output Register Descriptions<sup>a</sup>**

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
A_y[1:0]	R/W	01 Value: 750mV	QCLK_y Output Amplitude
			Setting for STYLE = 0 (LVDS) Termination: 100Ω across
			Setting for STYLE = 1 (LVPECL) Termination: 50Ω to V <sub>T</sub>
			A[1:0] = 00: 350mV A[1:0] = 01: 750mV A[1:0] = 10: Reserved A[1:0] = 11: Reserved
			A[1:0] = 00: 350mV A[1:0] = 01: 750mV A[1:0] = 10: 1000mV A[1:0] = 11: 1000mV
The following control bits combine the A(mplitude) function for multiple outputs: A_A0A1 sets the output amplitude for QCLK_A0 and QCLK_A1 A_B0B1 sets the output amplitude for QCLK_B0 and QCLK_B1			
STYLE_y		0 Value: LVDS	QCLK_y Output Format.  0 = Output(s) is/are LVDS (requires LVDS 100Ω output termination) 1 = Output(s) is LVPECL (requires LVPECL 50Ω output termination to the specified recommended termination voltage)
			The following control bits combine the STYLE function for multiple outputs: STYLE_A0A1 sets the output format for QCLK_A0 and QCLK_A1 STYLE_B0B1 sets the output format for QCLK_B0 and QCLK_B1
EN_y		1 Value: enabled	QCLK_y Output Enable: 0 = QCLK_y Output is disabled at the logic low state 1 = QCLK_y Output is enabled

a. x = A, B, C, D; y = A0, A1, A2, B0, B1, C0, C1, D.

## QREF\_r Output State Registers

The content of the QREF\_r output registers selects the source signal of the QREF\_r outputs, set the phase delay, the style, the amplitude, the power state, the enable state and the output bias.

**Table 17: QREF\_r Output State Register Bit Field Locations<sup>a</sup>**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QREF_A0 0x29: QREF_A1 0x2A: QREF_A2	Reserved	Reserved	Reserved	MUX_A0 MUX_A1 MUX_A2	ΦREF_A0[2:0] ΦREF_A1[2:0] ΦREF_A2[2:0]		Reserved	
0x38: QREF_B0 0x39: QREF_B1	Reserved	Reserved	Reserved	MUX_B0 MUX_B1	ΦREF_B0[2:0] ΦREF_B1[2:0]		Reserved	
0x48: QREF_C0 0x49: QREF_C1	Reserved	Reserved	Reserved	MUX_C0 MUX_C1	ΦREF_C0[2:0] ΦREF_C1[2:0]		Reserved	
0x58: QREF_D	Reserved	Reserved	Reserved	MUX_D	ΦREF_D[2:0]			Reserved
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_A0 PD_A1 PD_A2	Reserved	BIAS_A0 BIAS_A1 BIAS_A2	STYLE_A0 STYLE_A1 STYLE_A2	A_A0[1:0] A_A1[1:0] A_A2[1:0]	Reserved		Reserved
0x3C: QREF_B0 0x3D: QREF_B1	PD_B0 PD_B1	Reserved	BIAS_B0 BIAS_B1	STYLE_B0 STYLE_B1	A_B0[1:0] A_B1[1:0]	Reserved		Reserved
0x4C: QREF_C0 0x4D: QREF_C1	PD_C0 PD_C1	Reserved	BIAS_C0 BIAS_C1	STYLE_C0 STYLE_C1	A_C0[1:0] A_C1[1:0]	Reserved		Reserved
0x5C: QREF_D	PD_D	Reserved	BIAS_D	STYLE_D	A_D[1:0]	Reserved		Reserved
0x76	EN_QREF_A0 EN_QREF_A1 EN_QREF_A2 EN_QREF_B0 EN_QREF_B1 EN_QREF_C0 EN_QREF_C1 EN_QCLK_D							

a. r = A0, A1, A2, B0, B1, C0, C1, D.

**Table 18: QREF\_r Output State Register Descriptions<sup>a</sup>**

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
MUX_r	R/W	1 Value: QREF_r = SYSREF	0 = QREF_r output signal source is the channel's clock signal 1 = QREF_r output signal source is the centrally generated SYSREF signal	
ΦREF_r[2:0]	R/W	000 Value: 0ps	SYSREF Phase Delay:  QREF_r delay = ΦREF_r[2:0] · T <sub>DCB</sub> . Delay values for f <sub>DCO</sub> = 983.04MHz. Delay values are a function of T <sub>DCB</sub> .	
			ΦREF_r[2:0]   QREF_r delay in ps for a DLC[1:0] setting of:	
			00	01
			000	0
			001	131
			010	262
			...	...
			111	917
BIAS_r	R/W	0	QREF_r Output Bias Voltage:  Individual QREF_r output LVDS output bias operation. Not applicable to QREF_r outputs set to LVPECL mode.	
			0 = Normal operation  1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0.	
			BIAS_TYPE	BIAS_r
			0	0
			0	1
			1	0
			1	1

**Table 18: QREF\_r Output State Register Descriptions<sup>a</sup>**

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
A_r[1:0]	R/W	01 Value: 750mV	QREF_r Output Amplitude
			Setting for STYLE = 0 (LVDS) Termination: 100Ω across
			Setting for STYLE = 1 (LVPECL) Termination: 50Ω to V <sub>T</sub>
			A[1:0] = 00: 350mV A[1:0] = 01: 750mV A[1:0] = 10: Reserved A[1:0] = 11: Reserved
PD_r	R/W	0 Value: Powered up	QREF_r Output Power Down: 0 = Output is powered up 1 = Output is powered down. STYLE, EN and A[1:0] settings have no effect
STYLE_r	R/W	0 Value: LVDS	QREF_x Output Format. 0 = Output is LVDS (requires LVDS 100Ω output termination) 1 = Output is LVPECL (requires LVPECL 50Ω output termination of to the specified recommended termination voltage)
EN_r	R/W	0 Value: Disabled	QREF_r Output Enable: 0 = Output is disabled at the logic low state 1 = Output is enabled

a. r = A0, A1, A2, B0, B1, C0, C1, D. x = A, B, C, D

## SYSREF, DCB, and Phase Alignment Control Registers

**Table 19: SYSREF, DCB and Phase Alignment Control Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x18	PD_S	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x19	BIAS_TYPE	DLC[1:0]		Reserved	Reserved	Reserved	Reserved	M_DC[8]
0x1A	M_DC[7:0]							
0x1B	N_ALIGN	P_DC[6:0]						

**Table 20: SYSREF, DCB and Phase Alignment Control Register Descriptions**

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
PD_S	R/W	0 Value: Powered up	SYSREF Global Power-down: 0 = SYSREF functional blocks are powered-up 1 = SYSREF functional blocks are powered-down	
BIAS_TYPE	R/W	0	SYSREF Output Voltage Bias: Global to all QREF_r outputs bit to control the LVDS output operation. Not applicable to QREF_r outputs set to LVPECL mode.	
			BIAS_TYPE	BIAS_r
			QREF_r output operation if set to LVDS.	
			0	0
			QREF_r outputs are initially logic low (QREF_r = L, nQREF_r = H) and will start switching on the first rising edge of the REF input. Use in DC-coupled applications.	
			0	1
			Disabled with static low/high levels. During a SYSREF event, the output remains at static low levels (QREF_r = L, nQREF_r = H).	
			1	0
			Both QREF_r and nQREF_r outputs are initially set to the LVDS crosspoint level (VOS) and will start switching on the first rising edge of the REF input. Use in AC-coupled applications.	
			1	1
			Output is statically set to the LVDS crosspoint voltage. During a SYSREF event, the output remains at the LVDS crosspoint level (VOS).	

**Table 20: SYSREF, DCB and Phase Alignment Control Register Descriptions**

Register Description													
Bit Field Name	Field Type	Default (Binary)	Description										
DLC[1:0]	R/W	00 Value: 131ps	<p>Delay Unit Multiplier: Effective delay unit for the SYSREF outputs is <math>(1 + \text{DLC}[1:0]) \div (8 \cdot f_{\text{DCO}})</math>.</p> <table border="1"> <tr> <td>DLC[1:0]</td><td>Effective SYSREF Delay Unit for <math>f_{\text{DCO}} = 983.04\text{MHz}</math></td></tr> <tr> <td>00</td><td>131ps</td></tr> <tr> <td>01</td><td>262ps</td></tr> <tr> <td>10</td><td>393ps</td></tr> <tr> <td>11</td><td>524ps</td></tr> </table>	DLC[1:0]	Effective SYSREF Delay Unit for $f_{\text{DCO}} = 983.04\text{MHz}$	00	131ps	01	262ps	10	393ps	11	524ps
DLC[1:0]	Effective SYSREF Delay Unit for $f_{\text{DCO}} = 983.04\text{MHz}$												
00	131ps												
01	262ps												
10	393ps												
11	524ps												
M_DC[8:0]	R/W	0 0001 0000 Value: 16	Delay Calibration Block (DCB) DCO feedback divider. Set in conjunction with $f_{\text{IN}}$ and $P_{\text{DCB}}$ to achieve a DCO frequency of $983.04 \pm 20\text{MHz}$ : $f_{\text{DCO}} = f_{\text{IN}} \div P_{\text{DCB}} \cdot M_{\text{DCB}}$ .										
N_ALIGN	R/W	0 Value: $\div 24$	<p>Frequency divider dividing the input clock signal (<math>f_{\text{IN}}</math>) to an internal reference for the multi-device phase alignment engine. Use <math>\div 48</math> if any of the output clock divider is <math>N_x = \div 16</math>. The divider setting has an impact on the max. frequency <math>f_{\text{REF}}</math> during multi-device phase alignment (see <math>f_{\text{REF}}</math> in AC characteristics table).</p> <p><math>0 = \div 24</math>.</p> <p><math>1 = \div 48</math></p>										
P_DC[6:0]	R/W	000 1000 Value: 8	Delay Calibration Block (DCB) DCO input divider. Set in conjunction with $f_{\text{IN}}$ and $M_{\text{DCB}}$ to achieve DCO frequency of $983.04 \pm 20\text{MHz}$ : $f_{\text{DCO}} = f_{\text{IN}} \div P_{\text{DCB}} \cdot M_{\text{DCB}}$ . DCO phase detector frequency should not exceed 200MHz.										

## General Control Registers

**Table 21: General Control Register Bit Field Locations**

Register Address	Bit Field Location										
	D7	D6	D5	D4	D3	D2	D1	D0			
0x6C	Reserved	DAC_CODE[14:8]									
0x6D	DAC_CODE[7:0]										
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ST_READY	Reserved		
0x6F	Reserved	Reserved	PBIAS[5:0]								
0x70	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		
0x71	DCB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		
0x72	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		
0x73	MD_ALIGN_Φ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL		

**Table 22: General Control Register Descriptions**

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
DAC_CODE[14:0]	R only	X	DAC_CODE is the result of the internal DCB calibration routine. Trigger calibration by setting the DCB_CAL bit.
ST_READY	R only	X	Internal startup routine completion status. The device is ready for operation when this bit is set to 1. 0 = Incomplete 1 = Completed and device is ready for operation.
PBIAS[5:0]	R only	X	BIAS level.
INIT_CLK	W only Auto-Clear	X	Clock divider and phase clock phase delay initialization. Set INIT_CLK = 1 to initialize N_x divider and $\Phi$ CLK_x clock phase delay functions. Required as part of the startup procedure and after each change of a clock divider or clock phase delay value.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration: Set PB_CAL to 1 starts the auto-calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS. This bit will auto-clear after the calibration completed. Required to set as part of the startup procedure.
DCB_CAL	W only Auto-Clear	X	DCB Calibration: Setting this bit to 1 will begin the auto-calibration of the DCB. The DCB provides a reference for the SYSREF delay circuits. This bit will auto-clear. This bit should be set as part of the startup procedure. The result of the calibration routine is stored in the DAC_CODE register.
CPOL	R/W	0	SPI Read Operation SCLK Polarity: 0 = Data bits on MISO are output at the falling edge of SCLK edge. 1 = Data bits on MISO are output at the rising edge of SCLK edge.
MD_ALIGN_Φ	R/W Auto-clear	0	Multi-Buffer Phase Alignment Enable 0 = Multi-buffer phase alignment is disabled 1 = Multi-buffer phase alignment is enabled. The next rising edge at the REF input will start the phase alignment.

## Electrical Characteristics

### Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V79S683 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 23: Absolute Maximum Ratings**

Item	Rating
Supply Voltage, $V_{DD\_V}$	3.6V
Inputs	-0.5V to $V_{DD\_V}$ + 0.5V
Outputs, $V_O$ (LVC MOS)	-0.5V to $V_{DD\_V}$ + 0.5V
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	50mA 100mA
Input termination current, $I_{VT}$	$\pm 35$ mA
Junction Temperature, $T_J$	150°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
ESD - Human Body Model <sup>a</sup>	2000V
ESD - Charged Device Model <sup>a</sup>	500V

a. According to JEDEC JS-001-2012/JESD22-C101.

**Table 24: Recommended Operating Conditions**

Item	Rating
Supply Voltage, $V_{DD\_V}$	3.3V
Operating Junction Temperature, $T_J$ <sup>a</sup>	$\leq 125$ °C
Board Temperature, $T_B$	$\leq 105$ °C

a. 125°C/10year lifetime is based on the evaluation of intrinsic wafer process technology reliability metrics. The limiting wafer level reliability factor for this technology with respect to high temperature operation is electro-migration. The device is verified to the maximum operating junction temperature through simulation.

## Pin Characteristics

**Table 25: Pin Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			2	4	pF
$R_{PD}$	Input Pull-Down Resistor	SCLK		51		k $\Omega$
$R_{PU}$	Input Pull-Up Resistor	nCS		51		k $\Omega$
$R_{OUT}$	LVC MOS Output Impedance	SDAT (when output)		25		$\Omega$

## DC Characteristics

**Table 26: Power Supply DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C^a$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD\_V}$	Core Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$ (Total)	Power Supply Current	QCLK_y and QREF_r set to LVDS, 750mV amplitude, terminated 100 $\Omega$ , Nx dividers set to $\div 1$		820	960	mA

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 27: Typical Power Supply Current Characteristics,  $V_{DD\_V} = 3.3V$ ,  $T_A = 25^\circ C^a$**

Symbol	Supply Pin Current	Test Case						Unit
		1	2	3	4	5	6	
QCLK_y	Style	LVPECL	LVPECL	LVDS	LVDS	LVDS	LVDS	mV
	State	On	On	On	On	On	On	
	Amplitude	350	750	350	350	750	750	
QREF_r	Style	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	mV
	State	Off	Off	Off	On	On	On	
	Amplitude	–	–	–	350	350	750	
$I_{DD\_SC}$	Current through the $V_{DD\_SPI}$ , $V_{DD\_CLK}$ pins	124	124	125	125	125	125	mA
$I_{DD\_CLKAB}$	Current through the $V_{DD\_QCLKA}$ , $V_{DD\_QCLKB}$ pins	73	84	134	134	187	186	mA
$I_{DD\_CLKCD}$	Current through the $V_{DD\_QCLKC}$ , $V_{DD\_QCLKD}$ pins	58	65	94	94	126	126	mA

**Table 27: Typical Power Supply Current Characteristics,  $V_{DD\_V} = 3.3V$ ,  $T_A = 25^\circ C$ <sup>a</sup>**

Symbol	Supply Pin Current	Test Case						Unit
		1	2	3	4	5	6	
$I_{DD\_REFAB}$	Current through the $V_{DD\_REF}$ , $V_{DD\_QREF01}$ , $V_{DD\_QREF02}$ , $V_{DD\_QREFB}$	37	38	107	230	230	283	mA
$I_{DD\_REFCD}$	Current through the $V_{DD\_QREFC}$ , $V_{DD\_QREFD}$ pins	4	5	9	83	83	115	mA
$P_{TOT}$	Total Device Power Consumption	1.15	1.28	1.55	2.20	2.48	2.76	W
$P_{TOT, SYS}$	Total System Power Consumption <sup>b</sup>	1.54	1.75	1.55	2.20	2.48	2.76	W

a.  $f_{IN}$  (input) = 491.52MHz,  $f_{SYSREF}$  = 7.68MHz. Supply current is independent on the output frequency. QCLK\_y outputs terminated according to amplitude settings. QREF\_r outputs unterminated when SYSREF is turned off.

b. Includes total device power consumption and the power dissipated in external output termination components.

**Table 28: LVC MOS DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ <sup>a</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	NBC_DEF	$V_{DD\_V} = 3.3V$ , $V_{IN} = 3.3V$	2.0		$V_{DD\_V}$	V
$V_{IL}$	Input Low Voltage			-0.3		0.8	V
$I_{IH}$	Input High Current	NBC_DEF	$V_{DD\_V} = 3.3V$ , $V_{IN} = 0V$			5	$\mu A$
$I_{IL}$	Input Low Current			-150			$\mu A$

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpmin. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 29: LVC MOS (JESD8-7A, 1.8V) DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ <sup>a b</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{T+}$	Positive-going input threshold voltage	SCLK, nCS, SDAT		0.660		1.365	V
$V_{T-}$	Negative-going input threshold voltage			0.495		1.170	V
$V_H$	Hysteresis Voltage		$V_{T+} - V_{T-}$	0.165		0.780	V
$I_{IH}$	Input High Current		$V_{DD\_V} = 3.3V, V_{IN} = 1.8V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current		$V_{DD\_V} = 3.465V, V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage	SDAT (when output)	$I_{OH} = -4\text{mA}$	1.4			V
$V_{OL}$	Output Low Voltage		$I_{OL} = 4\text{mA}$			0.45	V

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Table is valid for the SPI interface pins nCS, SCLK and SDAT. SPI inputs have hysteresis.

**Table 30: Differential Input DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ <sup>a</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Input Resistance	CLK, nCLK REF, nREF		43.5	50	56.5	$\Omega$
$R_{IN\_DIFF}$	Differential Input Resistance	CLK, nCLK REF, nREF		87	100	113	$\Omega$

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 31: LVPECL DC Characteristics (QCLK\_y, QREF\_r, STYLE = 1),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ <sup>a</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage <sup>b</sup>	Any Amplitude Setting	$V_{DD\_V} - 1.20$	$V_{DD\_V} - 0.90$	$V_{DD\_V} - 0.60$	V
$V_{OL}$	Output Low Voltage <sup>b</sup>	350mV Amplitude Setting	$V_{DD\_V} - 1.40$	$V_{DD\_V} - 1.24$	$V_{DD\_V} - 1.05$	V
		750mV Amplitude Setting	$V_{DD\_V} - 1.90$	$V_{DD\_V} - 1.71$	$V_{DD\_V} - 1.60$	V
		1000mV Amplitude Setting	$V_{DD\_V} - 2.20$	$V_{DD\_V} - 1.98$	$V_{DD\_V} - 1.80$	V

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Outputs terminated with  $50\Omega$  to  $V_T = V_{DD\_V} - 1.6V$  (350mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting)

**Table 32: LVDS DC Characteristics (QCLK\_y, QREF\_r, STYLE = 0),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ <sup>a</sup> b**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OS}$	Offset Voltage <sup>c</sup>	350mV Amplitude Setting	1.20	1.25	1.30	V
		750mV Amplitude Setting	1.25	1.30	1.35	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Outputs are terminated  $100\Omega$ .

c.  $V_{OS}$  changes with  $V_{DD\_V}$ .

## AC Characteristics

**Table 33: AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}^a$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency <sup>b</sup>	CLK, nCLK	Single device	0	983.04	3000	MHz
			Phase alignment between multiple devices	>0		1000	MHz
$f_{REF}$	Input Frequency	REF, nREF	SYSREF operation	0		100	MHz
			During multi-device phase alignment <sup>c</sup>				
			$N_{ALIGN} = \div 24$	>0		$f_{IN} \div 48$	MHz
$V_{IN}$	Input Voltage Amplitude <sup>d</sup>	CLK, nCLK REF, nREF		0.15		1.2	V
$V_{DIFF\_IN}$	Differential Input Voltage Amplitude <sup>d e</sup>	CLK, nCLK REF, nREF		0.3		2.4	V
$V_{CMR}$	Common Mode Input Voltage			1		$V_{DD\_V} - (V_{IN} / 2)$	V
$f_{OUT}$	Output Frequency		QCLK_y, QREF_r (Clock), $N = \div 1$ to $\div 24$	0	983.04	$3000 \div N$	MHz
			QREF_r (SYSREF)	0		100	MHz
odc	Output Duty Cycle <sup>f</sup>		QCLK_y, QREF_r (Clock), $f_{IN} \leq 2500\text{MHz}$	45	50	55	%
			QCLK_y, QREF_r (Clock), $2500\text{MHz} < f_{IN} \leq 3000\text{MHz}$	42	50	58	%
			QREF_r (SYSREF at 7.68MHz)	45	50	55	%
$t_R / t_F$	Output Rise/Fall Time		QCLK_y, QREF_r (LVPECL), 20% to 80%			250	ps
			QCLK_y, QREF_r (LVDS), 20% to 80%			250	ps
			QREF_r (SYSREF, LVDS), 20% to 80%			250	ps
$V_{O(PP)}^g$	LVPECL Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	250	350	450	mV
			750mV Amplitude Setting	650	750	850	mV
			1000mV Amplitude Setting	900	1000	1100	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	500	700	900	mV
			750mV Amplitude Setting	1300	1500	1700	mV
			1000mV Amplitude Setting	1800	2000	2200	mV
$V_{O(PP)}^h$	LVDS Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	250	350	450	mV
			750mV Amplitude Setting	600	750	900	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	500	700	900	mV
			750mV Amplitude Setting	1200	1500	1800	mV

**Table 33: AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ <sup>a</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsk(o)	Output Skew; NOTE <sup>i,j</sup> All delays set to 0	QCLK_y (same N divider) <sup>k</sup>			100	ps
		QCLK_y (any N divider, incident rising edge)			100	ps
		QREF_r (Clock)			100	ps
		QREF_r (SYSREF)			100	ps
		QCLK_y to QREF_r (QREF_r as clock output) <sup>k</sup>			200	ps
tsk(pp)	Part-to-part skew All delays set to 0	CLK to any QCLK_y <sup>k</sup>			375	ps
		REF to any QREF_r			375	ps
t <sub>PD</sub>	Propagation Delay <sup>k</sup> All delay circuits set to 0	CLK to QCLK_y <sup>k</sup>	250		750	ps
		REF to QREF_r ( $\Phi_{REF\_y} = 0$ )	600	800	1000	ps
$\Delta t_{PD}$	Propagation delay variation between the clock input and any QCLK_y output	CLK to QCLK_y <sup>k</sup>	-100		+100	ps
t <sub>S</sub>	Setup time <sup>l</sup>	REF to CLK (rising)			250	ps
t <sub>H</sub>	Hold time	CLK (rising) to REF			250	ps
	Output isolation between any QCLK_y-QCLK_y and QREF_r-QREF_r outputs	$f_{QCLK\_y} = 983.04\text{MHz}^m$	60			dB
		$f_{QCLK\_y} = 491.52\text{MHz}^m$	65			dB
		$f_{QCLK\_y} = 245.76\text{MHz}^m$	70			dB
	Output isolation between any QREF_r/QCLK_y outputs	$f_{QCLK\_y} = 983.04\text{MHz}$ , $491.52\text{MHz}$ , $245.76\text{MHz}$ ; $f_{QREF\_r} = 7.68\text{MHz}$	50			dB

- a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- b. The CLK, nCLK input supports 0Hz if the applied static signal has a minimum amplitude as specified by  $V_{IN}$ ,  $V_{DIFF\_IN}$ .
- c. Only applicable to a multi-device phase alignment procedure as a max frequency for applying multiple edges to the REF input. This specification is not applicable if a single REF edge is used for multi-device phase alignment.
- d.  $V_{IL}$  should not be less than -0.3V and  $V_{IH}$  should not be greater than  $V_{DD\_V}$ .
- e. Common Mode Input Voltage is defined as the cross-point voltage.
- f. Input = 50% duty cycle.
- g. LVPECL outputs terminated with  $50\Omega$  to  $V_T = V_{DD\_V} - 1.6V$  (350mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting).
- h. LVDS outputs terminated  $100\Omega$  across Q, nQ.
- i. This parameter is defined in accordance with JEDEC standard 65.
- j. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points
- k. All frequency dividers N are in  $\div 1$ ,  $\div 2$ ,  $\div 4$  or  $\div 8$ ; output amplitude setting 750mV.
- l. Failure to meet CLK/REF setup and hold time can result in a failure to align output phases across multiple devices
- m. Output amplitudes set to 350mV or 750mV.

**Table 34: DCB and Phase Delay Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}^a$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{DCO}$	DCO Lock Range		963.04	983.04	1003.04	MHz	
$T_{DCB}$	$\Phi_{REF\_r}$ Delay Unit Range	$f_{DCO} = 983.04\text{MHz}$	DLC = 1 (DLC[1:0] = 00)	115	131	150	ps
			DLC = 2 (DLC[1:0] = 01)	230	262	300	ps
			DLC = 3 (DLC[1:0] = 10)	345	393	450	ps
			DLC = 4 (DLC[1:0] = 11)	460	524	600	ps
		$f_{DCO} = 963.04\text{MHz}$ (min DCO frequency)	DLC = 1 (DLC[1:0] = 00)	113	134	152	ps
			DLC = 2 (DLC[1:0] = 01)	226	268	304	ps
			DLC = 3 (DLC[1:0] = 10)	339	402	456	ps
			DLC = 4 (DLC[1:0] = 11)	452	536	608	ps
		$f_{DCO} = 1003.04\text{MHz}$ (max DCO frequency)	DLC = 1 (DLC[1:0] = 00)	112	128	142	ps
			DLC = 2 (DLC[1:0] = 01)	224	256	284	ps
			DLC = 3 (DLC[1:0] = 10)	336	384	426	ps
			DLC = 4 (DLC[1:0] = 11)	448	512	568	ps
$T_{IN}^b$	$\Phi_{CLK\_x}$ Delay Unit	$f_{IN} = 983.04\text{MHz}$			1017		ps
$f_1, f_2$	DCO Phase Detector Frequency				200	MHz	
$\Delta t_D$	Delay unit variation	$\Phi_{REF\_r}$ delay unit variation (deviation from nominal, DLC[1:0] = 00)		-30	0	+30	ps
		$\Phi_{CLK\_y}$ delay unit variation (deviation from nominal)		-20	0	+20	ps

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b.  $\Phi_{CLK\_x}$  clock channel delay unit is equal to  $1 \div f_{IN}$ .

## Additive Clock Phase Noise Characteristics

The 8V79S683 is a buffer device, it does not filter the phase noise on the input clock source. Phase noise caused by noise sources within the device can add to the input signal noise, resulting in an increased noise on the outputs (additive phase noise). Phase noise from within the part is not correlated with the noise on the input, therefore the root-sum-square method must be used to calculate the output phase noise:

$\Phi_{\text{OUT}}^2 = \Phi_{\text{IN}}^2 + \Phi_{\text{DEVICE}}^2$ . As a consequence, at frequency offsets where the input phase noise  $\Phi_{\text{IN}}$  is higher than internal noise sources, the effect of additive phase noise is not measurable.

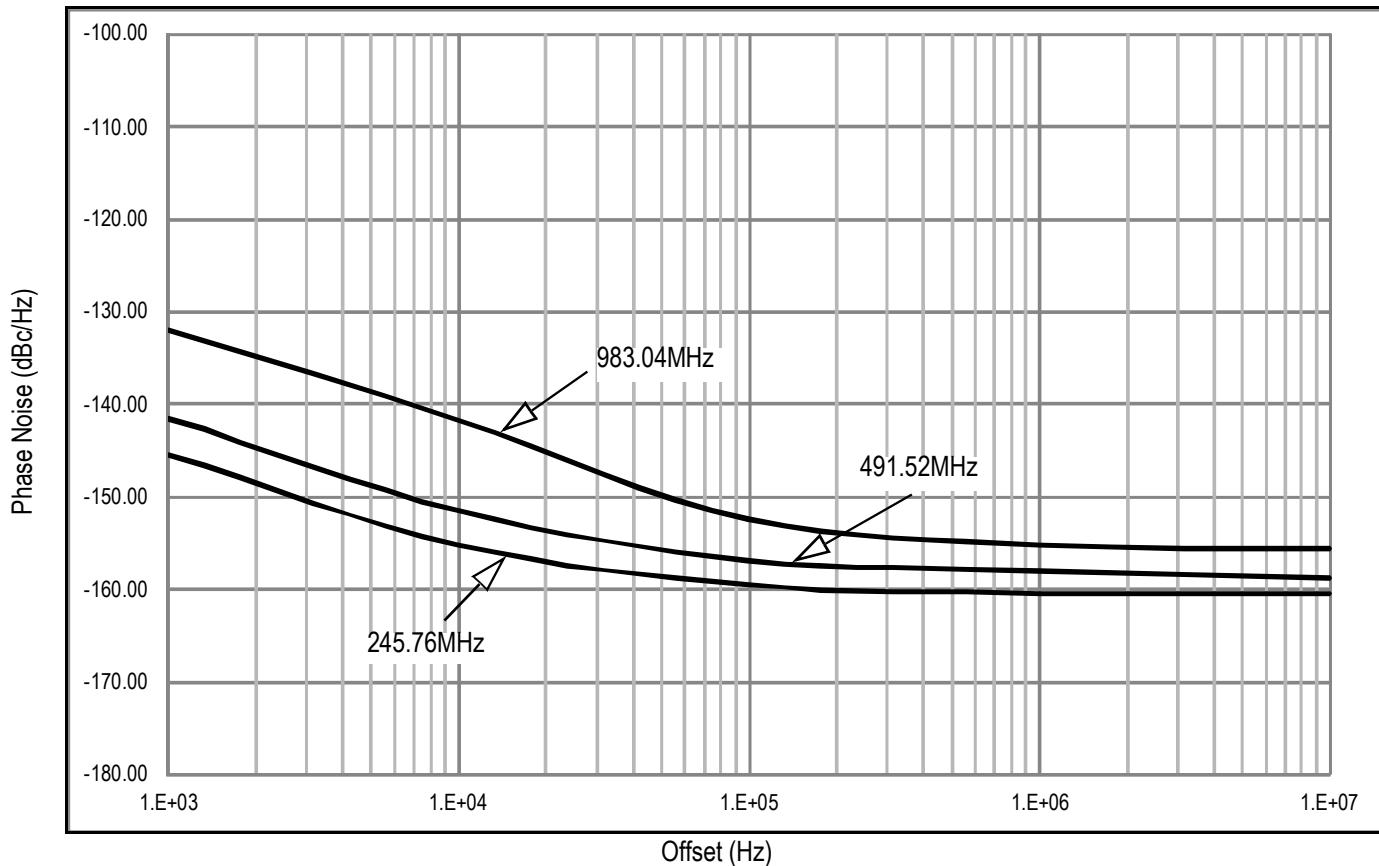
Simulations of the device phase noise performance are done with an ideal input source, however, simulation models may not account for all possible internal noise sources. [Table 35](#) shows the simulation results for the 8V79S683 buffer with an ideal input source. [Table 38](#) shows output phase noise measured with a low-noise input source, with one column for the measured data and a second column which de-rates the measured data by a factor to model the process variation. [Table 38](#) shows that the input phase noise is the dominating factor in the measured data up to an offset of 100kHz. Above 100kHz, the noise floor of the device dominates the characteristics.

**Table 35: Additive Clock Phase Noise Characteristics (Simulation<sup>a</sup>),  $V_{\text{DD}_V} = 3.3\text{V} \pm 5\%$ <sup>b</sup>**

Symbol	Parameter		Test Conditions	25°C	85°C, Worst Case	Units
$\Phi_N(1\text{k})$	QCLK_y Phase Noise	245.76MHz	1kHz offset from Carrier	-146.2	-145.5	dBc/Hz
$\Phi_N(10\text{k})$			10kHz offset from Carrier	-156.6	-155.3	dBc/Hz
$\Phi_N(100\text{k})$			100kHz offset from Carrier	-161.9	-159.6	dBc/Hz
$\Phi_N(1\text{M})$			1MHz offset from Carrier	-162.4	-160.5	dBc/Hz
$\Phi_N(10\text{M})$			10MHz offset from Carrier and Noise Floor	-162.4	-160.5	dBc/Hz
$\Phi_N(1\text{k})$		491.52MHz	1kHz offset from Carrier	-141.6	-141.6	dBc/Hz
$\Phi_N(10\text{k})$			10kHz offset from Carrier	-152.7	-151.6	dBc/Hz
$\Phi_N(100\text{k})$			100kHz offset from Carrier	-159.2	-157.0	dBc/Hz
$\Phi_N(1\text{M})$			1MHz offset from Carrier	-159.8	-158.1	dBc/Hz
$\Phi_N(10\text{M})$			10MHz offset from Carrier and Noise Floor	-159.9	-158.2	dBc/Hz
$\Phi_N(1\text{k})$		983.04MHz	1kHz offset from Carrier	-134.5	-132.0	dBc/Hz
$\Phi_N(10\text{k})$			10kHz offset from Carrier	-141.4	-141.8	dBc/Hz
$\Phi_N(100\text{k})$			100kHz offset from Carrier	-155.8	-152.6	dBc/Hz
$\Phi_N(1\text{M})$			1MHz offset from Carrier	-157.2	-155.3	dBc/Hz
$\Phi_N(10\text{M})$			10MHz offset from Carrier and Noise Floor	-157.2	-155.8	dBc/Hz

a. Ideal input signal: rectangular clock signal with a slew rate of 5V/ns and without phase noise.

b. Phase noise and spurious specifications apply for device operation with QREF\_r outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal, process and voltage variations included.

**Figure 8: Additive Clock Phase Noise Characteristics (85°C, Worst Case Simulation Model)**

**Table 36: Additive Clock Phase Noise Characteristics (Measured),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}^{\text{a b}}$** 

Symbol	Parameter		Test Conditions	Measured <sup>c</sup>	De-Rated <sup>d</sup>	Units
$\Phi_N(1k)$	QCLK_y Phase Noise	245.76MHz	1kHz offset from Carrier	-141.4	-137.2	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier	-151.7	-149.5	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier	-157.8	-155.5	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier	-158.6	-156.2	dBc/Hz
$\Phi_N(10M)$			10MHz offset from Carrier and Noise Floor	-158.8	-156.3	dBc/Hz
$\Phi_N(1k)$		491.52MHz	1kHz offset from Carrier	-135.3	-128.4	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier	-145.8	-140.5	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier	-154.2	-149.5	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier	-157.2	-155.4	dBc/Hz
$\Phi_N(10M)$			10MHz offset from Carrier and Noise Floor	-157.6	-156.3	dBc/Hz
$\Phi_N(1k)$	983.04MHz	1kHz offset from Carrier	-131.3	-125.7	dBc/Hz	
$\Phi_N(10k)$		10kHz offset from Carrier	-141.2	-138.5	dBc/Hz	
$\Phi_N(100k)$		100kHz offset from Carrier	-149.6	-146.5	dBc/Hz	
$\Phi_N(1M)$		1MHz offset from Carrier	-154.5	-152.2	dBc/Hz	
$\Phi_N(10M)$		10MHz offset from Carrier and Noise Floor	-155.3	-152.5	dBc/Hz	
$t_{\text{jit}}(\emptyset)$	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 61.44MHz		100	fs
			Integration Range: 12kHz - 20MHz		100	fs

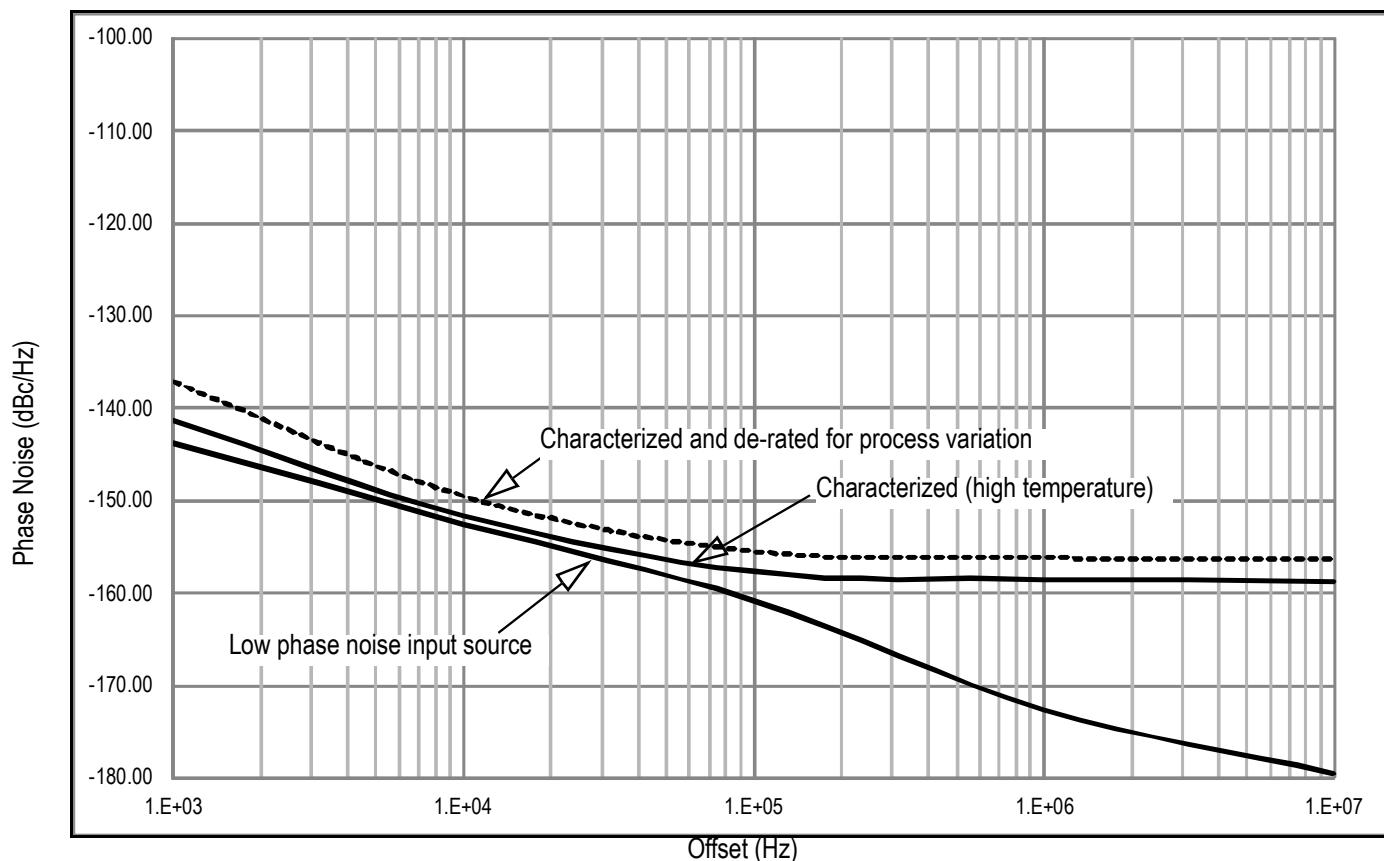
a. Phase noise and spurious specifications apply for device operation with QREF\_r outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal.

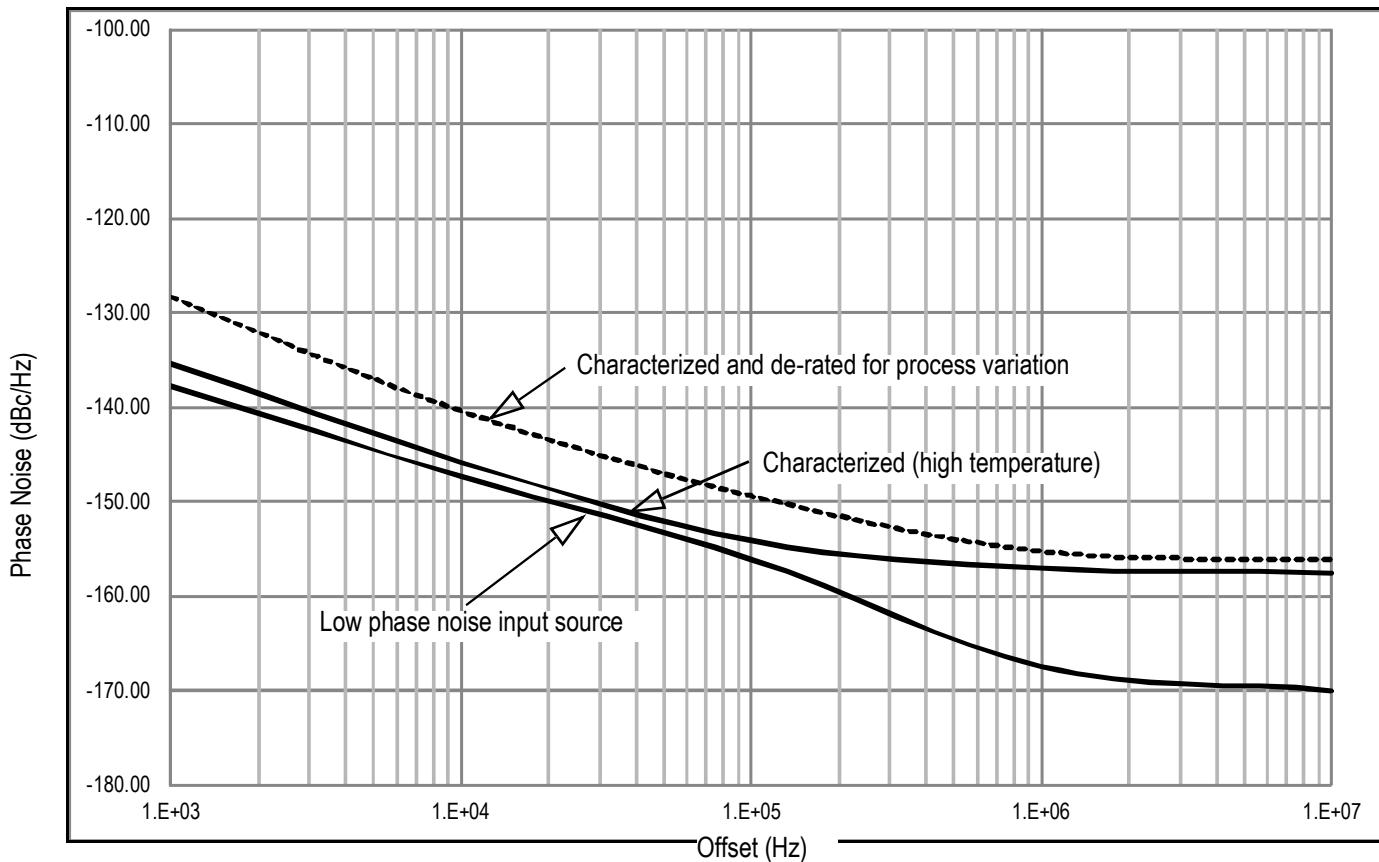
b. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

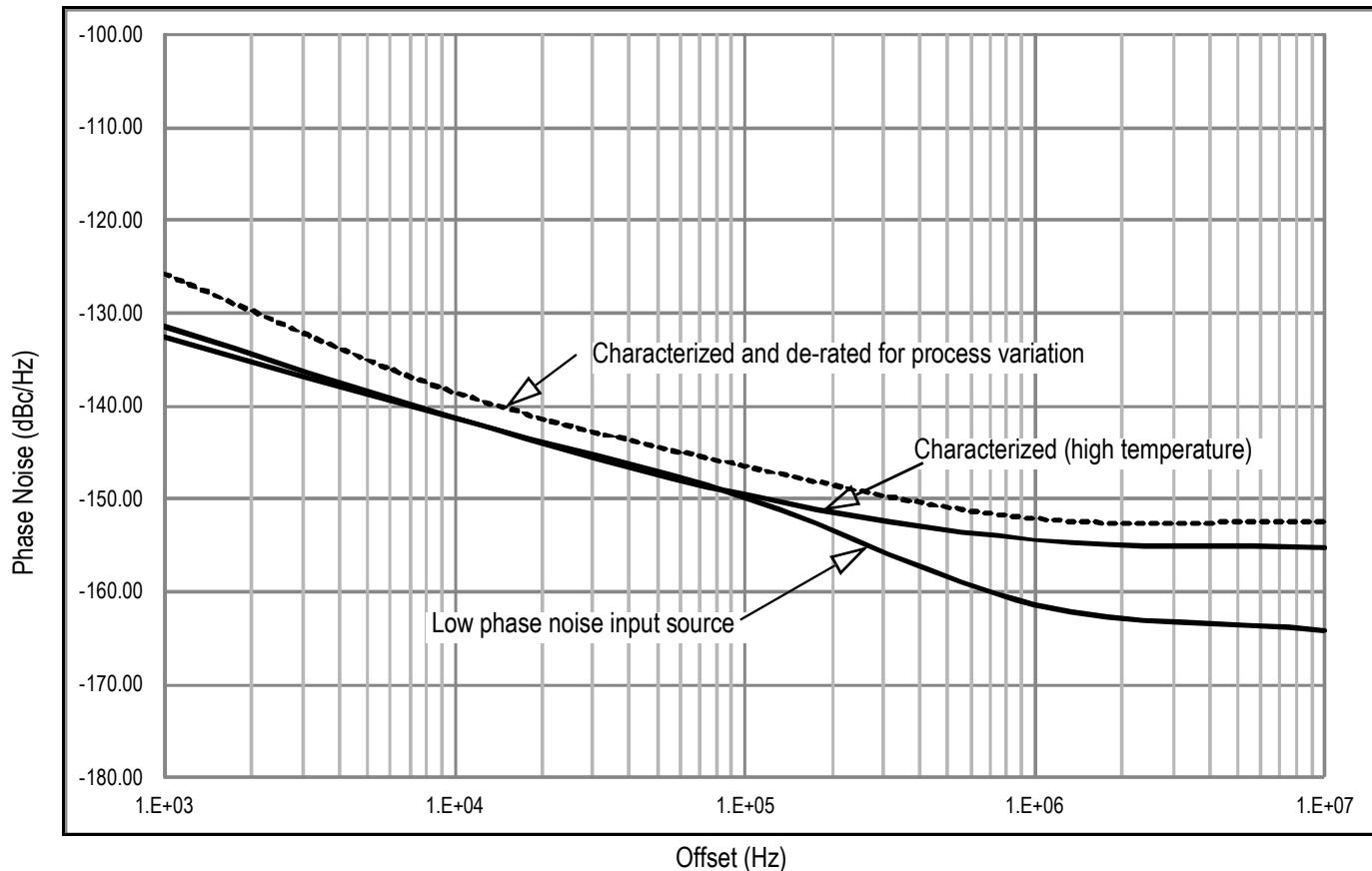
c. Measured results at the max. temperature of 85°C using an input source with a phase noise characteristics of:

- 245.76MHz: -143.7dBc/Hz (1kHz offset), -152.5dBc/Hz (10kHz), -160.8dBc/Hz (100kHz), -172.6dBc/Hz (1MHz), -179.5dBc/Hz (10MHz).
- 491.52MHz: -137.7dBc/Hz (1kHz offset), -147.4dBc/Hz (10kHz), -156.1dBc/Hz (100kHz), -167.6dBc/Hz (1MHz), -170.1dBc/Hz (10MHz).
- 983.04MHz: -132.5dBc/Hz (1kHz offset), -141.4dBc/Hz (10kHz), -149.9dBc/Hz (100kHz), -161.4dBc/Hz (1MHz), -164.2dBc/Hz (10MHz).

d. De-rating factor applied to the characterized data at 85°C to account for worst-case process variation.

**Figure 9: Additive Clock Phase Noise Characteristics (Measured),  $f_{OUT} = 245.76\text{MHz}$** 

**Figure 10: Additive Clock Phase Noise Characteristics (Measured),  $f_{\text{OUT}} = 491.52\text{MHz}$** 

**Figure 11: Additive Clock Phase Noise Characteristics (Measured),  $f_{\text{OUT}} = 983.04\text{MHz}$** 

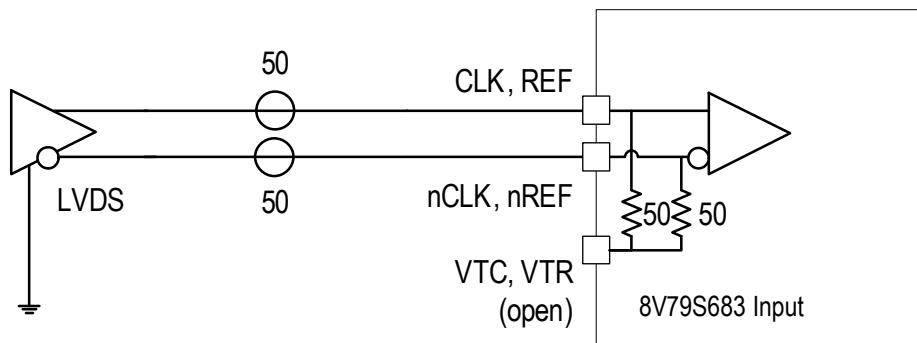
Symbol	Parameter		Test Conditions	Typical	Units
$\Phi_N(1\text{k})$	QREF_r	15.36MHz <sup>a</sup>	1kHz offset from Carrier	-146	dBc/Hz
$\Phi_N(10\text{k})$			10kHz offset from Carrier	-152.5	dBc/Hz
$\Phi_N(100\text{k})$			100kHz offset from Carrier	-156	dBc/Hz
$\Phi_N(1\text{M})$			1MHz offset from Carrier	-156	dBc/Hz
$\Phi_N(1\text{k})$		30.72MHz <sup>c</sup>	1kHz offset from Carrier	-147.5	dBc/Hz
$\Phi_N(10\text{k})$			10kHz offset from Carrier	-153.5	dBc/Hz
$\Phi_N(100\text{k})$			100kHz offset from Carrier	-155.5	dBc/Hz
$\Phi_N(1\text{M})$			1MHz offset from Carrier	-155.5	dBc/Hz

a. Measured results with  $\text{DLC}[1:0] = 00$  and  $\Phi_{\text{REF\_r}} = 3$ .

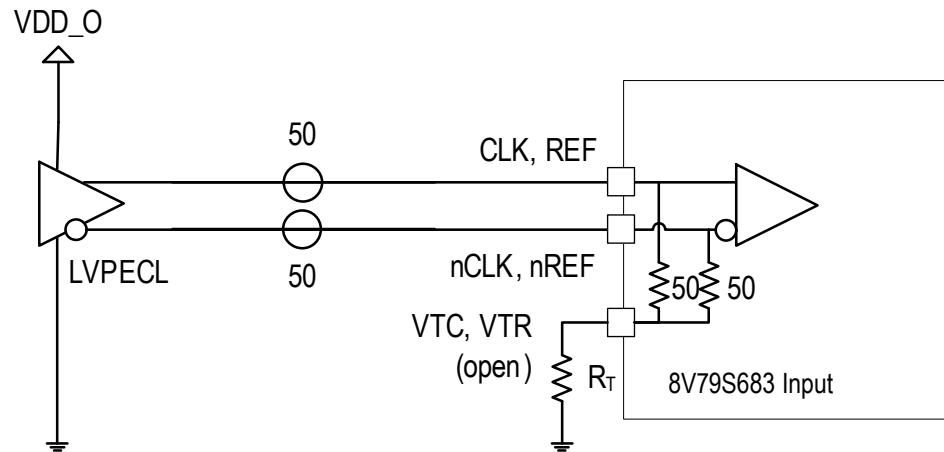
## Application Information

### Input Interface Circuits

**Figure 12: LVDS Output Drives 8V79S683 Input with Integrated Termination Resistor (DC-Coupled)**



**Figure 13: LVPECL Output Drives 8V79S683 Input with Integrated Termination Resistor (DC-Coupled)**



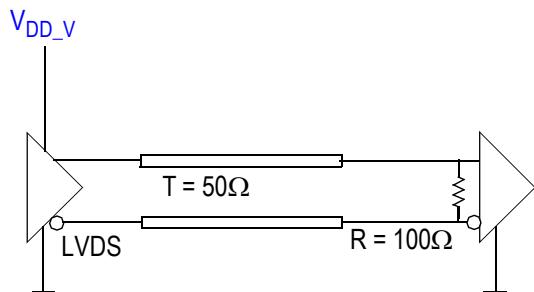
**Table 37: Termination Resistors**

	$V_{DD\_O} = 2.5V$	$V_{DD\_O} = 3.3V$
$R_T$	18Ω	50Ω

### Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 14 shows an example termination for the QCLK\_y, QREF\_r LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 14 is applicable for any output amplitude setting specified in Table 9.

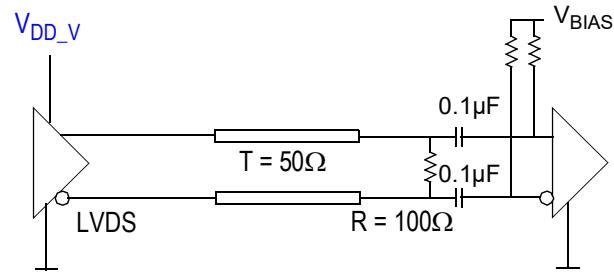
**Figure 14: LVDS (STYLE = 0) Output Termination**



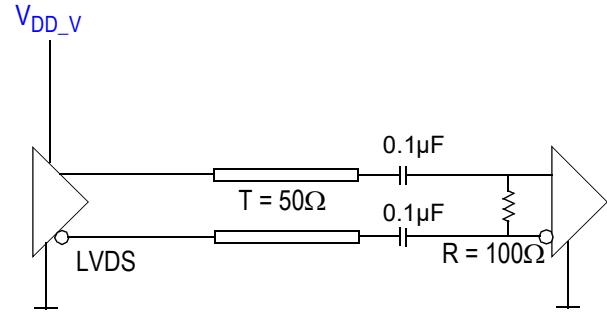
## AC Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 15 and Figure 16 show example AC terminations for the QCLK\_y, QREF\_r LVDS outputs. In the examples, the characteristic transmission line impedance is  $50\Omega$ . In Figure 15, the termination resistor  $R$  ( $100\Omega$ ) is placed at the line end. No external termination resistor is required if  $R$  is an internal part of the receiver circuit, which is shown in Figure 16. The LVDS terminations in both Figure 15 and Figure 16 are applicable for any output amplitude setting specified in Table 9. The receiver input should be re-biased according to its common mode range specifications.

**Figure 15: LVDS (STYLE = 0) AC Output Termination**



**Figure 16: LVDS (STYLE = 0) AC Output Termination**



## Termination for QCLK\_y, QREF\_r LVPECL Outputs (STYLE = 1)

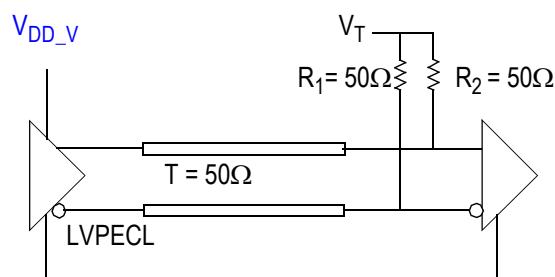
Figure 17 shows an example termination for the QCLK\_y, QREF\_r LVPECL outputs. In this example, the characteristic transmission line impedance is  $50\Omega$ . The  $R_1$  ( $50\Omega$ ) and  $R_2$  ( $50\Omega$ ) resistors are matched load terminations. The output is terminated to the termination voltage  $V_T$ . The  $V_T$  must be set according to the output amplitude setting defined in Table 9. The termination resistors must be placed close at the line end.

**Figure 17: LVPECL (STYLE = 1) Output Termination**

$$V_T = V_{DD\_V} - 1.60V \text{ (350 mV Amplitude)}$$

$$V_T = V_{DD\_V} - 2.00V \text{ (750 mV Amplitude)}$$

$$V_T = V_{DD\_V} - 2.25V \text{ (1000mV Amplitude)}$$

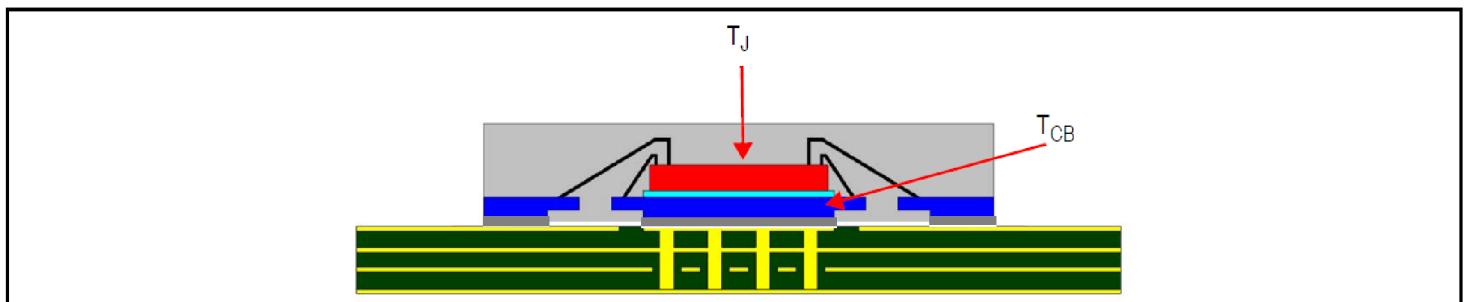


## Package Exposed Pad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in **Figure 18**. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Lead-frame Base Package, Amkor Technology.

**Figure 18: Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)**



## Thermal Characteristics

**Table 38: Thermal Resistance for 64-VFQFPN Package<sup>a</sup>**

Symbol	Thermal Parameter	Condition	Value	Unit
$\Theta_{JA}$	Junction to ambient	0 m/s air flow	22.76	°C/W
		1 m/s air flow	19.25	°C/W
		2 m/s air flow	17.70	°C/W
		3 m/s air flow	16.87	°C/W
		4 m/s air flow	16.37	°C/W
		5 m/s air flow	16.03	°C/W
$\Theta_{JC}$	Junction to case		14.33	°C/W
$\Theta_{JB}$	Junction to board		1.1	°C/W

a. Standard JEDEC 2S2P multilayer PCB.

### Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter  $\Psi_{JB}$  (Psi-JB) to calculate the junction temperature ( $T_J$ ) and ensure it does not exceed the maximum allowed operating junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter,  $\Psi_{JB}$ , is calculated using the following equation:

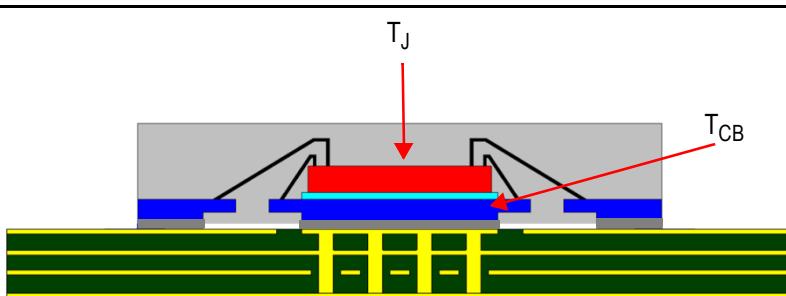
$$T_J = T_{CB} + \Psi_{JB} \times P_D, \text{ where:}$$

$T_J$  = Junction temperature at steady state condition in (°C)

$T_{CB}$  = Case temperature (Bottom) at steady state condition in (°C)

$\Psi_{JB}$  = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board

$P_D$  = power dissipation (W) in desired operating configuration



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ( $T_{CB}$ ). A good connection ensures that temperature at the exposed pad ( $T_{CB}$ ) and the board temperature ( $T_B$ ) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

**Example Calculation for Junction Temperature ( $T_J$ ):  $T_J = T_{CB} + \Psi_{JB} \times P_D$** **Table 39: Thermal Resistance for 64-VFQFPN package<sup>a</sup>**

Package type	64-VFQFPN
Body size (mm)	9 × 9 × 0.85 mm
ePad size (mm)	6.00 × 6.00 mm
Thermal Via	8 × 8 Matrix
$\Psi_{JB}$	1.1 C/W
$T_{CB}$	105°C
$P_D$	2.76W <sup>b</sup>

a. Standard JEDEC 2S2P multilayer PCB.

b. [See Table 27](#), test case 6.

For the variables above, the junction temperature is  $T_J = T_{CB} + \Psi_{JB} \times P_D = 105^\circ\text{C} + 1.1^\circ\text{C/W} \times 2.76\text{W} = 108^\circ\text{C}$ . Since this operating junction temperature is below the maximum operating junction temperature of 125°C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 108.6°C, this device can function without the degradation of the specified AC or DC parameters.

**Package Outline Drawings**

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

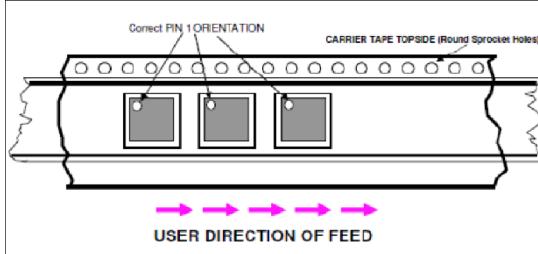
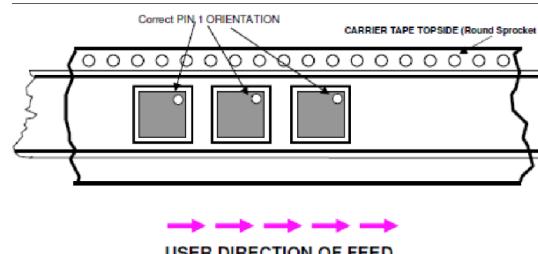
**Marking Diagram**

- Line 1 indicates the manufacturer.
- Line 2 indicates the part number.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.

## Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
8V79S683NLGI	RoHS 6/6 <b>64-VFQFPN</b>	3	Tray	-40°C to +85°C
8V79S683NLGI8		3	Tape and Reel, Pin 1 Orientation: EIA-481-C	
8V79S683NLGI/W		3	Tape and Reel, Pin 1 Orientation: EIA-481-D/E	

**Table 40: Pin 1 Orientation in Tape and Reel Packaging**

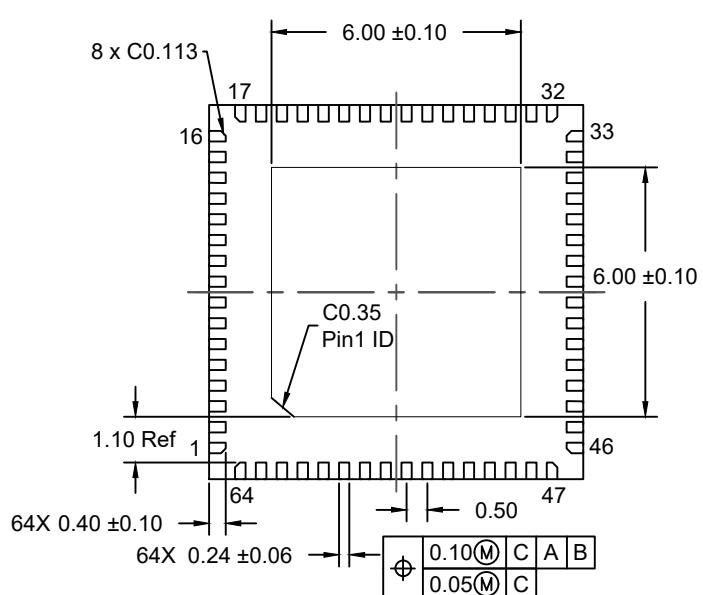
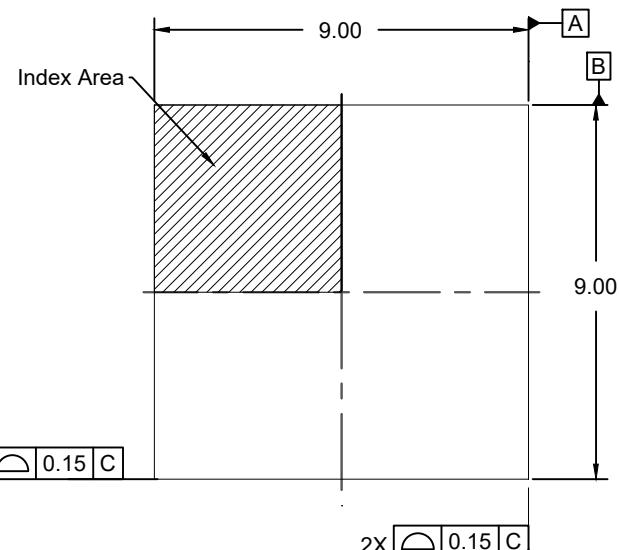
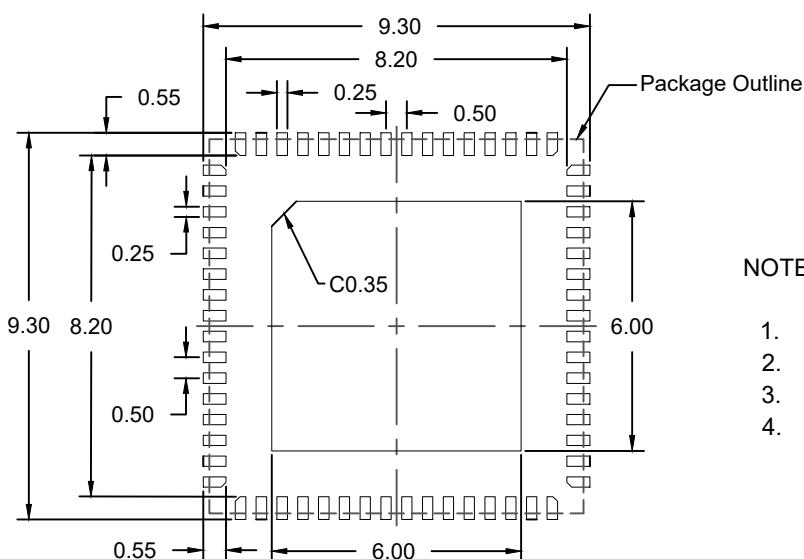
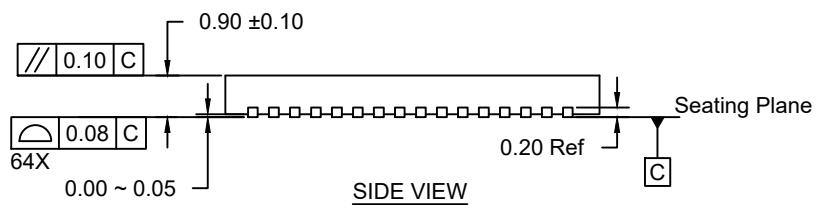
Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

## Glossary

Abbreviation	Description
Index $x$	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D.
Index $y$	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.
Index $r$	Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.
$V_{DD\_V}$	Denominates voltage supply pins. Range: $V_{DD\_QCLKA}$ , $V_{DD\_QREFA01}$ , $V_{DD\_QREFA2}$ , $V_{DD\_QCLKB}$ , $V_{DD\_QREFB}$ , $V_{DD\_QCLKC}$ , $V_{DD\_QREFC}$ , $V_{DD\_QCLKD}$ , $V_{DD\_QREFD}$ , $V_{DD\_CLK}$ , $V_{DD\_REF}$ .
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{...}	List of discrete values.

## Revision History

Date	Description of Change
September 13, 2021	Updated $V_{CMR}$ minimum voltage to '1'.
July 18, 2019	Initial release.


TOP VIEW
BOTTOM VIEW

**NOTES:**

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

RECOMMENDED LAND PATTERN  
 (PCB Top View, NSMD Design)

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