

TPS72518EVM-207

**1-Amp, Low Input Voltage, Low Dropout Linear
Regulator EVM**

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.1 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation and use of the TPS72518EVM-207 1-A low input voltage, low dropout linear regulator evaluation module (EVM). The user's guide includes a schematic diagram, printed-circuit board (PCB) layouts, and bill of materials. electronic PCB layout files are available upon request.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Test Setup
- Chapter 3 – Board Layout
- Chapter 4 – Schematic and Bill of Materials

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This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

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Related Documentation From Texas Instruments

SLVS341 – TPS725xx data sheet, literature number

SLVS403 – TPS726xx data sheet, literature number

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

Introduction

This chapter contains background information for the TPS725xx and TPS726xx families of devices and support documentation for the TPS72518EVM-207 evaluation module. The EVM performance specifications are also given.

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1.1 Background

The purpose of the TPS72518EVM is to facilitate evaluation of the TPS725xx and TPS726xx families of devices. The TPS72518EVM consists of the SLVP207 PCB, one TPS72518 1.8-V, 1-A linear regulator in a TO-263 package, and supporting passive components. The SLVP207 PCB is designed to accommodate multiple devices with similar pinouts in different packages (i.e., TO-220, TO-263, or SOT-223). Specifically, in addition to the TPS725xx and TPS726xx families, the SLVP207 can be used with the UCx82, UCx85, TPS755xx, TPS756xx, TPS757xx, TPS758xx, TPS759xx, TPS786xx, TPS795xx, and TPS796xx families as well as any other device in the same package with the same pinout.

The TPS725xx and TPS726xx family of parts feature 1-A output current, and an active high reset (RST) signal that goes high following a fixed delay when the output voltage reaches 95% of its regulated voltage. Additional features, as well as detailed specifications of the two families of regulators, can be found in the TPS725xx data sheet (SLVS341) and the TPS726xx data sheet (SLVS403).

1.2 Performance Specification Summary

Table 1-1 provides a summary of the TPS72518EVM performance specifications

Table 1-1. Performance Specification Summary

| Specification | Test Conditions | Min | Typ | Max | Unit |
|----------------------|-----------------|-----|-----|-----|------|
| Input voltage | | 2.1 | 5.5 | | V |
| Output voltage | | | 1.8 | | V |
| Output current range | | 0 | | 1 | A |

1.3 Modifications

The TPS72518EVM is designed to allow parts to be easily interchanged. Although the EVM is designed with a TPS72518 regulator in a TO-263 package, the SLVP207 EVM board also accommodates the SOT-223 packaged version of the device or any other fixed or adjustable voltage option of TPS725xx or TPS726xx. Passive elements such as the output capacitors (C4, C5, and C6) and the input capacitor (C3) are easily changed. The board accommodates the TPS72501 or TPS72601 adjustable versions with resistors R3 and R4 used as the feedback resistors. Capacitor C2 is used to reduce the inductance from long input supply leads and may or may not be necessary, depending on the specific test setup. With JP1 open, the device is enabled. Shorting JP1 disables the device.

Chapter 2

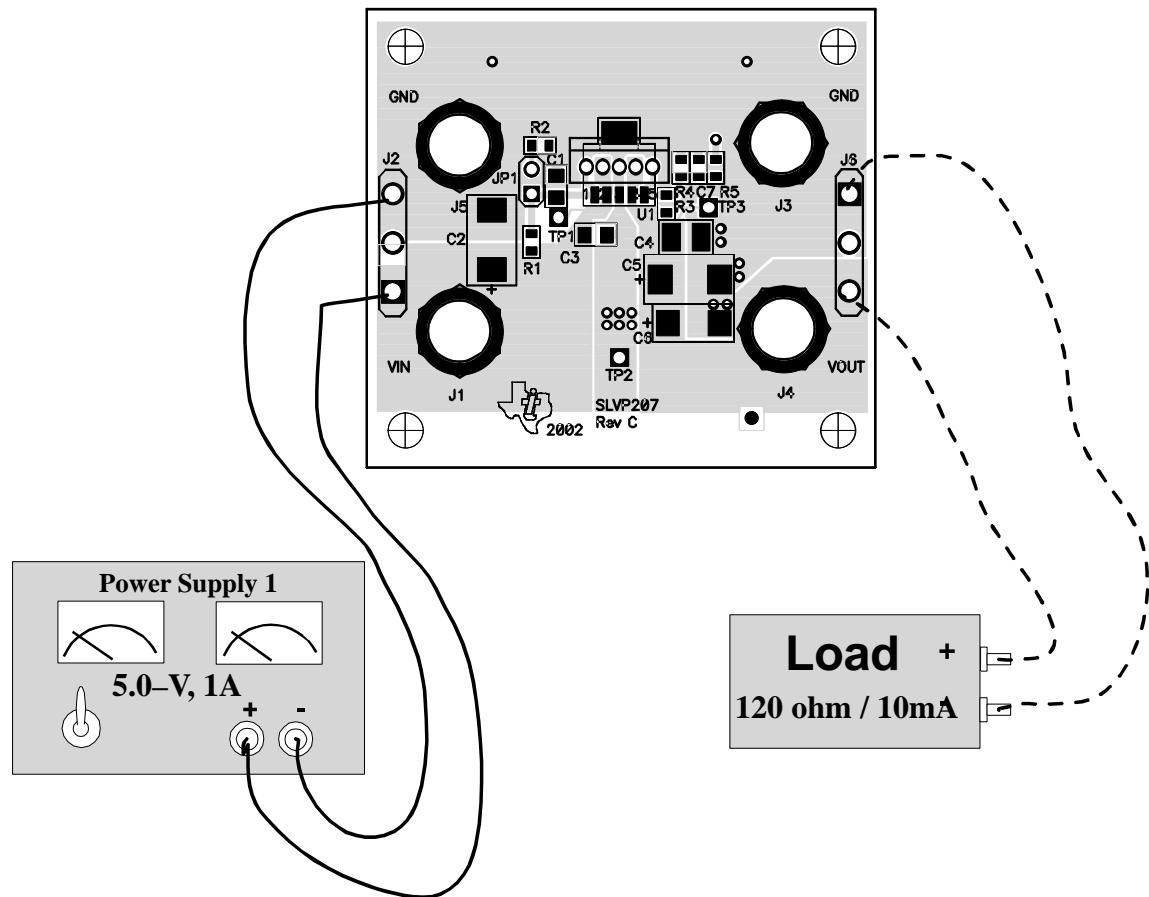
Test Setup

This chapter describes how to properly connect, and setup the TPS72518EVM.

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2.1 Test Setup for DC Testing

Figure 2-1. Test Setup for DC Testing



Chapter 3

Board Layout

This chapter provides a description of the SLVP207 board layout and layer illustrations used in the TPS72518EVM.

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3.1 Layout

The EVM PCB consists of two layers of 1.5 oz. copper. The top side (component) layout of the EVM is shown in Figure 3-1. Large power and ground planes are used to minimize trace resistance. The input capacitor (C3) is located close to the input pin. Proper board layout is critical to ensure the best noise and PSRR performance. The ground of the output capacitor (C4) is close to the board's ground connection for improved transient response, and the bypass capacitor's (C7) ground has a low impedance connection to the IC's ground connection. The top and bottom side layouts are shown in Figures 3-2 and 3-3 respectively.

Figure 3-1. Top Side Assembly

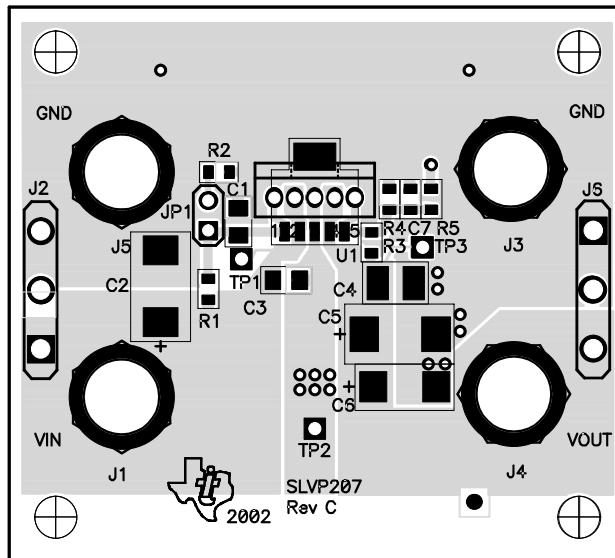


Figure 3-2. Bottom Side Assembly

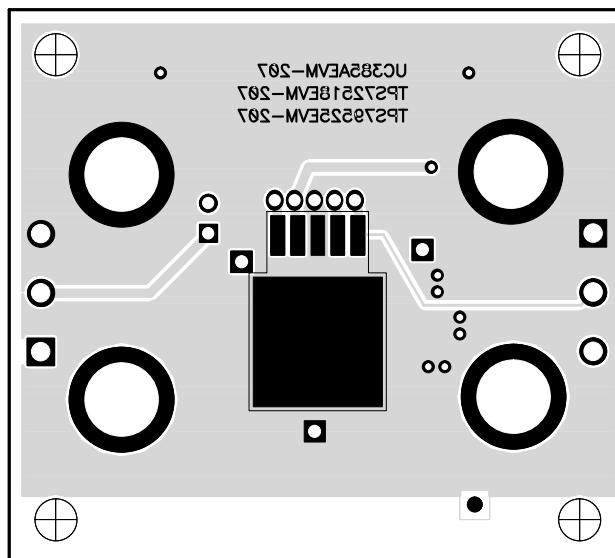


Figure 3–3. Top Side Layout

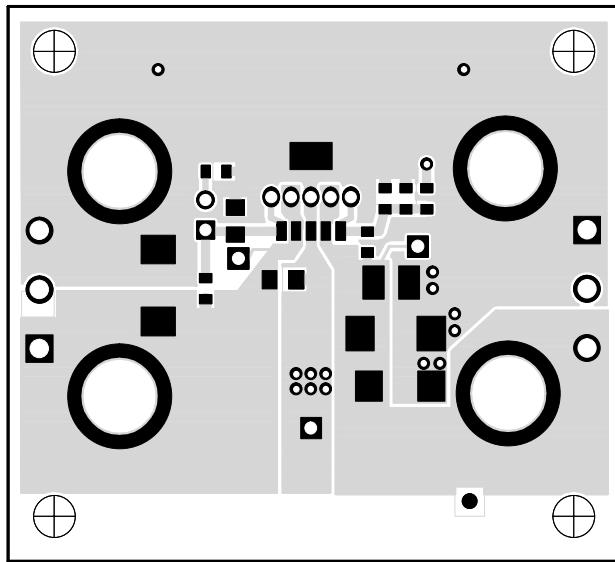
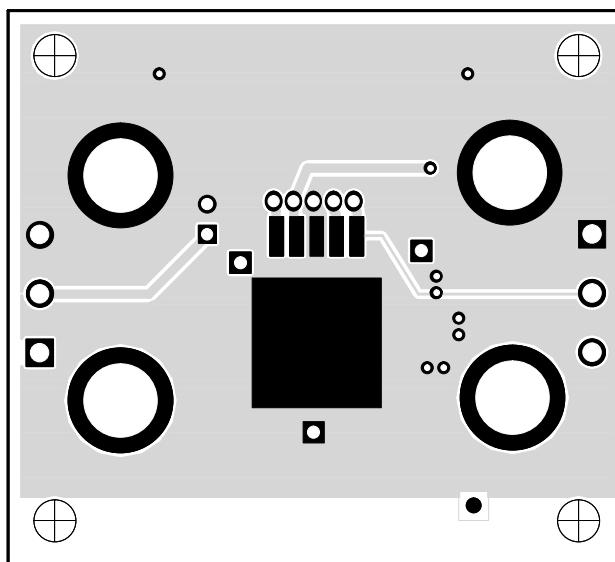


Figure 3–4. Bottom Side Layout



Chapter 4

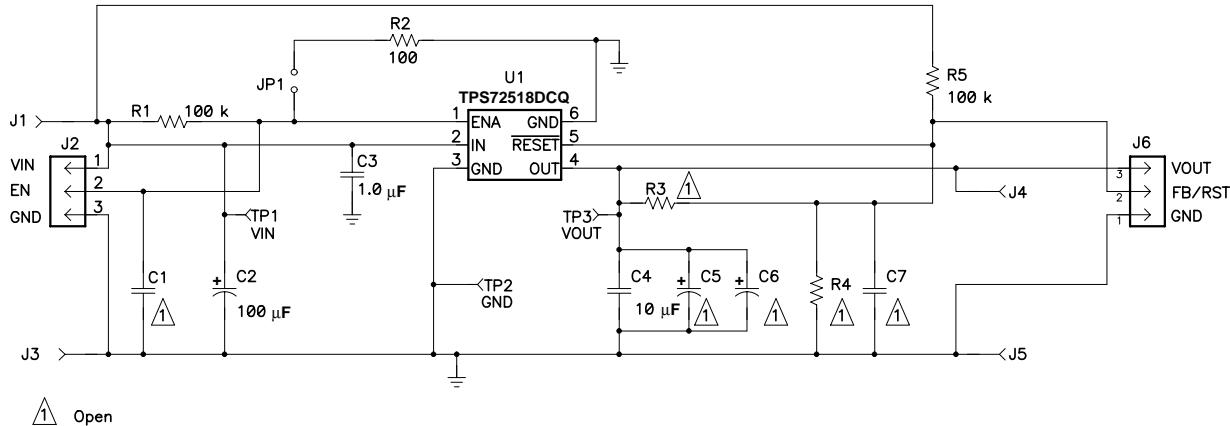
Schematic and Bill of Materials

The EVM schematic and bill of materials are presented in this chapter.

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4.1 Schematic

Figure 4–1. Schematic



4.2 Bill of Materials

Table 4–1. Bill of Materials

| Qty | Ref Des | Description | Size | Mfr | Part Number |
|-----|----------------|--|------------|------------|-------------------|
| 1 | C1 | Open | 805 | | |
| 1 | C2 | Capacitor, POSCAP, 100 μ F, 10 V, 55 m Ω , 20% | 7343 (D) | Sanyo | 10TPB100M |
| 1 | C3 | Capacitor, ceramic, 1 μ F, 10 V, X7R, 10% | 805 | Murata | GRM21BR71C105KA01 |
| 1 | C4 | Capacitor, ceramic, 10 μ F, 6.3 V, X5R, 20% | 1210 | Murata | GRM31CR60J106KC01 |
| 1 | C5 | Open | 7343 (D) | | |
| 1 | C6 | Open | 6032 (C) | | |
| 1 | C7 | Open | 603 | | |
| 4 | J1, J3, J4, J5 | Connector, mini banana jack, uninsulated, 4-mm inside diameter | 0.300 OD | Hirschmann | B0 10 |
| 2 | J2, J6 | Header, 3 pin, 5-mm spacing | 0.197 x 3" | OST | ED1661 |
| 1 | JP1 | Header, 2 pin, 100-mil spacing, (36-pin strip) | 0.100 x 2" | Sullins | PTC36SAAN |
| 2 | R1, R5 | Resistor, chip, 100 k Ω , 1/16 W, 1% | 603 | Std | Std |
| 1 | R2 | Resistor, chip, 100 Ω , 1/16 W, 1% | 603 | Std | Std |
| 2 | R3, R4 | Open | 603 | | |
| 2 | TP1, TP3 | Test point, red, 1 mm | 0.038" | Farnell | 240-345 |
| 1 | TP2 | Test point, black, 1 mm | 0.038" | Farnell | 240-333 |
| 1 | U1 | IC, LDO with supervisor, 1.8 V, 1 A | SOT-223 | TI | TPS72518DCQ |
| 1 | | PCB, 2.055" x 1.85 " x 0.62" | | Any | SLVP207 |
| 1 | | Shunt, black, 100 mm | 0.100 | 3M | 929950-00 |