AT24CSW01X/AT24CSW02X

I²C-Compatible (Two-Wire) Serial EEPROM with a Security Register and Software Write Protection 1-Kbit (128 x 8), 2-Kbit (256 x 8)

Features

- Low-Voltage Operation:
  - V_{CC} = 1.7V to 3.6V
- Internally Organized as 128 x 8 (1K) or 256 x 8 (2K)
- Software Write Protection of the EEPROM Array:
  - Five configuration options
  - Protection settings can be made permanent
- 256-Bit Security Register:
  - Preprogrammed 128-bit serial number
  - Additional 16 bytes of free user EEPROM provided to store critical user data
- Factory Set Hardware Client Address:
  - Unique ordering code for each available client address value (AT24CSW01X/AT24CSW02X)
- Industrial Temperature Range: -40°C to +85°C
- I²C-Compatible (Two-Wire) Serial Interface:
  - 100 kHz Standard Mode, 1.7V to 3.6V
  - 400 kHz Fast Mode, 1.7V to 3.6V
  - 1 MHz Fast Mode Plus (FM+), 1.7V to 3.6V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Ultra Low Active Current (1 mA maximum) and Standby Current (0.8 µA maximum)
- 8-Byte Page Write Mode:
  - Partial page writes allowed
- Random and Sequential Read Modes
- Self-Timed Write Cycle within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green Package Options (Lead-free/Halide-free/RoHS compliant)
- Die Sale Option: Wafer Form

Packages

- 5-Lead SOT23 and 4-Ball Ultra-Thin WLCSP

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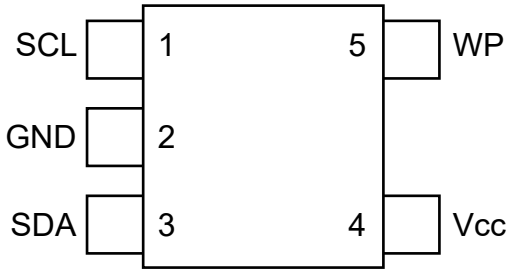
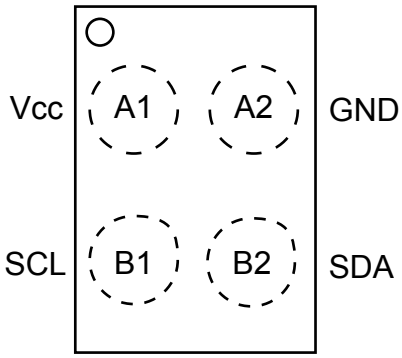
1. Package Types (not to scale)

5-lead SOT23
(Top View)



4-ball WLCSP
(Top View)



2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	5-Lead SOT23	4-Ball WLCSP	Function
SCL	1	B1	Serial Clock
GND	2	A2	Ground
SDA	3	B2	Serial Data
V_{CC}	4	A1	Device Power Supply
WP(1)	5	—	Write-Protect

Note:

1. If the WP pin is not driven, it is internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once this pin is biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting this pin to a known state whenever possible.

2.1 Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

2.2 Ground (GND)

The ground reference for the Device Power Supply (V_{CC}). The Ground (GND) pin should be connected to the system ground.

2.3 Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.4 Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

2.5 Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to V_{CC}, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the WP pin to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

Table 2-2. Write-Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array and Security Register
At GND	Normal Write Operations

3. Description

The AT24CSW01X/AT24CSW02X provides 1,024/2,048 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 128/256 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The device features a software write protection feature with five different programmable levels of protection for the EEPROM array. The protection settings of the device can be made permanent, if desired. Safeguards are included to prevent accidental invocation of the permanent feature.

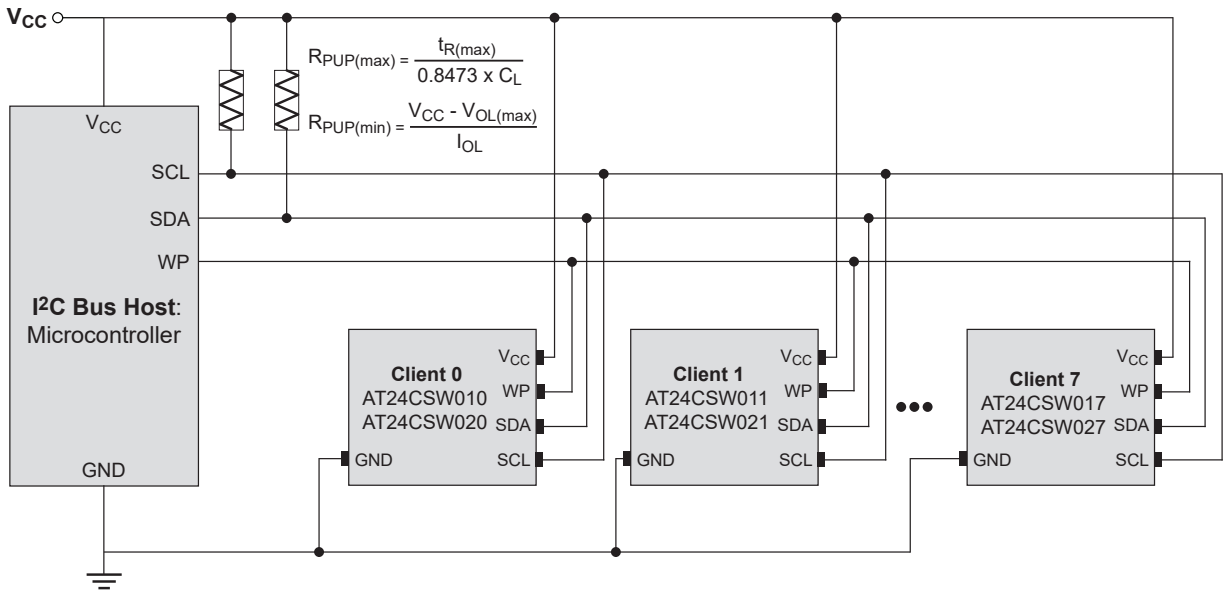
Additionally, each device includes a Security register with an extra 256 bits of EEPROM beyond the nominal EEPROM array. The Security register is comprised of a read-only section of 16 bytes and an additional user-programmable section of 16 bytes.

The Security register begins with a read-only section that contains a factory programmed, ensured unique 128-bit serial number. The time-consuming step of performing and ensuring true serialization of a product on a manufacturing line can be removed from the production flow by employing a CS or CSW Series Serial EEPROM. The 128-bit serial number is programmed and permanently locked from future writing during the Microchip production process. Further, this 128-bit location does not consume any of the user read/write area of the 1-Kbit or 2-Kbit Serial EEPROM. The uniqueness of the serial number is ensured across the entire CS or CSW Series of Serial EEPROMs, regardless of the size of the memory array or the type of interface protocol. This means that as an application's needs for memory size or interface protocol evolve in future generations, any previously deployed serial number from any CS or CSW Series Serial EEPROM part will remain valid.

Following the 128-bit read-only serial number in the Security register is an additional 16 bytes of EEPROM organized as two pages of 8 bytes each. This region of the Security register is user-programmable and, if desired, can later be permanently write protected with a software sequence. This user-programmable section of the Security register is ideal for applications that need to irreversibly protect critical or sensitive application data.

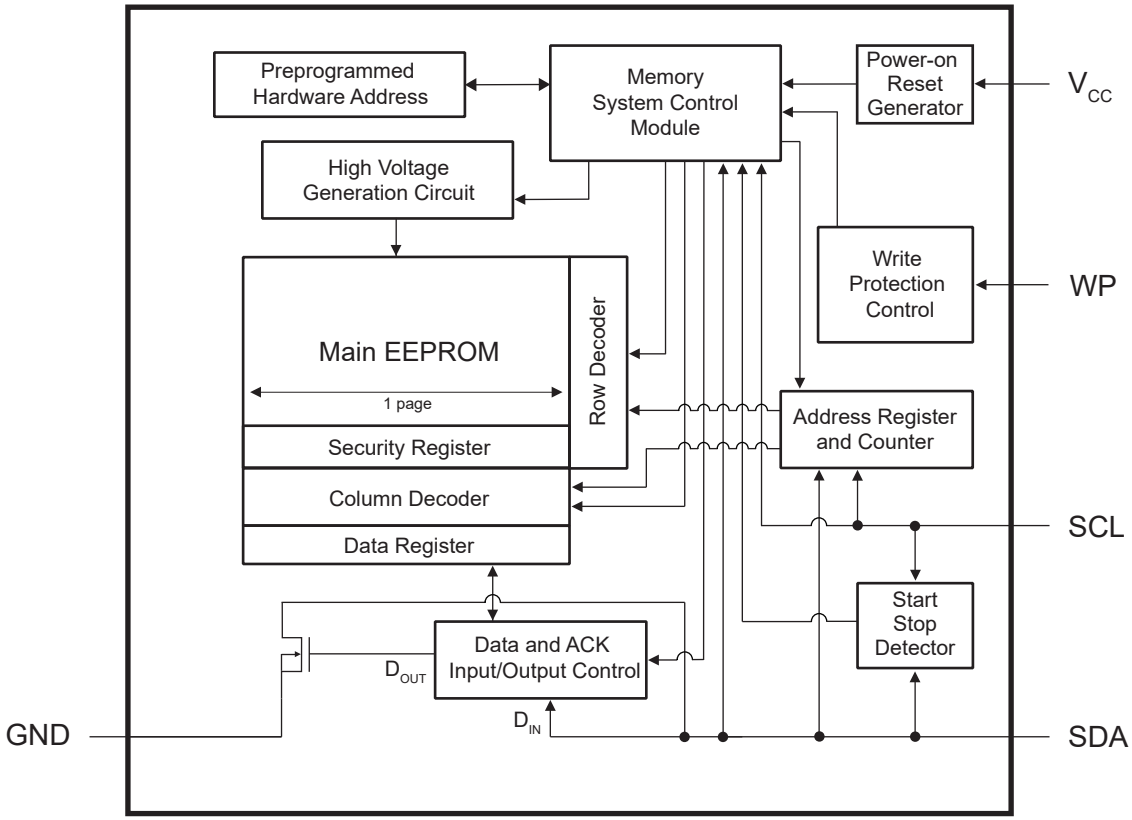
The AT24CSW01X/AT24CSW02X is available in 5-lead SOT23 and best-in-class 4-ball Ultra-Thin WLCSP packages and is accessed via an I^2C-compatible two-wire serial interface. Other package options are available upon request. The device operates with a supply voltage ranging from 1.7V to 3.6V.

3.1 System Configuration Using Two-Wire Serial EEPROMs



Note: The WP pin is only available on the 5-lead SOT23 package.

3.2 Block Diagram



Note: The WP pin is only available on the 5-lead SOT23 package.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	4.1V
Voltage on any pin with respect to ground	-0.6V to V_{CC}+0.5V
DC output current	5.0 mA
ESD protection	> 4 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT24CSW01X/AT24CSW02X		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low-Voltage Grade	1.7V to 3.6V

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Typical(1)	Maximum	Units	Test Conditions
Supply Voltage	V_{CC}	1.7	—	3.6	V	
Supply Current	I_{CC1}	—	0.08	0.3	mA	V_{CC} = 1.8V(2), Read at 400 kHz
		—	0.15	0.5	mA	V_{CC} = 3.6V, Read at 1 MHz
Supply Current	I_{CC2}	—	0.20	1.0	mA	V_{CC} = 3.6V, Write at 1 MHz
Standby Current	I_{SB}	—	0.08	0.4	µA	V_{CC} = 1.8V(2), V_{IN} = V_{CC} or GND
		—	0.10	0.8	µA	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND
Input Leakage Current	I_{LI}	—	0.10	3.0	µA	V_{IN} = V_{CC} or GND
Output Leakage Current	I_{LO}	—	0.05	3.0	µA	V_{OUT} = V_{CC} or GND
Input Low Level	V_{IL}	-0.6	—	V_{CC} x 0.3	V	Note 2
Input High Level	V_{IH}	V_{CC} x 0.7	—	V_{CC} + 0.5	V	Note 2
Output Low Level	V_{OL1}	—	—	0.2	V	V_{CC} = 1.8V, I_{OL} = 0.15 mA

.....continued						
Parameter	**Symbol**	**Minimum**	**Typical(1)**	**Maximum**	**Units**	**Test Conditions**
Output Low Level	V_{OL2}	—	—	0.4	V	V_{CC} = 3.0V, I_{OL} = 2.1 mA

Notes:

1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

4.4 AC Characteristics

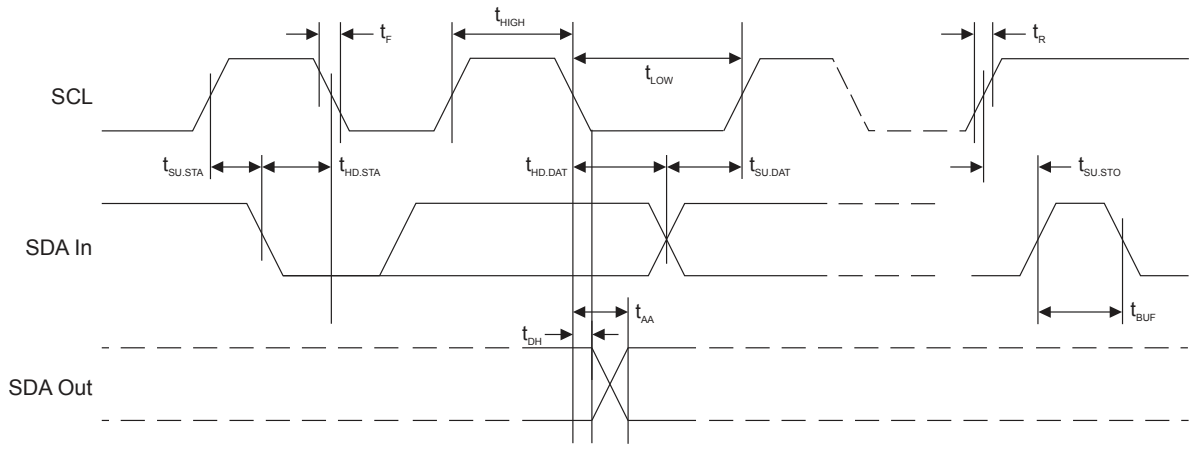
Table 4-3. AC Characteristics(1)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Units
		V_{CC} = 1.7V to 3.6V		V_{CC} = 1.7V to 3.6V		V_{CC} = 1.7V to 3.6V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency, SCL	f_{SCL}	—	100	—	400	—	1000	kHz
Clock Pulse Width Low	t_{LOW}	4,700	—	1,300	—	500	—	ns
Clock Pulse Width High	t_{HIGH}	4,000	—	600	—	400	—	ns
Input Filter Spike Suppression (SCL,SDA)(2)	t_I	—	100	—	100	—	100	ns
Clock Low to Data Out Valid	t_{AA}	—	4,500	—	900	—	450	ns
Bus Free Time between Stop and Start(2)	t_{BUF}	4,700	—	1,300	—	500	—	ns
Start Hold Time	$t_{HD.STA}$	4,000	—	600	—	250	—	ns
Start Set-up Time	$t_{SU.STA}$	4,700	—	600	—	250	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	0	—	0	—	ns
Data In Set-up Time	$t_{SU.DAT}$	200	—	100	—	100	—	ns
Inputs Rise Time(2)	t_R	—	1,000	—	300	—	100	ns
Inputs Fall Time(2)	t_F	—	300	—	300	—	100	ns
Stop Set-up Time	$t_{SU.STO}$	4,700	—	600	—	250	—	ns
Write-Protect Setup Time	$t_{SU.WP}$	4,000	—	600	—	100	—	ns
Write-Protect Hold Time	$t_{HD.WP}$	4,000	—	600	—	400	—	ns
Data Out Hold Time	t_{DH}	100	—	50	—	50	—	ns
Write Cycle Time	t_{WR}	—	5	—	5	—	5	ms

Notes:

1. AC measurement conditions:
   - C_L: 100 pF
   - R_{PUP} (SDA bus line pull-up resistor to V_{CC}): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz), 10 kΩ (100 kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤50 ns
   - Input and output timing reference voltages: 0.5 x V_{CC}
2. These parameters are determined through product characterization and are not 100% tested in production.

Figure 4-1. Bus Timing



4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT24CSW01X/AT24CSW02X should monotonically rise from GND to the minimum V_{CC} level (as specified in Table 4-1), with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT24CSW01X/AT24CSW02X includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus host must wait at least t_{PUP} before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions(1)

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	1	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT24CSW01X/AT24CSW02X drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed. First, drive the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then perform a new power-up sequence in compliance with the requirements defined in this section.

4.5.2 Pin Capacitance

Table 4-5. Pin Capacitance(1)

Symbol	Test Condition	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.

4.5.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	T_A = +25°C, V_{CC} (min.) < V_{CC} < V_{CC} (max.), Byte or Page Write mode	1,000,000	—	Write Cycles
Data Retention(1)	T_A = +55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

5. Device Operation and Communication

The AT24CSW01X/AT24CSW02X operates as a client device and utilizes a simple I^2C-compatible two-wire digital serial interface to communicate with a host controller, commonly referred to as the bus host. The host initiates and controls all read and write operations to the client devices on the serial bus, and both the host and the client devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the host, while the bidirectional SDA pin is used to receive command and data information from the host as well as to send data back to the host. Data is always latched into the AT24CSW01X/AT24CSW02X on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the host. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the host and the client devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the host. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic high state at the same time.

5.1 Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT24CSW01X/AT24CSW02X are shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in AC Characteristics.

5.2 Start and Stop Conditions

5.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state and will bring the device out of Standby mode. The host uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 5-1 for more details.

5.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.

The host can use the Stop condition to end a data transfer sequence with the AT24CSW01X/AT24CSW02X, which will subsequently return to Standby mode. The host can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the host will perform another operation. Refer to Figure 5-1 for more details.

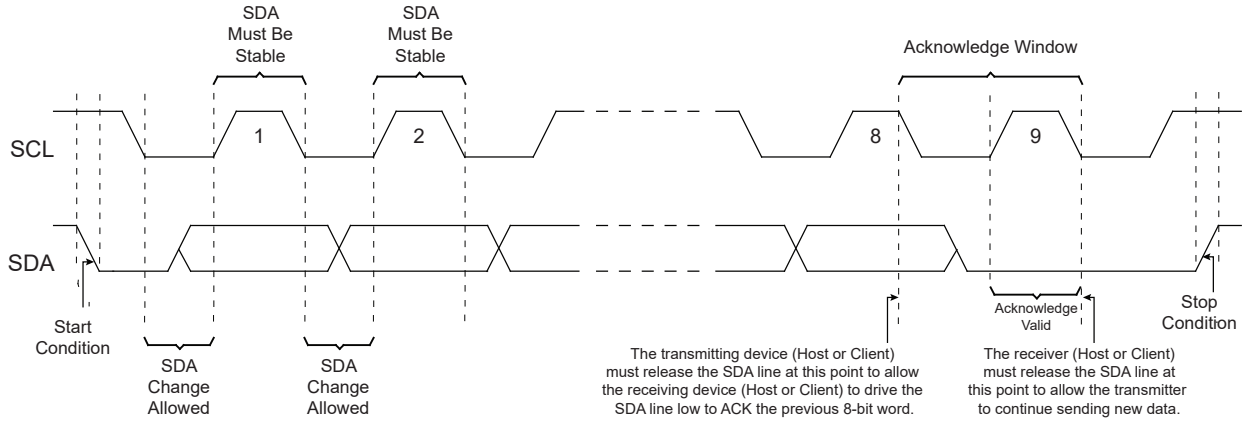
5.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a logic '0' during the entire high period of the ninth clock cycle.

When the AT24CSW01X/AT24CSW02X is transmitting data to the host, the host can indicate that it is done receiving data and wants to end the operation by sending a logic '1' response to the AT24CSW01X/AT24CSW02X instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished by the host sending a logic '1' during the ninth clock cycle, at which point the AT24CSW01X/AT24CSW02X will release the SDA line so the host can then generate a Stop condition.

The transmitting device, which can be the bus host or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 5-1 to better illustrate these requirements.

Figure 5-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



5.4 Standby Mode

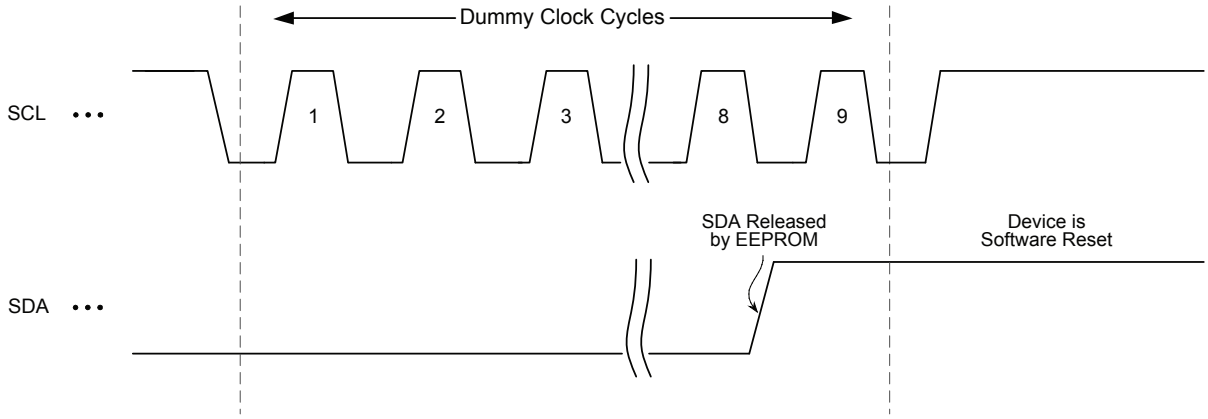
The AT24CSW01X/AT24CSW02X features a low-power Standby mode that is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).
- An unsuccessful match of the device type identifier or hardware address in the device address byte occurs (see Device Addressing).
- The bus host does not ACK the receipt of data read out from the device; instead it sends a NACK response (see Read Operations).

5.5 Software Reset

After an interruption in protocol, power loss or system Reset, any two-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.

Figure 5-2. Software Reset

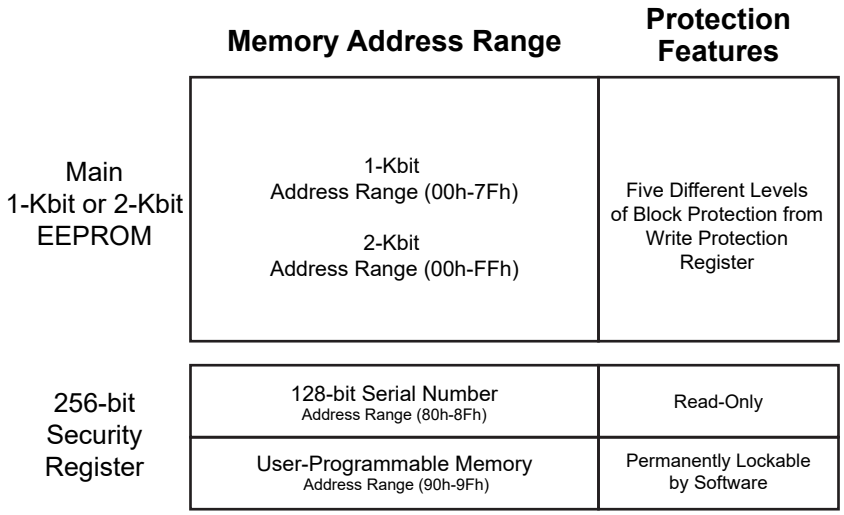


In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).

6. Memory Organization

The AT24CSW01X is internally organized as 16 pages of 8 bytes each. The AT24CSW02X is internally organized as 32 pages of 8 bytes each for the EEPROM Array. The device also contains a 32-byte Security register which is organized as four pages of eight bytes each. This register contains a factory programmed ensured unique 128-bit serial number in the lower 16 bytes. The upper 16 bytes are user-programmable and can (later) be permanently write protected (see Security Register).

Figure 6-1. Memory Organization



The AT24CSW01X/AT24CSW02X also contains an 8-bit Write Protection register that controls which regions of the memory can be written to. Details about how to use this register can be found in Write Protection.

6.1 Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple client devices can reside on the serial bus, each client device must have its own unique address so the host can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) for the main EEPROM access, or '1011' (Bh) for Security register and Write Protection register access is required in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier are the client address bits, A2, A1 and A0. The value that the AT24CSW01X/AT24CSW02X will ACK to is preprogrammed in each device. Unique ordering codes are available for each of the eight possible client combinations. The client address preprogrammed in the device is embedded in the base part number as shown in Table 6-2.

Access to the Security register memory location is similar to the main EEPROM region with the exception that the device address word must begin with '1011' (Bh). The behavior of the hardware address bits (A2, A1, A0) remains the same as during a EEPROM addressing sequence (see Table 6-2). While the lower order 16 bytes of the Security register are read-only, the device will ACK if this bit is a logic '0'. To read from the Security register, please refer to Read Operations in the Security Register. For writing, please refer to Write Operations in the Security Register.

Note: Accessing the Security register is only possible if any sequence or command to the EEPROM (if one has been sent) has been properly terminated with a NACK or Stop condition from the host. Without proper termination of that previous sequence, all communications with the Security register will not execute successfully.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT24CSW01X/AT24CSW02X will return an ACK. If a valid comparison is not made, the device will NACK.

Note: While the lower order 16 bytes of the Security register are read-only, the device will ACK if the Read/Write Select bit is a logic '0'.

Table 6-1. Device Address Byte

Memory Region	Device Type Identifier				Hardware Client Address Bits			R/$\overline{W}$ Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM Array	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Security Register and Write Protection Register	1	0	1	1	A2	A1	A0	R/$\overline{W}$

Table 6-2. Hardware Address Response by Part Number

Part Number Series		Hardware Address Bits		
1-Kbit	2-Kbit	A2	A1	A0
AT24CSW01**0**	AT24CSW02**0**	0	0	0
AT24CSW011(1)	AT24CSW021(1)	0	0	1
AT24CSW012(1)	AT24CSW022(1)	0	1	0
AT24CSW013(1)	AT24CSW023(1)	0	1	1
AT24CSW014(1)	AT24CSW024(1)	1	0	0
AT24CSW015(1)	AT24CSW025(1)	1	0	1
AT24CSW016(1)	AT24CSW026(1)	1	1	0
AT24CSW017(1)	AT24CSW027(1)	1	1	1

Note:

1. Contact your local sales representative for hardware client address availability.

For all operations other than a current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte contains a 7-bit (in the case of the AT24CSW01x) or 8-bit (in the case of the AT24CSW02x) memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 6-3 to review these bit positions.

When accessing the Security register, it is required that the A7 and A6 bits of the word address be set to '10' respectively. These bits are at a higher order address range than what is needed to address the 32 byte space (A4 through A0). It is recommended that all address bits that fall outside the address range that do not have other requirements be set to a logic '0'.

Table 6-3. Word Address Byte

Memory Region	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM Array	A7(1)	A6	A5	A4	A3	A2	A1	A0
Security Register	1	0	X	A4	A3	A2	A1	A0
Security Register Lock Function	0	1	1	0	X	X	X	X
Write Protection Register	1	1	X	X	X	X	X	X

Note:

1. Bit 7 is a "don't care" bit on the AT24CSW01x.

7. Write Operations

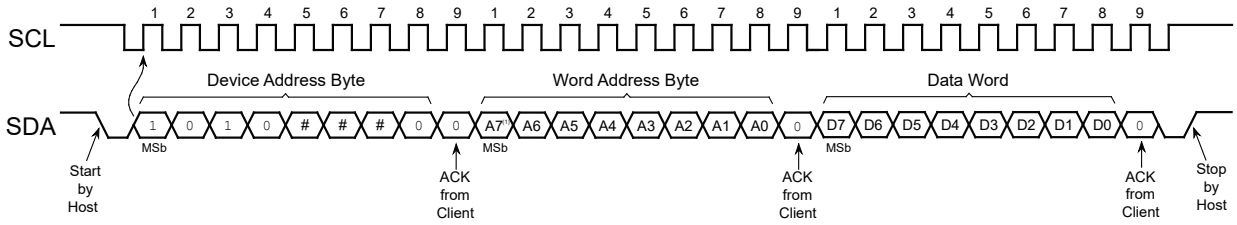
All write operations for the AT24CSW01X/AT24CSW02X begin with the host sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to logic '0' and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte. When writing to a protected region, the device will ACK but the internal write cycle will abort, leaving the device ready for the next operation.

7.1 Byte Write

The AT24CSW01X/AT24CSW02X supports the writing of a single 8-bit byte. Selecting a data word in the AT24CSW01X requires a 7-bit word address, while selecting a data word in the AT24CSW02X requires an 8-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an ACK. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus client, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within t_{WR}, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Figure 7-1. Byte Write



Notes:

1. The A7 bit falls outside of the addressable 1K range and is therefore a don't care value on an AT24CSW01x.
2. # indicates the hardware address value that is managed by the ordering code of the device (see Table 6-2).

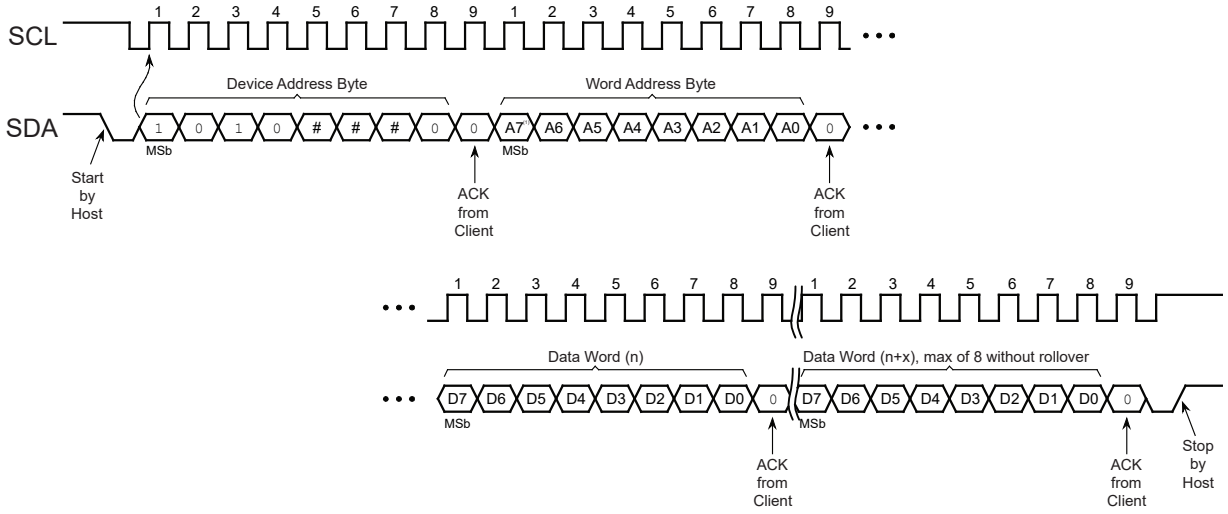
7.2 Page Write

A page write operation allows up to 8 bytes to be written in the same write cycle, provided all bytes are in the same row of the memory array (where address bits A7/A6 to A3 are the same). Partial page writes of less than 8 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus host does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus host can transmit up to seven additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus host must issue a Stop condition (see Figure 7-2), at which time the internally self-timed write cycle will begin.

The lower three bits of the word address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will rollover to the beginning of the same page. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 7-2. Page Write



Notes:

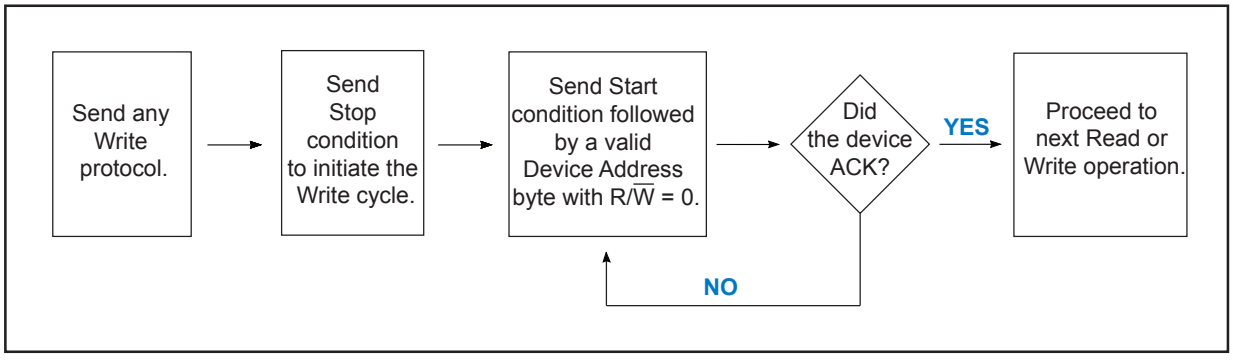
1. The A7 bit falls outside of the addressable 1K range and is therefore a don't care value on an AT24CSW01x.
2. # indicates the Hardware Address value which is managed by the ordering code of the device (see Table 6-2).

7.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed, so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/$\overline{W}$ bit set at logic '0'. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included below in Figure 7-3 to better illustrate this technique.

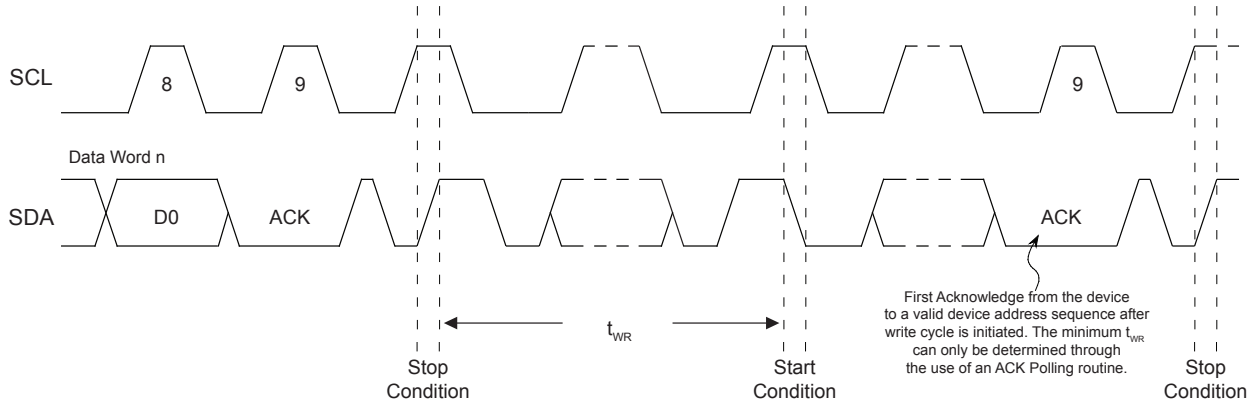
Figure 7-3. Acknowledge Polling Flowchart



7.4 Write Cycle Timing

The length of the self-timed write cycle (t_{WR}) is defined as the amount of time from the Stop condition that begins the internal write cycle to the Start condition of the first device address byte sent to the AT24CSW01X/AT24CSW02X that it subsequently responds to with an ACK. Figure 7-4 has been included to show this measurement. During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.

Figure 7-4. Write Cycle Timing



8. Write Protection

8.1 Hardware Write Protection

The AT24CSW01X/AT24CSW02X utilizes a hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is at V_{CC} (or a valid V_{IH}). No write protection will be set if the WP pin is at GND or left floating.

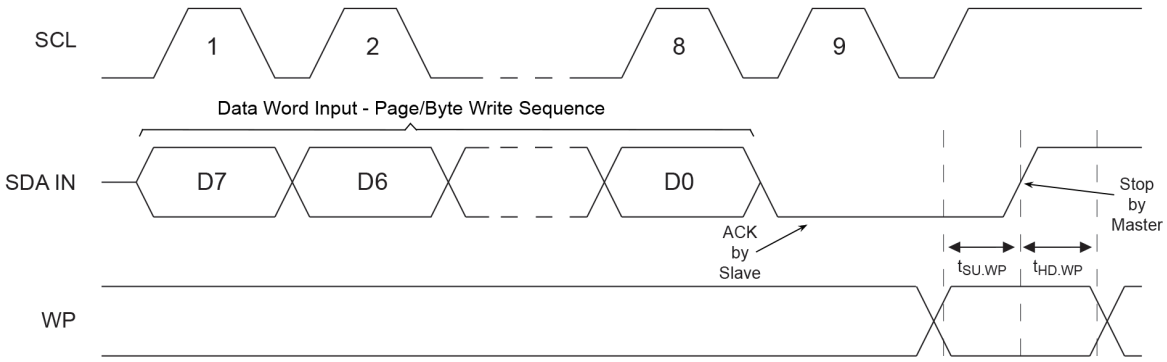
Table 8-1. AT24CSW01X/AT24CSW02X Write-Protect Behavior

WP Pin Voltage	Part of the Array Protected
V_{CC}	Full Array
GND	None – Write Protection Not Enabled

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation prior to the start of an internally self-timed write cycle. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle. The WP pin state must be valid with respect to the associated setup ($t_{SU.WP}$) and hold ($t_{HD.WP}$) timing as shown in Figure 8-1 below. The WP setup time is the amount of time that the WP state must be stable before the Stop condition is issued. The WP hold time is the amount of time after the Stop condition that the WP pin must remain stable.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the device address, word address and data bytes. However, no write cycle will occur when the Stop condition is issued. The device will immediately be ready to accept a new read or write command.

Figure 8-1. Write-Protect Setup and Hold Timing



8.2 Software Write Protection of the EEPROM Array

The AT24CSW01X/AT24CSW02X utilizes a software scheme that allows a portion or the entire EEPROM to be inhibited from being written to by modifying the contents of the Write Protection register (WPR). If desired, the WPR can be set so that it may no longer be modified, thereby making the current protection scheme permanent.

The status of the WPR can be determined by following a random read operation. Changing the state of the WPR is accomplished with a byte write operation with the requirements outlined in this section.

Accessing the WPR requires the use of 1011b (Bh) as the device type identifier in the device address byte (see Device Address Byte Requirements for Accessing the Write Protection Register). Following the device type identifier are the hardware address bits (A2, A1, A0) for which the values are determined by the ordering code of the device (see Table 6-2). Finally, bit 0 is the Read/Write Select bit where '1' is used for reading and '0' is used for writing.

Table 8-2. Device Address Byte Requirements for Accessing the Write Protection Register

Memory Region	Device Type Identifier				Hardware Client Address Bits			R/$\overline{W}$ Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write Protection Register	1	0	1	1	A2	A1	A0	R/$\overline{W}$

When accessing the Write Protection register, it is required that the A7 and A6 bits of the word address be set to '11b' respectively. The remaining bits of the word address byte are 'don't care' bits as shown in Word Address Byte Requirements for Accessing the Write Protection Register.

Table 8-3. Word Address Byte Requirements for Accessing the Write Protection Register

	A 7	A6	A5	A4	A3	A2	A1	A0
Write Protection Register	1	1	X	X	X	X	X	X

Following the word address byte are the contents of the 8-bit Write Protection register. The register format is shown in Write Protection Register Format, and the WPR bit functions are included in Write Protection Register Bit Function.

Table 8-4. Write Protection Register Format

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read WPR	0	0	0	0	WPRE	WPB1	WPB0	WPRL
Write WPR	0	1	0: No Lock	0				
			1: Set Lock					

Table 8-5. Write Protection Register Bit Function

Bit	Name		Type	Description	
3	**WPRE**	Write Protection Register Enable bit	R/W	0	No software write protection is enabled (*Factory Default*).
				1	Write protection is set by the state of the WPB[1:0] bits.
2-1	**WPB[1:0]**	Write-Protect Block bits	R/W	00	Upper ¼ of EEPROM is write protected (*Factory Default*).
				01	Upper ½ of EEPROM is write protected.
				10	Upper ¾ of EEPROM is write protected.
				11	Entire EEPROM is write protected.
0	**WPRL**	Write-Protect Lock Bit	R/OTP	0	WPR can be written to; requires D5 = 0 during write (*Factory Default*).
				1	WPR will become permanently locked (requires D5 = 1) during write.

- **Write Protection Register Enable bit (WPRE), Bit 3**
  This bit is used to enable or disable the device software write protection feature. A logic '0' in this position will disable software write protection, and a logic '1' will enable this function.
- **Write-Protect Block bits (WPB[1:0]), Bits 2:1**
  These bits allow four levels of protection of the memory array provided that the WPRE bit is a logic '1'. If the WPRE bit is a logic '0', the state of the WPB[1:0] bits have no impact to device protection. The protected address ranges are found in Table 8-6.

- **Write-Protect Lock Bit (WPRL), Bit 0**
  This bit is used to permanently lock the current state of the WPR. A logic '0' indicates that the WPR can be modified, whereas a logic '1' indicates the WPR has been locked and can no longer be modified. To safeguard against accidental locking of the WPR, the D5 bit must match the WPRL bit (D0 bit) sent to the device. If these bits do not match, the write cycle is aborted and the WPR contents are not modified.

8.2.1 Protected Address Ranges Set by WPB1 and WPB0

The EEPROM array in the AT24CSW01X/AT24CSW02X will be protected from writing in accordance with the WPB1 and WPB0 bit values as long as the WPRE bit is set to logic '1'. If the WPRE bit is set to logic '0', no portion of the EEPROM array will be protected. The combination of these three bits creates five possible levels of protection for the device. The protected address ranges of the memory are shown in Table 8-6.

Table 8-6. Word Address Byte Requirements for Accessing the Write Protection Register

Protection Level	WPRE	WPB1	WPB2	Protected Address Range		Unprotected Address Range	
				1-Kbit	2-Kbit	1-Kbit	2-Kbit
None	0	X	X	None	None	00h–7Fh	00h-FFh
Upper ¼	1	0	0	60h–7Fh	C0h–FFh	00h–5Fh	00h–BFh
Upper ½	1	0	1	40h–7Fh	80h–FFh	00h–3Fh	00h–7Fh
Upper ¾	1	1	0	20h–7Fh	40h–FFh	00h–1Fh	00h–3Fh
Full Array	1	1	1	00h-7Fh	00h-FFh	None	None

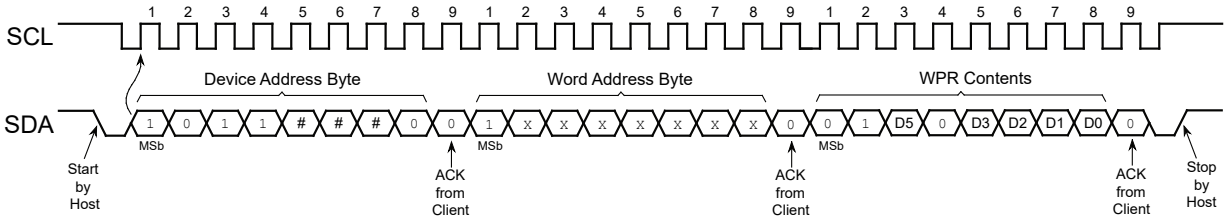
8.3 Writing to the Write Protection Register

When writing the WPR, data bit 7 through 4 are used to ensure that a write operation was intentional. For all write operations to the WPR, bit 6 must be a logic '1' as seen in Table 8-4.

Additionally, data bit 5 must be set in accordance with the D0 bit value (WPRL) as noted below. If the WPR is to remain unlocked, then the upper nibble sent during the write operation would be 4h and D0 must be a logic '0', whereas if the WPR is to be permanently locked, the upper nibble would need to be 6h and D0 must be a logic '1'. A mismatch of D5 and the WPRL bit will cause the write cycle to abort.

Sending more than one byte to the AT24CSW01X/AT24CSW02X when trying to write to the WPR will cause the write cycle to abort and the contents of the WPR will not be changed. Additionally, if the WPR is already locked (WPRL = 1), the write cycle will not execute and the device will be ready for a new operation.

Figure 8-2. Write Protection Register Write Operation



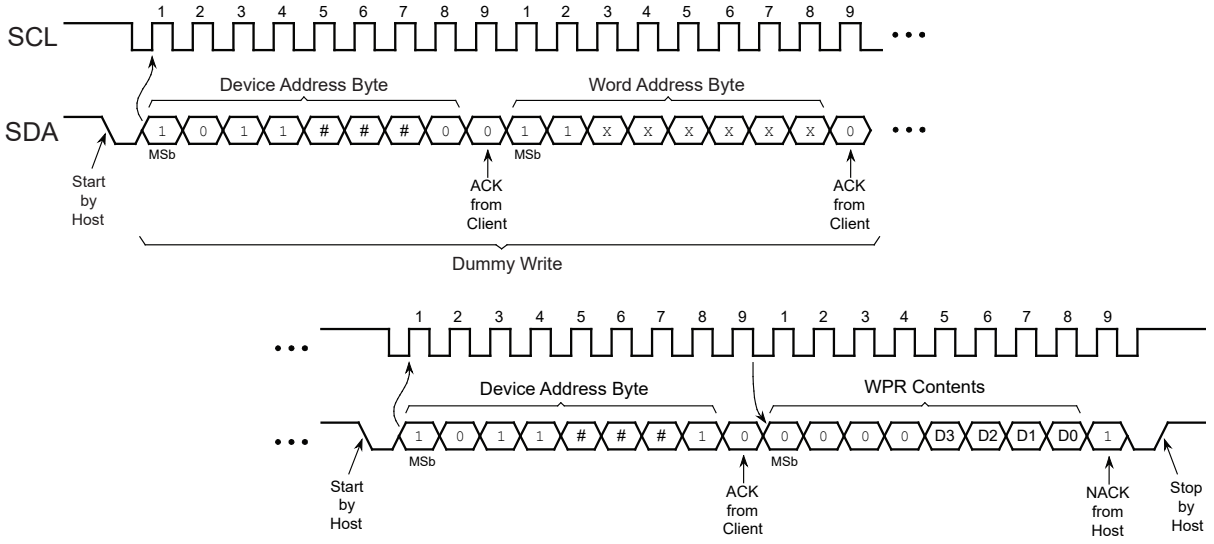
Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

8.4 Reading the Write Protection Register

To read the contents of the WPR, a random read operation must be sent to the device (see Random Read) so that the reserved word address bits A7 and A6 can properly be set. It is not possible to read the contents of the WPR with a current address read.

When reading the WPR contents, data bit 7 through 4 will always read as a logic '0' as seen in Table 8-4.

Figure 8-3. Read Write Protection Register



Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

9. Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are multiple read operations supported by the device:

- Current Address Read
- Random Address Read
- Sequential Read

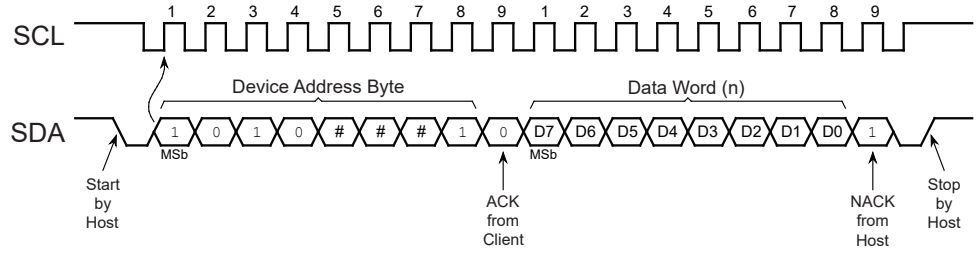
Note:
The AT24CSW01x/AT24CSW02x contains a single Address Pointer register, which is shared by both the EEPROM and the Security register. As such, when changing from one region to the other, the first read operation in the new region should begin with a dummy write sequence (i.e. a random read operation with the new region's device address and word address bytes) in order to ensure the Address Pointer is set to a known value. See Read Operations in the Security Register for additional requirements on read operations in the Security register.

9.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address roll-over during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 9-1. Current Address Read

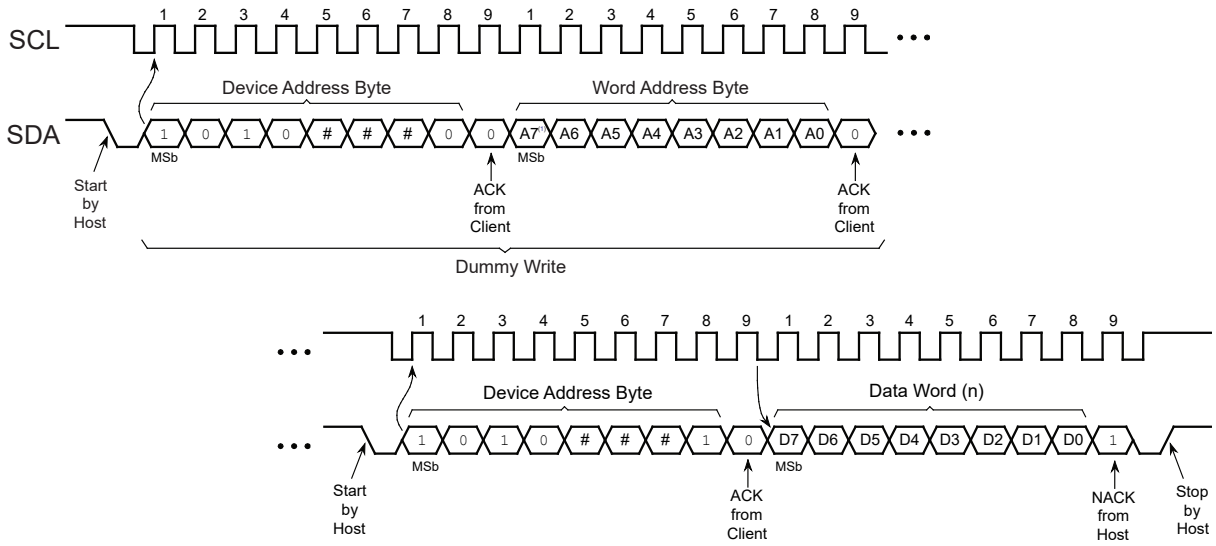


Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

9.2 Random Read

A random read begins in the same way as a byte write operation does to load in a new data word address. This is known as a "dummy write" sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus host must generate another Start condition. The bus host now initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 9-2. Random Read



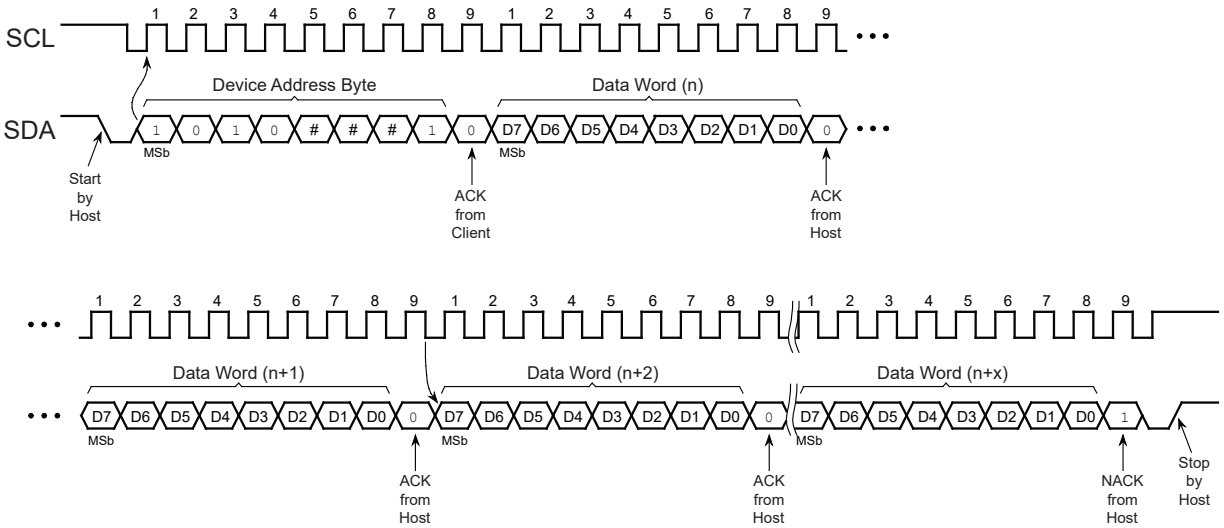
Notes:

1. The A7 bit falls outside of the addressable 1K range and is therefore a “don’t care” value on an AT24CSW01x.
2. # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

9.3 Sequential Read

Sequential reads are initiated by either a current address read or a random read. After the bus host receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will roll-over and the sequential read will continue from the beginning of the memory array. All types of read operations will be terminated if the bus host does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the host may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 9-3. Sequential Read



Note:

1. # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

10. Security Register

The AT24CSW01X/AT24CSW02X includes a 32-byte Security register. The Security register is segmented into a 16-byte read-only section and a 16-byte user-programmable section organized as 4 pages of 8 bytes each. The user-programmable portion supports both byte write and page write operations. The read-only section contains a pre-programmed ensured unique 128-bit serial number. The user-programmable portion may be permanently locked at any time with the Lock command.

Table 10-1. Security Register Organization

Security Register Byte Number									
0	1	...	14	15	16	17	...	30	31
Factory Programmed (Read-only) 0-15: Device Serial Number					User Programmable (Lockable)				

10.1 Custom Programming Option

Microchip supports the preprogramming and subsequent locking of customer specific data in the user-programmable portion of the Security register. Contact the local Microchip Sales representative for more details on this custom solution.

10.2 Read Operations in the Security Register

Random read and sequential read operations are supported by the Security register provided the device address uses a device type identifier of `1011b` (Bh), and the A7 and A6 bits of the word address are set to `10b`. Current address reads in the Security register are not supported due to the fact that the required A7 and A6 address bits in the word address byte do not get sent to the device.

The first 16 bytes of the Security register are by definition read-only and contain a preprogrammed ensured unique 128-bit serial number. The remaining 16 bytes of the Security register are user-programmable and can be locked from any future programming operations (see Lock Command).

10.2.1 Address Pointer Behavior

The AT24CSW01X/AT24CSW02X contains a single Address Pointer that is shared between the EEPROM and the Security register. As such, any read operation to the Security register should begin with a dummy write sequence (i.e. random read) to ensure the Address Pointer is set to a known value. If the preceding operation was to the Security register, the Address Pointer will retain the last access location incremented by one.

10.2.2 Serial Number Read

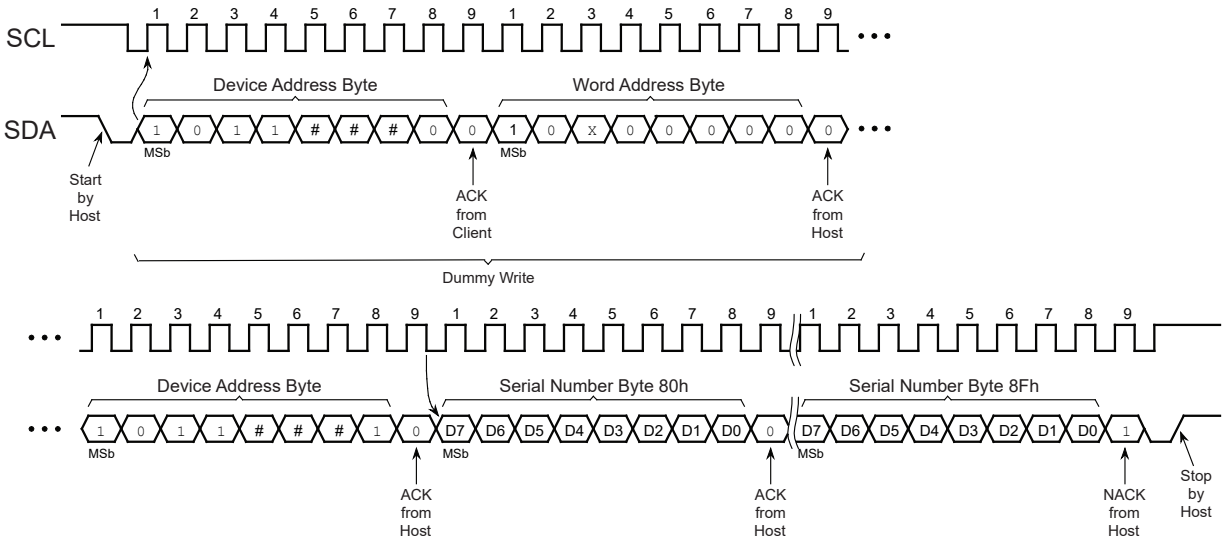
Reading the 128-bit serial number is similar to the sequential read sequence, but requires use of the device address seen in a dummy write and a specific word address. The word address must begin with a `10b` sequence regardless of the intended address. If a word address other than `10b` is used, the device will not output valid data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

Note: The entire 128-bit value must be read from the starting address of the serial number block to ensure a unique number. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

When the end of the Security register is reached (32 bytes of data), the data word address will roll over to the beginning of Security register starting with the most significant byte of the 128-bit serial number. The serial number read operation or any read of the Security register is terminated when the host does not respond with an ACK and instead issues a Stop condition.

Figure 10-1. Serial Number Read



Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

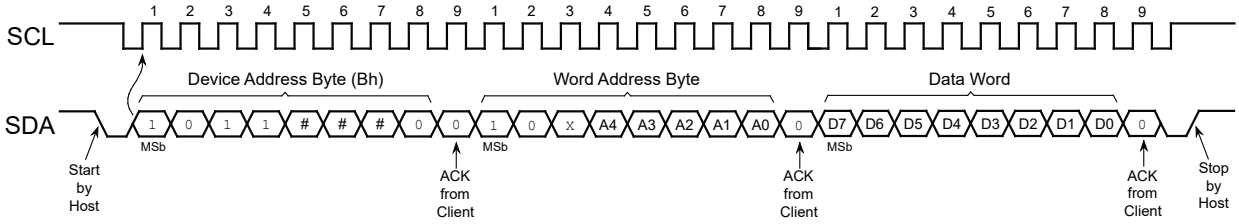
10.3 Write Operations in the Security Register

The Security register supports byte writes, page writes, and partial page writes in the upper 16 bytes of the region. Page writes and partial page writes in the Security register have the same page boundary restrictions and behavior as they do in the EEPROM region (see Write Operations).

Writing in the Security register requires beginning the device address byte with `1011b`(Bh), matching the hardware address bits (A2, A1, A0) to the corresponding value determined by the ordering code (see Table 6-2), and sending a logic '`0`' in the Read/Write Select bit. The device will ACK this sequence.

Following the device address byte, bits A7 and A6 of the word address byte must be set to `10b` regardless of the intended address being written. Refer to Table 6-3 for detailed requirements on these bits. Figure 10-2 is an example of a byte write operation in the Security register.

Figure 10-2. Byte Write in the Security Register



Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

The user-programmable portion of the Security register can be permanently inhibited from future writing with the Lock command. The status of the Lock state can be determined by sending a subset of the Lock command.

10.3.1 Lock Command

The Lock command is an irreversible sequence that will permanently prevent all future writing to the Security register. Once the Lock command has been executed, the Security register becomes read-only.

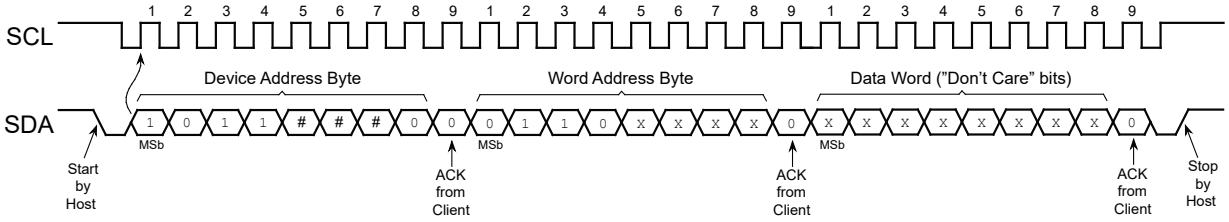
Note: Once the Security register has been locked, it cannot be unlocked.

The Lock command protocol emulates a byte write operation to the Security register. However, the A7 through A4 bits of the word address must be set to `0110b` (6h). The remaining bits of the word address and the data word are "don't care" bits. Even though these bits are "don't cares", they still must be transmitted to the part. An ACK response to the

word address and data word byte indicates the Security register is not currently locked. A NACK response indicates the AT24CSW01x/AT24CS02x is already locked. Please refer to Determining the Lock State of the Security Register for details about determining the Lock status of the AT24CSW01x/AT24CS02x.

The sequence completes with a Stop condition being sent to the device, which initiates a self-timed internal write cycle. The Lock operation will conclude upon completion of that write cycle, subsequently making the Security register permanently read-only. Read operations are always allowed to the device.

Figure 10-3. Lock Command

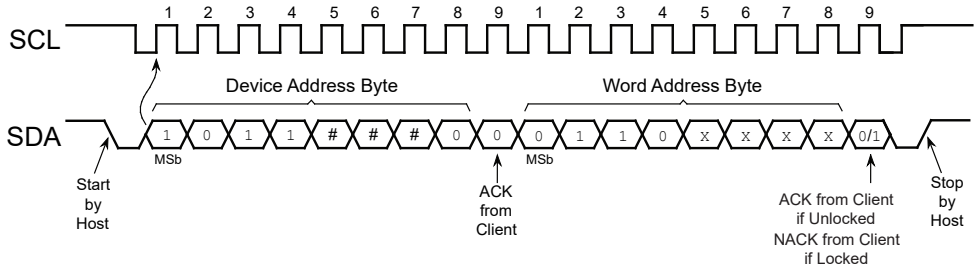


Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

10.3.2 Determining the Lock State of the Security Register

The Lock state of the device can be determined by sending a subset of the Lock command to the device. Only the device address byte and word address byte need to be transmitted to the device to determine the Lock state. An ACK response to the word address byte indicates the Lock has not been set while a NACK response indicates the Lock has been set. If the Lock has already been set, it cannot be undone. The abbreviated Lock sequence is completed by the host sending a Stop condition to the device.

Figure 10-4. Determining the Security Register Lock State



Note: # indicates the hardware address value which is managed by the ordering code of the device (see Table 6-2).

11. Device Default Condition from Microchip

The AT24CSW01X/AT24CSW02X is delivered with the EEPROM array set to logic '1', resulting in FFh data in all locations.

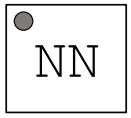
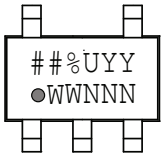
The Security register contains a preprogrammed 128-bit serial number in the lower 16 bytes. The upper 16 bytes of this register is set to logic '1' resulting in FFh data.

The device is delivered with the Security register Lock function not enabled (see Lock Command), and the Write Protection register set to 00h (no software protection).

12. Packaging Information

12.1 Package Marking Information

AT24CSW01x and AT24CSW02x: Package Marking Information

4-ball WLCSP	5-lead SOT23
	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

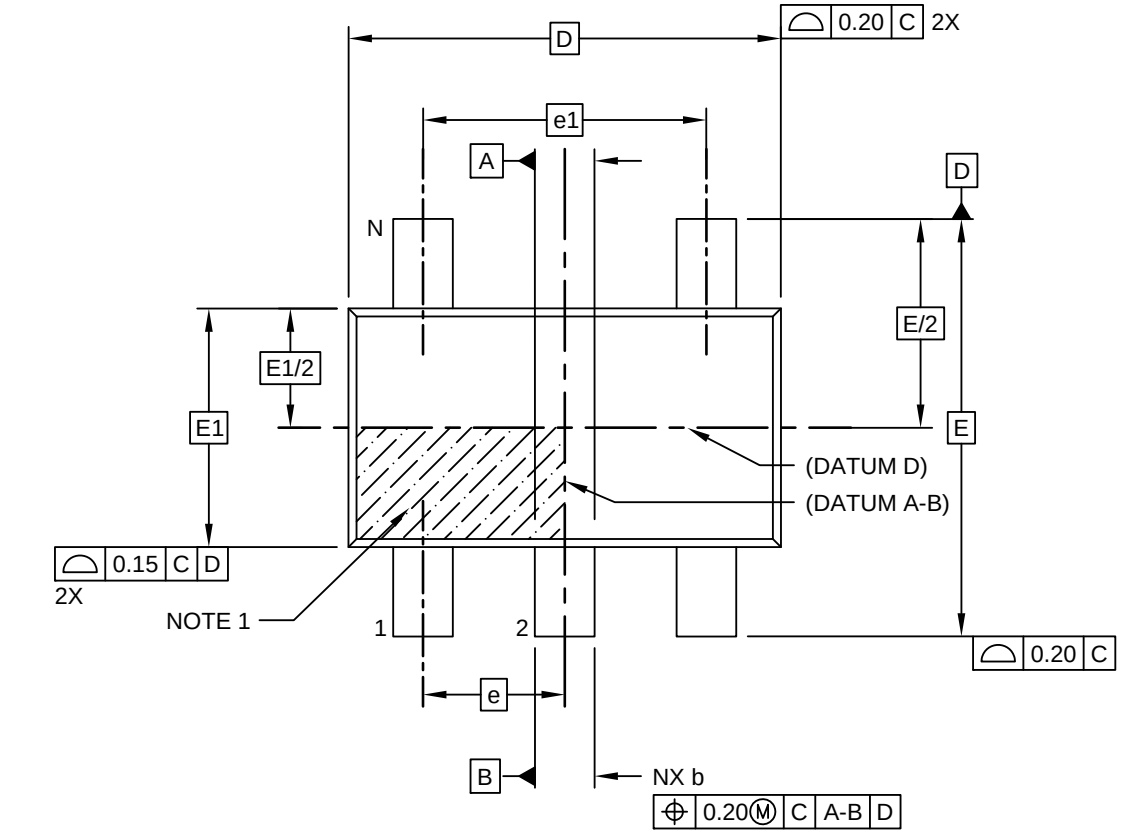
Catalog Number Truncation					
AT24CSW01X				Truncation Code W1: Not used for WLCSP	
AT24CSW02X				Truncation Code W2: Not used for WLCSP	
Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	M: 1.7V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	

Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	H or U: Industrial Grade	AT: Atmel ATM: Atmel ATML: Atmel

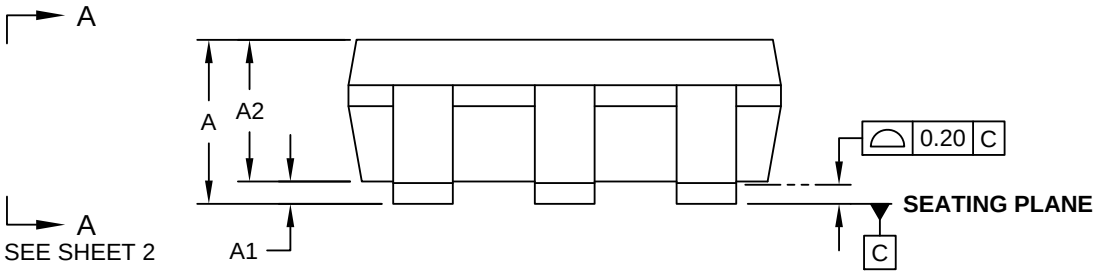
Trace Code
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

5-Lead Plastic Thin Small Outline Transistor (NMB) [TSOT]
Atmel Legacy Global Package Code TSZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

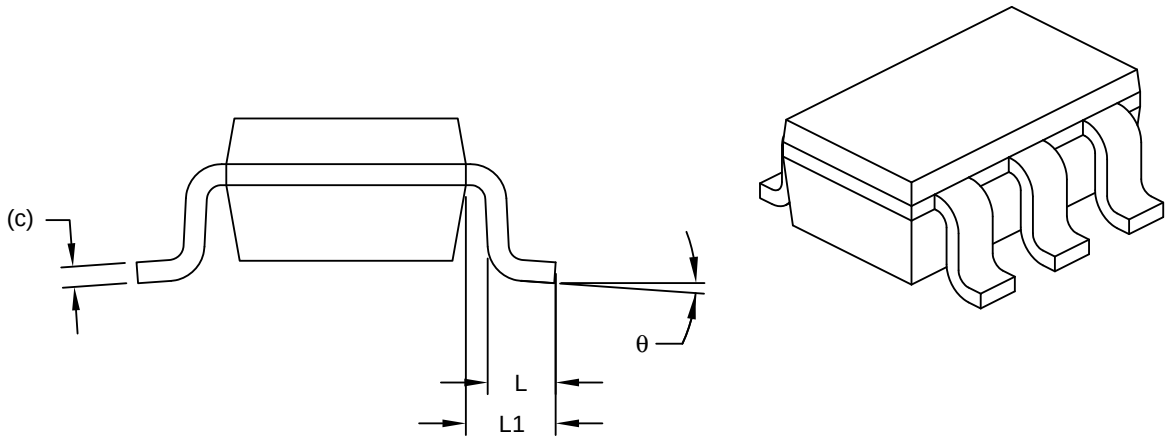


SIDE VIEW

Microchip Technology Drawing C04-21344 Rev B Sheet 1 of 2

5-Lead Plastic Thin Small Outline Transistor (NMB) [TSOT]
Atmel Legacy Global Package Code TSZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.70	0.90	1.00
Standoff	A1	-	-	0.10
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	8°
Lead Thickness	c	0.08	-	0.20
Lead Width	b	0.30	-	0.50

Notes:

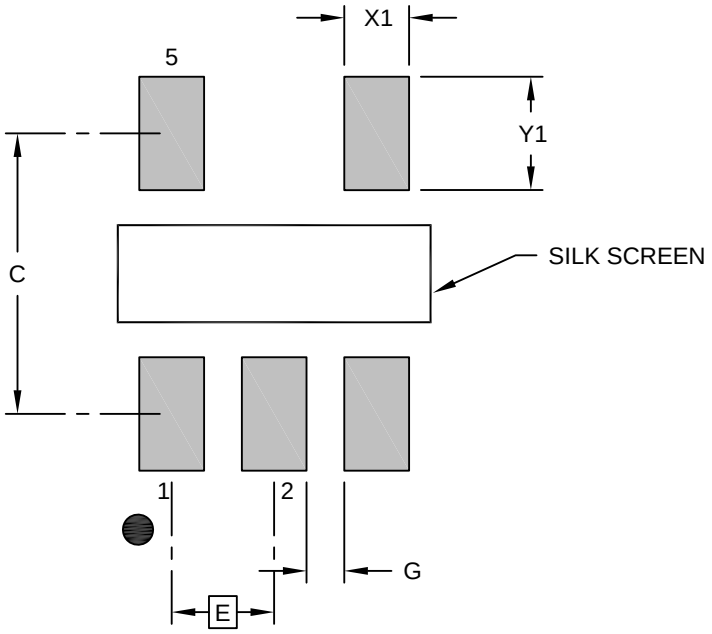
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21344 Rev B Sheet 2 of 2

5-Lead Plastic Thin Small Outline Transistor (NMB) [TSOT]
Atmel Legacy Global Package Code TSZ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



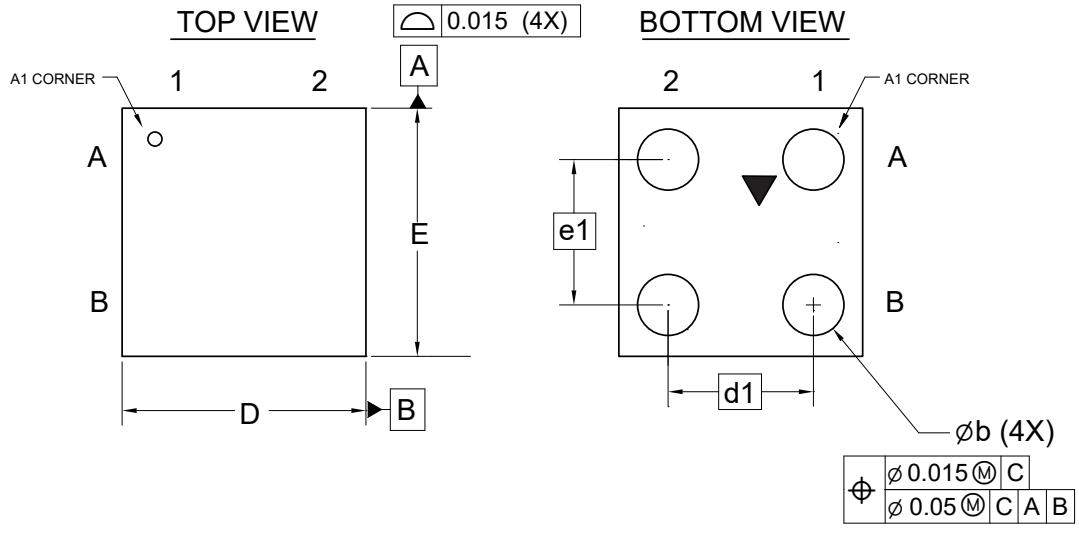
RECOMMENDED LAND PATTERN

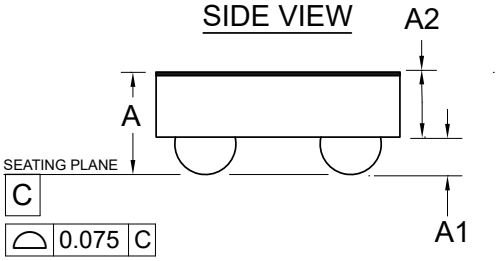
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.60	
Contact Pad Width (X5)	X1			0.60
Contact Pad Length (X5)	Y1			1.05
Contact Pad to Center Pad (X2)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23344 Rev B





PIN ASSIGNMENT MATRIX

	1	2
A	V_{CC}	GND
B	SCL	SDA

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.260	0.295	0.330	
A1	—	0.070	—	
A2	—	0.225	—	3
D	Contact Microchip for Details			
d1	0.400 BSC			
E	Contact Microchip for Details			
e1	0.400 BSC			
b	—	0.162	—	

Note: 1. Dimensions are NOT to scale.
2. Solder ball composition is 95.5Sn-4.0Ag-0.5Cu.
3. Product offered with Back Side Coating (BSC)

10/1/15

	TITLE	GPC	DRAWING NO.	REV.
	4U-13, 4-ball 2x2 Array, 0.40mm Pitch Wafer Level Chip Scale Package (WLCSP) with BSC	GUJ	4U-13	A

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

13. Revision History

Revision B (August 2021)
Replaced terminology "Master" and "Slave" with "Host" and "Client" respectively. Added SOT23 package option and WP pin details.

Revision A (August 2020)
Updated to the Microchip template. Microchip DS20006396 replaces Atmel document 8982. Updated Part Marking Information. Updated the "Software Reset" section. Added ESD rating. Updated formatting to current template.

Atmel Document 8982 Revision B (January 2017)
Updated from Preliminary to Complete status. Updated Power On Requirements and Reset Behavior section

Atmel Document 8982 Revision A (July 2015)
Initial release of this document, Preliminary status.

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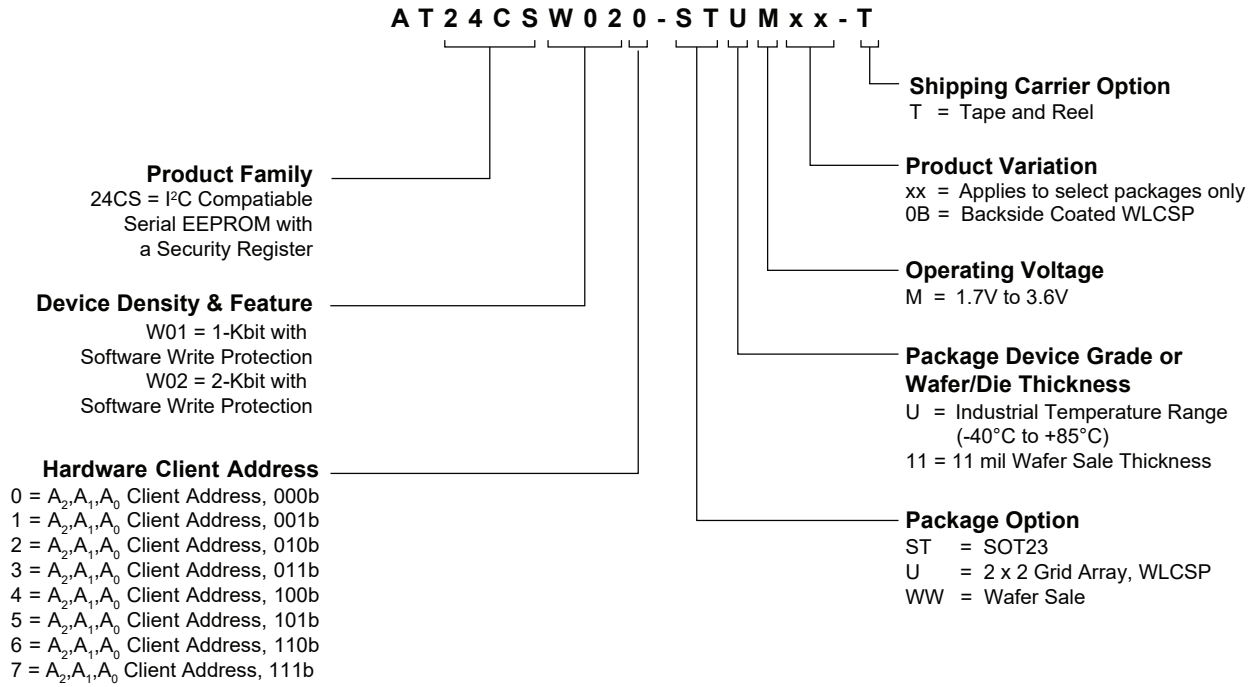

Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT24CSW010-STUM-T	SOT23	4U-13	ST	Tape and Reel	Industrial Temperature (-40°C to 85°C)
AT24CSW020-STUM-T	SOT23	4U-13	ST	Tape and Reel	
AT24CSW010-UUM0B-T	WLCSP	4U-13	U	Tape and Reel	
AT24CSW020-UUM0B-T	WLCSP	4U-13	U	Tape and Reel	

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- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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