

# Four Channel, High Speed $\pm 70V$ 2.0A Ultrasound RTZ Pulser

## Features

- ▶ HVCMOS technology for high performance
- ▶ High density integrated ultrasound transmitter
- ▶ 0 to  $\pm 70V$  output voltage
- ▶  $\pm 2.0A$  source and sink minimum pulse current
- ▶ Up to 20MHz operation frequency
- ▶  $\pm 2.5ns$  matched delay times
- ▶ 2.5 to 5.0V CMOS logic interface
- ▶ Built-in output drain diode and bleed resistors
- ▶ CW/RTZ Doppler quick switching
- ▶ Two damping mode options

## Applications

- ▶ Portable medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ NDT ultrasound transmission
- ▶ Pulse waveform generator

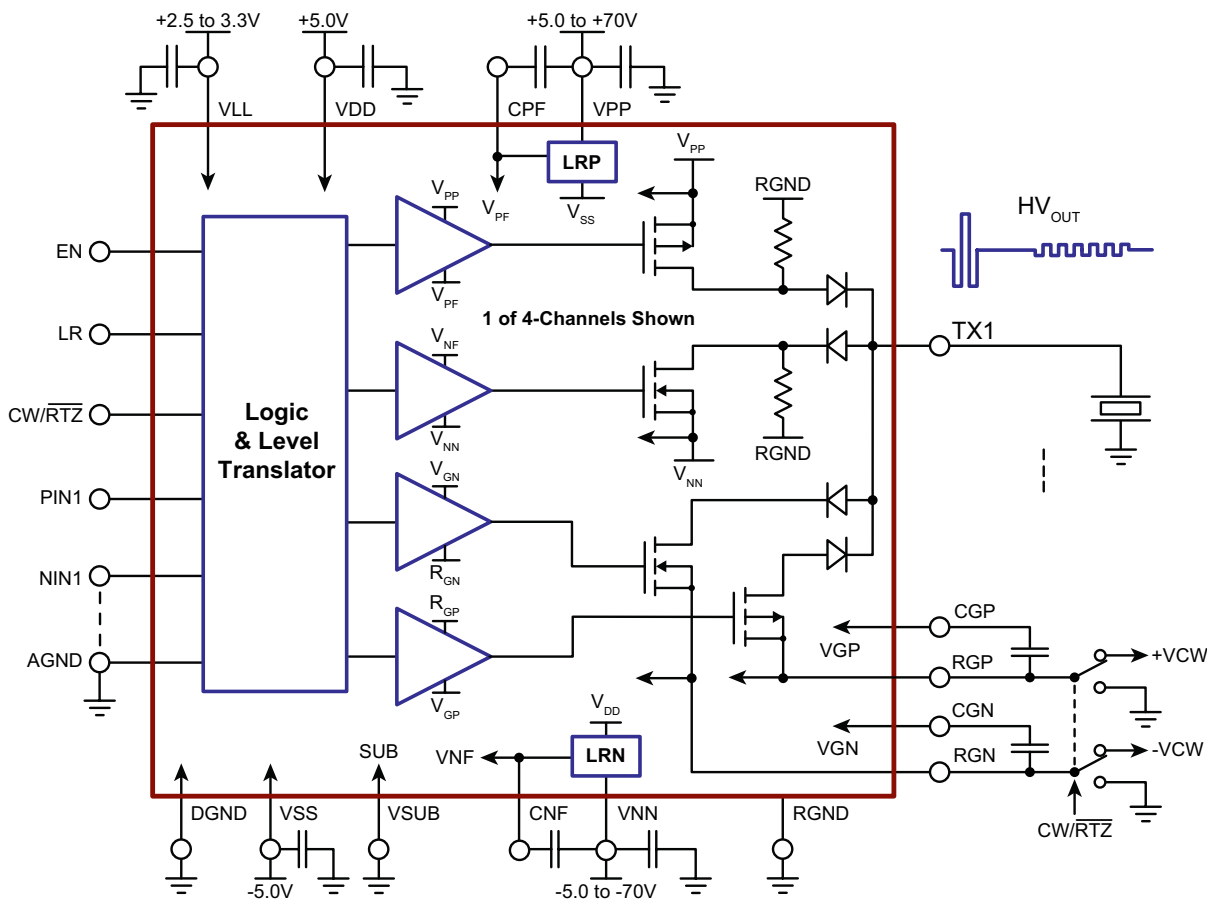
## General Description

The Supertex HV7331 is a four-channel, monolithic, high voltage, high speed pulse generator with built in fast return to zero damping FETs. This high voltage and high-speed integrated circuit is designed for portable medical ultrasound imaging devices, and can also be used for NDT applications.

The HV7331 consists of a controller logic interface circuit, level translators, MOSFET gate drives, and high current power P-channel and N-channel MOSFETs as the output stage for each channel.

The peak output currents of each channel are guaranteed to be over 2.0A with up to a  $\pm 70V$  pulse swing. The integrated regulators for the gate drivers not only saves two floating voltage supplies, but also makes the PCB layout easier. The split common source for the P or N damping MOSFETs provide pulse or CW Doppler mode quick switch-over for cost and power savings.

## Typical Application Circuit



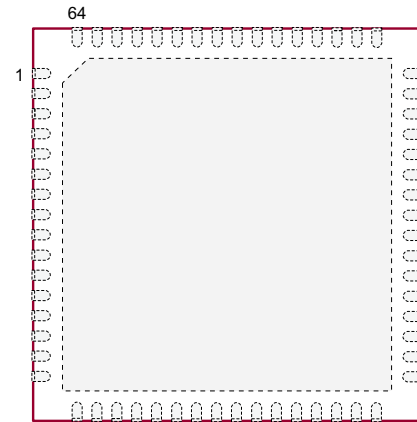
## Ordering Information / Availability

Part Number	Package Option	Packing
HV7331K6-G	64-Lead QFN (9.0x9.0)	260/tray

-G indicates package is RoHS compliant ("Green")

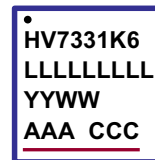


## Pin Configuration



**64-Lead QFN**  
(top view)

## Package Marking



L = Lot Number  
 YY = Year Sealed  
 WW = Week Sealed  
 A = Assembler ID  
 C = Country of Origin  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

**64-Lead QFN**

## Typical Thermal Resistance

Package	$\theta_{ja}$
64-Lead QFN	21°C/W

## Absolute Maximum Ratings

Parameter	Value
AGND, DGND and $V_{SUB}$	0V
$V_{LL}$ , Positive logic supply	-0.5 to +5.5V
$V_{DD}$ , Positive logic and level translator supply	-0.5 to +5.5V
$V_{SS}$ , Negative level translator supply	+0.5 to -5.5V
$(V_{PP} - V_{NN})$ Differential high voltage supply	+160V
$V_{PP}$ , High voltage positive supply	-0.5 to +80V
$V_{NN}$ , High voltage negative supply	+0.5 to -80V
All logic input $PIN_x$ , $NIN_x$ , EN and CW voltages	-0.5 to +5.5V
$(V_{PP} - TX_n)$ $V_{PP}$ to $TX_n$ voltage difference	+160V
$(TX_n - V_{NN})$ $TX_n$ to $V_{NN}$ voltage difference	+160V
(RGP - GND) RGP to GND voltage difference	-0.5 to +5.5V
(RGN - GND) RGN to GND voltage difference	+0.5 to -5.5V
Storage temperature	-65 to 150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Power-Up Sequence

Step	Description
1	$V_{LL}$ with logic signal low
2	$V_{DD}$ , $V_{SS}$
3	$V_{PP}$ , $V_{NN}$
4	Logic control signals active

**Note:**

Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering up/down sequence is only recommended in order to minimize possible inrush current.

## Power-Down Sequence

Step	Description
1	All logic signals go to low
2	$V_{PP}$ , $V_{NN}$
3	$V_{DD}$ , $V_{SS}$
4	$V_{LL}$

## Operating Supply Voltages and Current (Four Active Channels)

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $V_{PP} = +70V$ ,  $V_{NN} = -70V$ ,  $V_{SUB} = 0V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{LL}$	Logic voltage reference	2.25	3.3	5.25	V	---
$V_{DD}$	Positive voltage supply	4.85	5.0	5.15	V	---
$V_{SS}$	Negative voltage supply	-5.15	-5.0	-4.85	V	---
$V_{RGP}$	Positive voltage supply	1.0	-	5.5	V	When $CW/\overline{RTZ} = 0$ (in B-Mode) must be $0 \leq V_{RGP} \leq +0.5V$ and $0 \geq V_{RGN} \geq -0.5V$
$V_{RGN}$	Negative voltage supply	-5.5	-	-1.0	V	
$V_{PP}$	Positive HV supply	VDD	-	+70	V	---
$V_{NN}$	Negative HV supply	-70	-	VSS	V	---
$I_{LL}$	$V_{LL}$ , Current EN = 0	-	1.0	3.0	$\mu A$	---
$I_{DDQ}$	$V_{DD}$ , Current EN = 0	-	100	180	$\mu A$	---
$I_{DDEN}$	$V_{DD}$ , Current EN = 1	-	2.5	6.0	mA	f = 0MHz, $CW/\overline{RTZ} = \text{Low}$ RGN = RGP = 0V
$I_{SSQ}$	$V_{SS}$ , Current EN = 0	-	10	20	$\mu A$	
$I_{SSEN}$	$V_{SS}$ , Current EN = 1	-	2.0	6.0	mA	f = 5.0MHz, $CW/\overline{RTZ} = \text{High}$ RGN/RGP = $\pm 5.0V$ , No Load
$I_{DDCW}$	$V_{DD}$ , Current EN = CW = 1	-	45	55	mA	
$I_{SSCW}$	$V_{SS}$ , Current EN = CW = 1	-	45	55	mA	
$I_{RGPCW}$	RGP Current EN = CW = 1	-	60	75	mA	
$I_{RGNCW}$	RGP Current EN = CW = 1	-	35	75	mA	---
$I_{PPQ}$	$V_{PP}$ , Current EN = 0	-	32	50	$\mu A$	
$I_{NNQ}$	$V_{NN}$ , Current EN = 0	-	32	50	$\mu A$	f = 5.0MHz, continuous, no loads
$I_{PPEN}$	$V_{PP}$ , Current EN = 1	-	290	-	mA	
$I_{NNEN}$	$V_{NN}$ , Current EN = 1	-	290	-	mA	f = 0MHz
$I_{PPEN}$	$V_{PP}$ , Current EN = 1, LR = 1	-	0.25	0.5	mA	
$I_{NNEN}$	$V_{SS}$ , Current EN = 1, LR = 1	-	0.25	0.5	mA	
$I_{PPEN}$	$V_{PP}$ , Current EN = 1, LR = 0	-	32	50	$\mu A$	
$I_{NNEN}$	$V_{NN}$ , Current EN = 1, LR = 0	-	32	50	$\mu A$	

## Logic Inputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{IH}$	Input logic high voltage	$(V_{LL} - 0.4)$	-	$V_{LL}$	V	---
$V_{IL}$	Input logic low voltage	0	-	0.4	V	---
$I_{IH}$	Input logic high current	-	-	1.0	$\mu A$	---
$I_{IL}$	Input logic low current	-1.0	-	-	$\mu A$	---
$C_{IN}$	Input logic capacitance	-	-	5.0	pF	---

**Electrical Characteristics**

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +70V$ ,  $V_{NN} = -70V$ ,  $V_{SUB} = 0V$ ,  $T_A = 25^\circ C$ )

**Pulser P-Channel MOSFET**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	2.0	3.3	-	A	---
$R_{ON}$	Channel resistance	-	4.0	5.5	$\Omega$	$I_{SD} = 100mA$
$C_{OSS}$	Output capacitance	-	50	-	pF	$V_{DS} = 25V$ , $f = 1.0MHz$

**Pulser N-Channel MOSFET**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	2.0	3.3	-	A	---
$R_{ON}$	Channel resistance	-	2.3	3.0	$\Omega$	$I_{SD} = 100mA$
$C_{OSS}$	Output capacitance	-	50	-	pF	$V_{DS} = 25V$ , $f = 1.0MHz$

**MOSFET Drain Bleed Resistor**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{P/N1-4}$	Output bleed resistance	120	-	190	k $\Omega$	---
$P_{RO}$	Bleed resistors power limit	-	-	40	mW	---

**Damping P-Channel MOSFET**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	2.0	3.3	-	A	$V_{RGP} = V_{RGN} = 0V$
$R_{ON}$	Channel resistance	-	3.7	4.8	$\Omega$	$I_{SD} = 100mA$
$C_{OSS}$	Output capacitance	-	50	-	pF	$V_{DS} = 25V$ , $f = 1.0MHz$

**Damping N-Channel MOSFET**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	2.0	3.3	-	A	$V_{RGP} = V_{RGN} = 0V$
$R_{ON}$	Channel resistance	-	2.7	3.5	$\Omega$	$I_{SD} = 100mA$
$C_{OSS}$	Output capacitance	-	50	-	pF	$V_{DS} = 25V$ , $f = 1.0MHz$

**CW Mode P- & N-Channel MOSFET**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{ONCW-P}$	CW Mode ON-resistance	-	14	-	$\Omega$	$I_{SD} = 100mA$ , $V_{RGP} = +5.0V$ , $V_{RGN} = -5.0V$
$R_{ONCW-N}$	CW Mode ON-resistance	-	14	-	$\Omega$	
$\Delta R_{ONCW}$	P- & N-Ch $R_{ONCW}$ matching	-	$\pm 2.0$	-	$\Omega$	

**AC Electrical Characteristics**

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +70V$ ,  $V_{NN} = -70V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{r1}$	Pulser output rise time	-	15	18	ns	330pF//2.5k $\Omega$ load
$t_{f1}$	Pulser output fall time	-	15	18	ns	
$t_{r2}$	Damping output rise time	-	15	18	ns	
$t_{f2}$	Damping output fall time	-	15	18	ns	
$t_{r3}$	CWD output rise time	-	17	22	ns	330pF//2.5k $\Omega$ load, RGP/RGN = $\pm 5.0V$
$t_{f3}$	CWD output fall time	-	17	22	ns	

**AC Electrical Characteristics (cont.)**

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +70V$ ,  $V_{NN} = -70V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$f_{OUT}$	Output frequency range	-	-	20	MHz	100Ω load
HD2	Second harmonic distortion	-	-40	-	dB	
$t_{EN\_ON}$	Delay on mode change	-	200	300	μs	CPF, CNF capacitor 0.47μF per pin, 50% to 90%
$t_{EN\_OFF}$	Chip disable time	-	2.0	4.0	μs	
$t_{LR\_ON}$	Linear regulators enable time	-	200	300	μs	
$t_{LR\_OFF}$	Linear regulators disable time	-	2.0	4.0	μs	
$t_{drp1}$	Pulser delay time on P-rise	8.0	-	13	ns	CW/ $\overline{RTZ}$ = 0 $R_1 = R_2 = 1.0\Omega$ to GND
$t_{dfp1}$	Pulser delay time on P-fall	5.0	-	10	ns	
$t_{drn1}$	Pulser delay time on N-rise	8.0	-	13	ns	
$t_{dfn1}$	Pulser delay time on N-fall	5.0	-	10	ns	
$t_{drp2}$	CWD delay time on P-rise	6.0	-	12	ns	CW/ $\overline{RTZ}$ = 1 $R_1 = R_2 = 1.0\Omega$ to GND
$t_{dfp2}$	CWD delay time on P-fall	6.0	-	12	ns	
$t_{drn2}$	CWD delay time on N-rise	6.0	-	12	ns	
$t_{dfn2}$	CWD delay time on N-fall	6.0	-	12	ns	
$\Delta t_{DELAY}$	Delay time matching	-	±2.5	-	ns	P to N, channel to channel
$t_{JCW}$	Delay jitter on rise or fall	-	13	-	ps	$V_{RGP}/V_{RGN} = \pm 5.0V$ , input $t_r$ 50% to HV <sub>OUT</sub> $t_r$ or $t_f$ 50%, with 50Ω load

**Logic Control Table (each channel)**

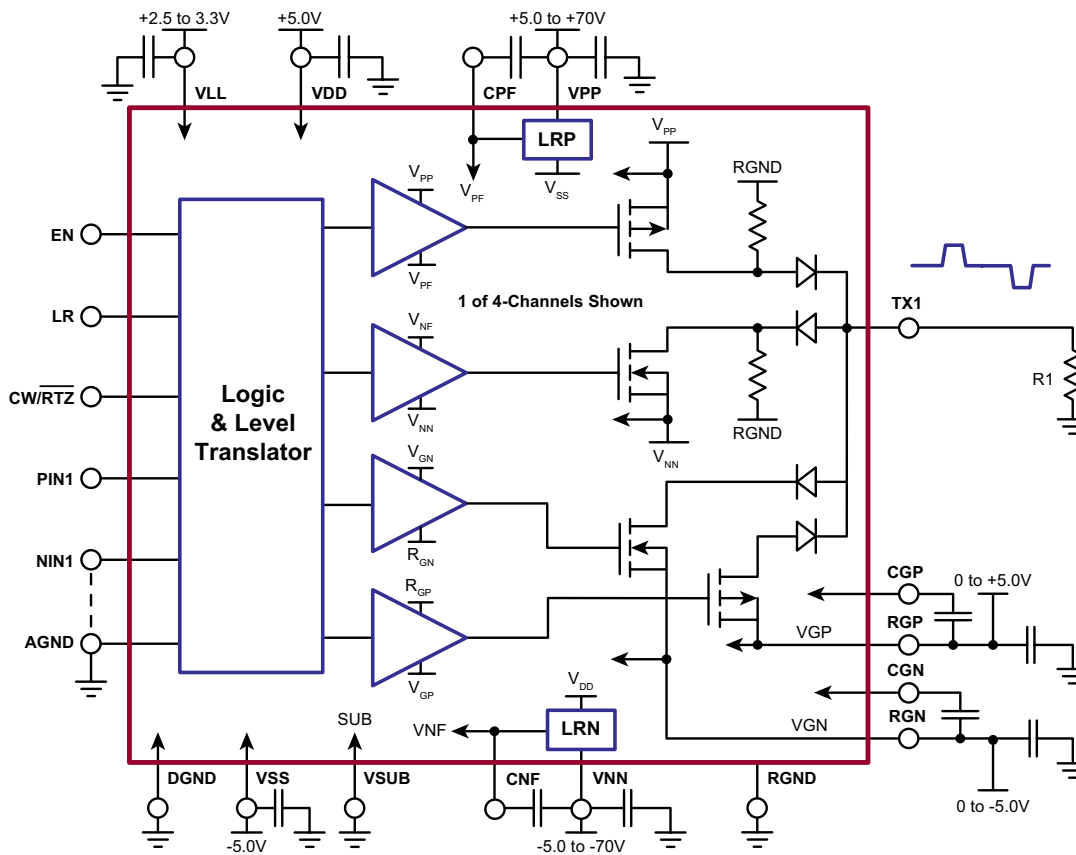
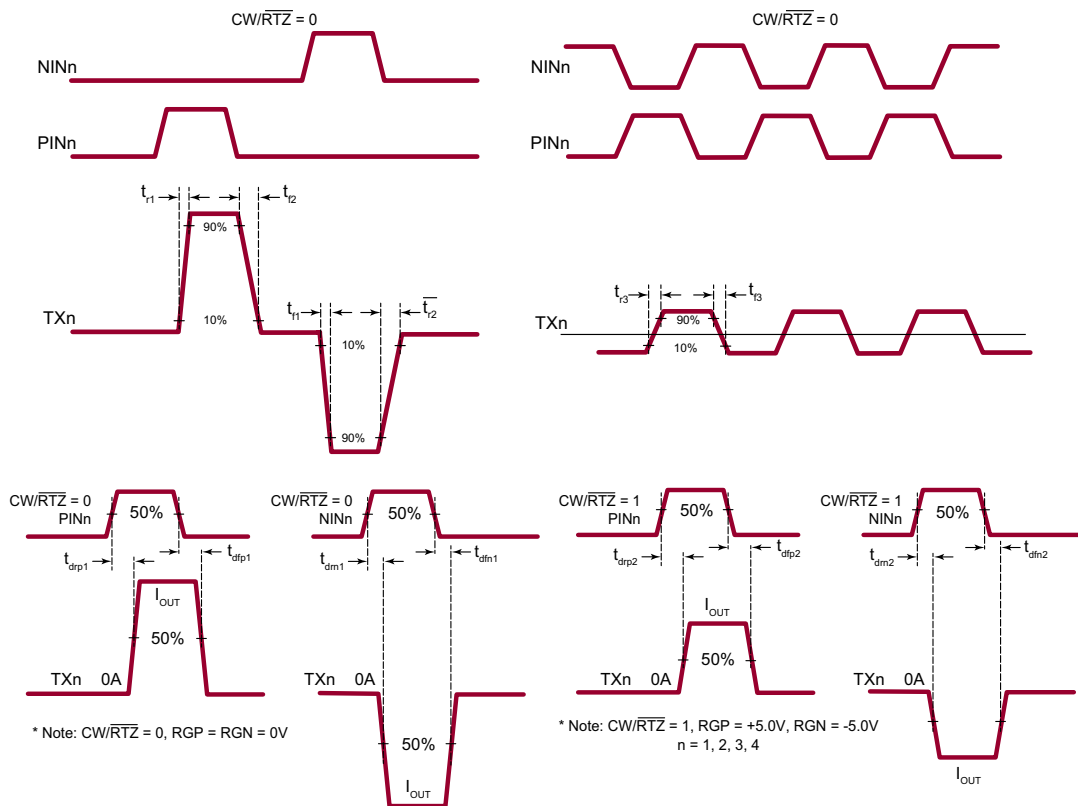
Operation Mode	Inputs				Output MOSFETs			
	EN	CW/ $\overline{RTZ}$	PIN	NIN	VPP to TX	VNN to TX	TX to RGP	TX to RGN
<b>B-Mode with RTZ</b>	1	0	0	0	OFF	OFF	<b>ON</b>	<b>ON</b>
		0	1	0	<b>ON</b>	OFF	OFF	OFF
		0	0	1	OFF	<b>ON</b>	OFF	OFF
		0	1	1	OFF	OFF	OFF	OFF
<b>CW-Mode</b>	1	1	0	0	OFF	OFF	OFF	OFF
		1	1	0	OFF	OFF	<b>ON</b>	OFF
		1	0	1	OFF	OFF	OFF	<b>ON</b>
		1	1	1	OFF	OFF	OFF	OFF
<b>Disable</b>	0	X	X	X	OFF	OFF	OFF	OFF

**Note:**

When CW/ $\overline{RTZ}$  = 0 (in B-Mode) must be  $0 \leq V_{RGP} \leq +0.5V$  and  $0 \geq V_{RGN} \geq -0.5V$

When CW/ $\overline{RTZ}$  = 1 (in CW-Mode) must be  $0 \leq V_{RGP} \leq +5.5V$  and  $0 \geq V_{RGN} \geq -5.5V$

# Switch Timing and Delay Test



## Pin Description

Pin	Name	Description
1	EN	Chip power enable Hi = ON, Low = OFF
2	CW/RTZ	B-Scan or CWD mode control pin, see Control Logic Table
3	NIN1	Input logic control signal for channel 1
4	PIN1	Input logic control signal for channel 1
5	NIN2	Input logic control signal for channel 2
6	PIN2	Input logic control signal for channel 2
7	AGND	Digital logic circuit ground (0V)
8	NIN3	Input logic control signal for channel 3
9	PIN3	Input logic control signal for channel 3
10	NIN4	Input logic control signal for channel 4
11	PIN4	Input logic control signal for channel 4
12	VDD	Positive voltage power supply (+5.0V)
13	LR	Built-in linear regulators power turned on (enabled) when LR = 1 and EN = 1 Built-in linear regulators power turned off (disabled) when EN = 0 or LR = 0
14	VDD	Positive voltage power supply (+5.0V)
15	VDD	
16	VLL	Logic "1" voltage reference input (+2.5 to +5V)
17	AGND	Digital logic circuit ground (0V)
18	VDD	Positive voltage power supply (+5.0V)
19	DGND	Driver and level translator circuit ground return (0V)
20	VSS	Negative voltage power supply (-5.0V)
21	CPF	VPP to VPF decoupling capacitor (low voltage, 0.22 to 0.47 $\mu$ F 10V) See Note 1
22	VPP	Positive high voltage power supply (+5.0 to +70V)
23	VPP	
24	CGP	CGP to RGP decoupling capacitor (low voltage, 0.47 $\mu$ F 10V)
25	RGP	Common return ground or positive CW power supply. When CW/RTZ = 0 (in B-Mode) must be $0 \leq V_{RGP} \leq +0.5V$ . When CW/RTZ = 1 (in CW-Mode) must be $0 \leq V_{RGP} \leq +5.5V$ .
26	RGP	
27	CGN	CGN to RGN decoupling capacitor (low voltage, 0.47 $\mu$ F 10V)
28	RGN	Common return ground or positive CW power supply. When CW/RTZ = 0 (in B-Mode) must be $0 \geq V_{RGN} \geq -0.5V$ . When CW/RTZ = 1 (in CW-Mode) must be $0 \geq V_{RGN} \geq -5.5V$ .
29	RGN	
30	CNF	VNF to VNN decoupling capacitor (low voltage, 0.22 to 0.47 $\mu$ F 10V) See Note 1
31	VNN	Negative high voltage power supply (-5.0 to -70V)
32	VNN	
33	TX4	Transmit pulser output for channel 4
34	TX4	

## Pin Description (cont.)

Pin	Name	Description
35	RGND	Bleeding resistor common return ground
36	RGND	
37	TX3	Transmit pulser output for channel 3
38	TX3	
39	RGND	Bleeding resistor common return ground
40	RGND	
41	RGND	
42	RGND	
43	TX2	Transmit pulser output for channel 2
44	TX2	
45	RGND	Bleeding resistor common return ground
46	RGND	
47	TX1	Transmit pulser output for channel 1
48	TX1	
49	VNN	Negative high voltage power supply (-5.0 to -70V)
50	VNN	
51	CNF	VNF to VNN decoupling capacitor (low voltage, 0.22 to 0.47 $\mu$ F 10V) See Note 1
52	RGN	Common return ground or negative CW power supply. (0V or -1.0 to -5.5V)
53	RGN	
54	CGN	CGN to RGN decoupling capacitor (low voltage, 2.2 $\mu$ F 10V)
55	RGP	Common return ground or positive CW power supply.(0V or +1.0 to +5.5V)
56	RGP	
57	CGP	CGP to RGP decoupling capacitor (low voltage, 2.2 $\mu$ F 10V)
58	VPP	Positive high voltage power supply (+5 to +70V)
59	VPP	
60	CPF	CGP to RGP decoupling capacitor (low voltage, 0.22 to 0.47 $\mu$ F 10V) See Note 1
61	VSS	Negative voltage power supply (-5.0V)
62	DGND	Driver and level translator circuit ground return (0V)
63	VDD	Positive voltage power supply (+5.0V)
64	AGND	Digital logic circuit ground (0V)
(Thermal Pad) VSUB		Substrate connect to ground (0V)

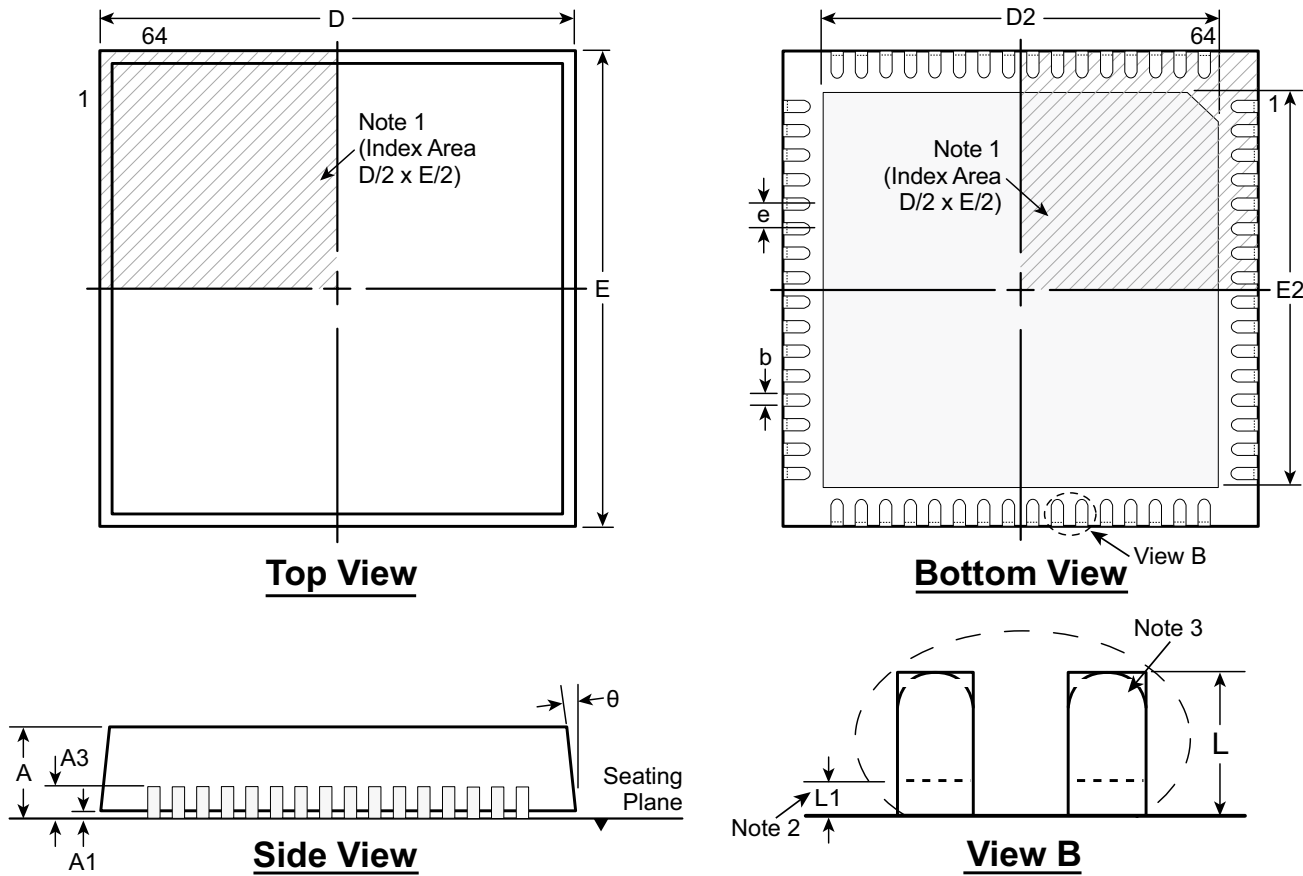
**Note 1:**

To minimize the rush-in current, nominal capacitor values for the CPF to VPP pins and the CNF to VNN pins should not exceed 0.47 $\mu$ F.



# 64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	8.85*	6.00	8.85*	6.00	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	9.00	7.70*	9.00	7.70*		0.40	-	-
	MAX	1.00	0.05		0.30	9.15*	7.80†	9.15*	7.80†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VMMD-4, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-64QFNK69X9P050, Version B020112

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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