

RJK0652DPB

60V, 35A, 7.0mΩ max.

Silicon N Channel Power MOS FET
Power Switching

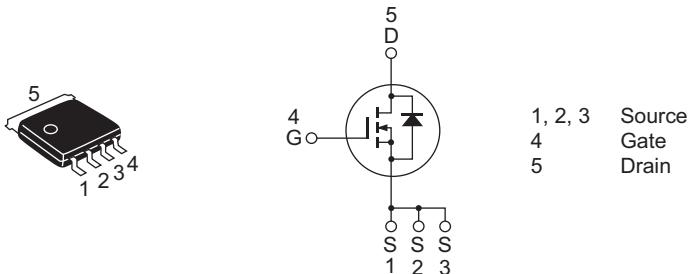
R07DS0077EJ0200
Rev.2.00
Apr 09, 2013

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 5.5 \text{ m}\Omega \text{ typ. (at } V_{GS} = 10 \text{ V)}$
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



Application

- Switching Mode Power Supply

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	35	A
Drain peak current	I _{D(pulse)} ^{Note1}	140	A
Body-drain diode reverse drain current	I _{DR}	35	A
Avalanche current	I _{AP} ^{Note 2}	17.5	A
Avalanche energy	E _{AS} ^{Note 2}	23	mJ
Channel dissipation	P _{ch} ^{Note3}	55	W
Channel to Case Thermal Resistance	θ _{ch-C}	2.27	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

3. T_c = 25°C

This product is for the low voltage drive (≤ 10V).

If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage (V_{GS(off)}) which characteristics has been improved.

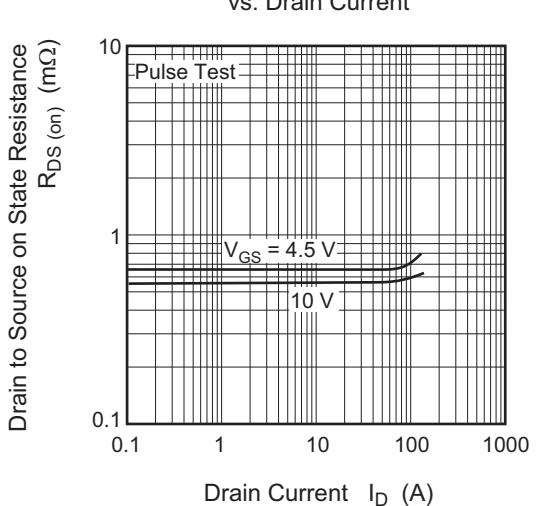
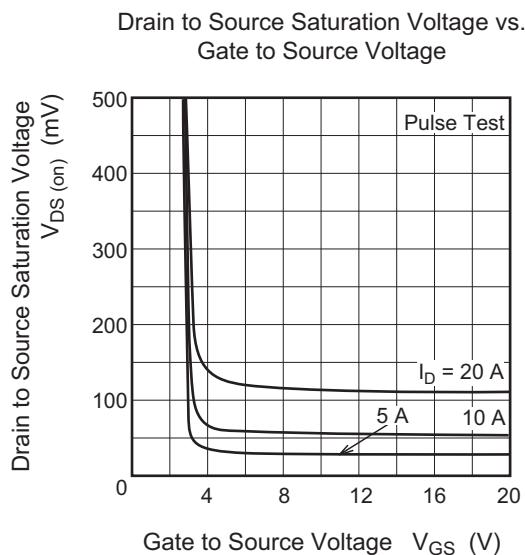
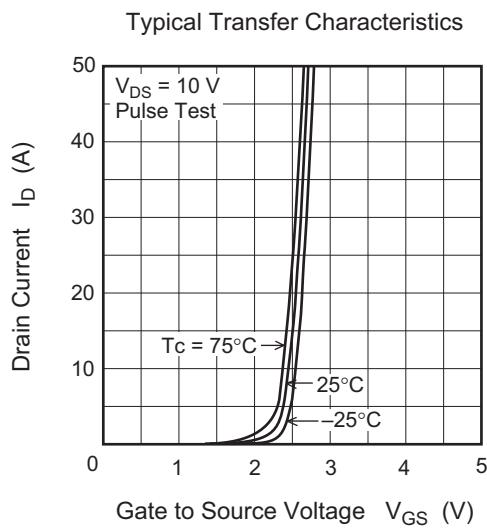
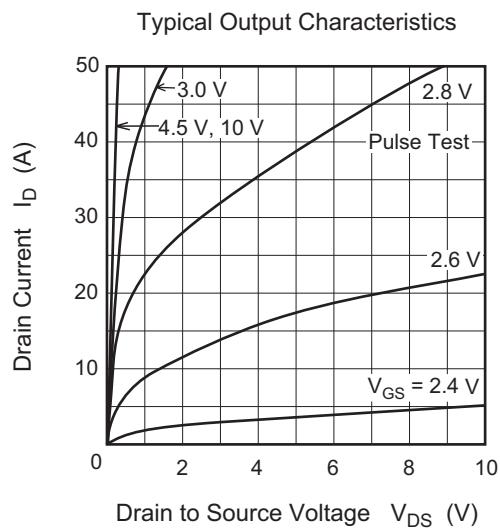
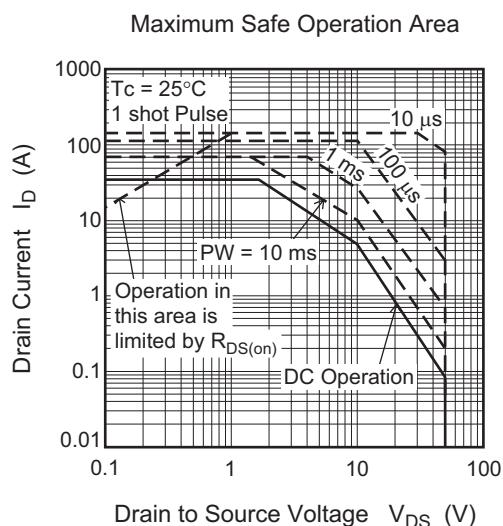
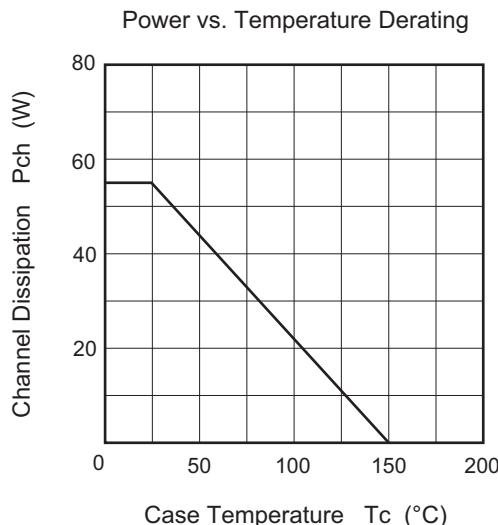
Electrical Characteristics

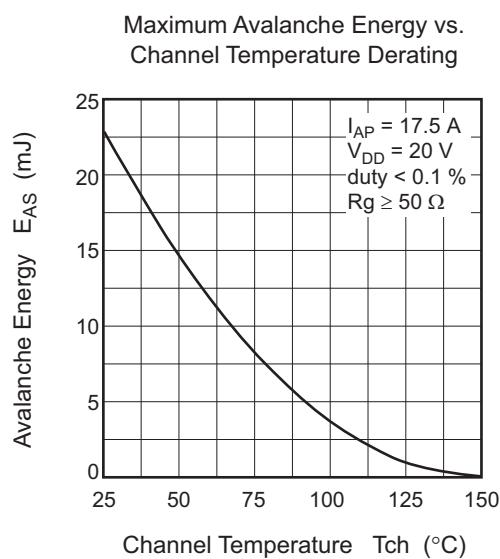
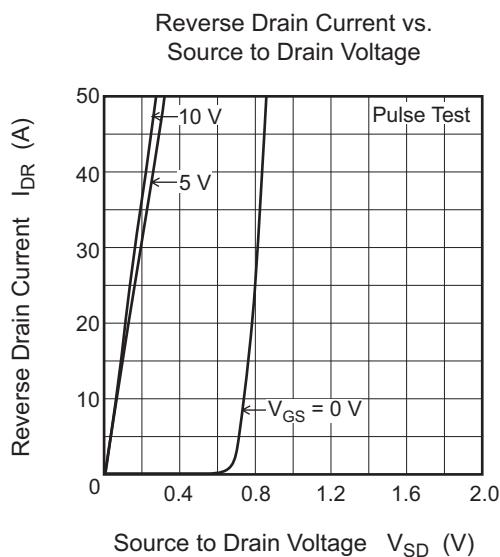
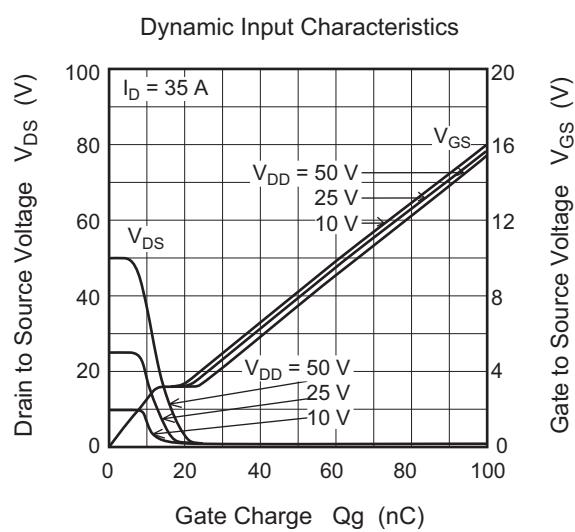
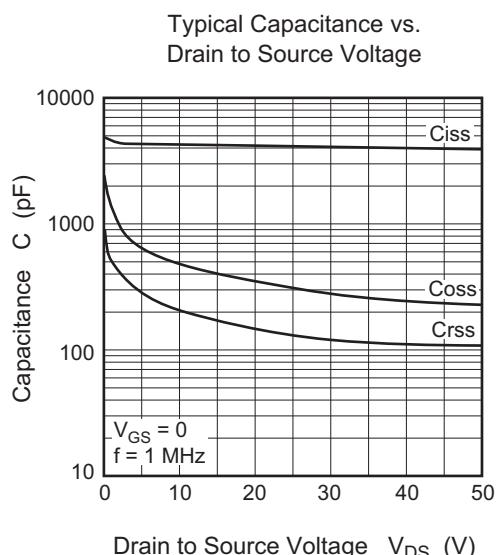
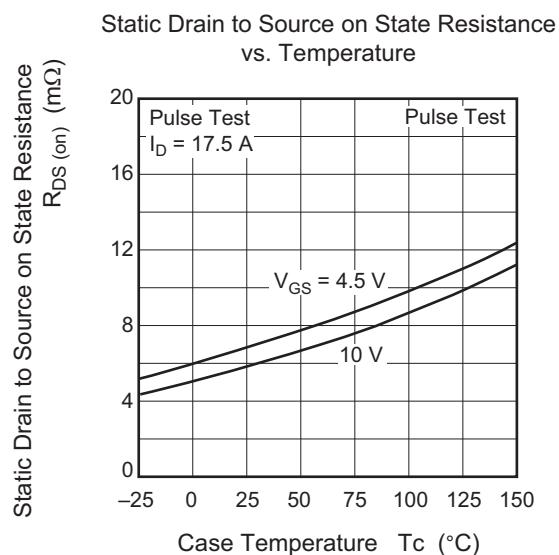
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.5	7.0	$\text{m}\Omega$	$I_D = 17.5 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	6.5	9.0	$\text{m}\Omega$	$I_D = 17.5 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	54	—	S	$I_D = 17.5 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4100	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	485	—	pF	
Reverse transfer capacitance	C_{rss}	—	200	—	pF	
Gate Resistance	R_g	—	0.4	—	Ω	
Total gate charge	Q_g	—	29	—	nC	$V_{DD} = 25 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 35 \text{ A}$
Gate to source charge	Q_{gs}	—	13	—	nC	
Gate to drain charge	Q_{gd}	—	8.8	—	nC	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10 \text{ V}, I_D = 17.5 \text{ A},$ $V_{DD} \geq 30 \text{ V}, R_L = 1.71 \Omega,$ $R_g = 4.7 \Omega$
Rise time	t_r	—	7.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	54	—	ns	
Fall time	t_f	—	10	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.83	1.1	V	$I_F = 35 \text{ A}, V_{GS} = 0 \text{ V}$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 35 \text{ A}, V_{GS} = 0 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

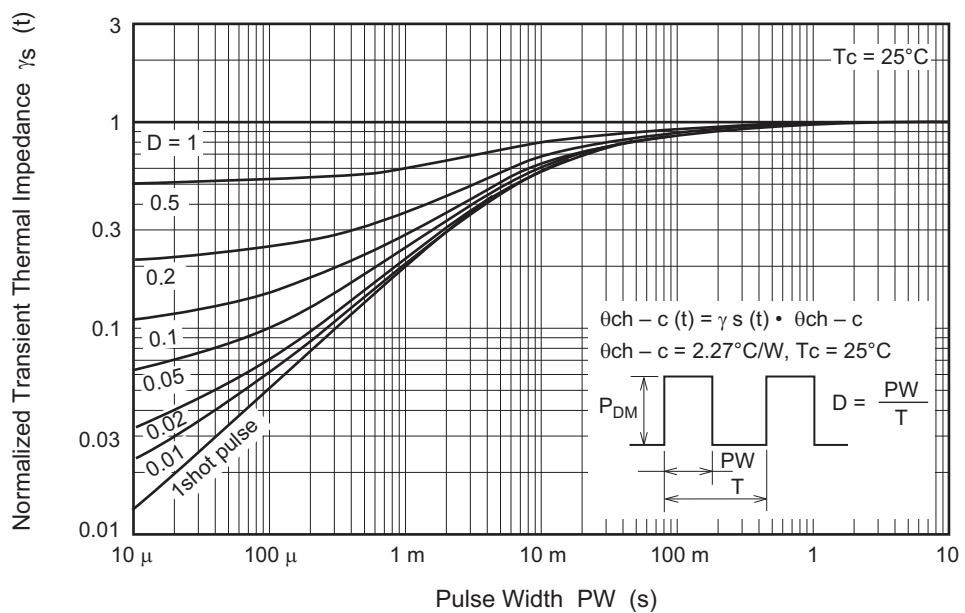
Notes: 4. Pulse test

Main Characteristics

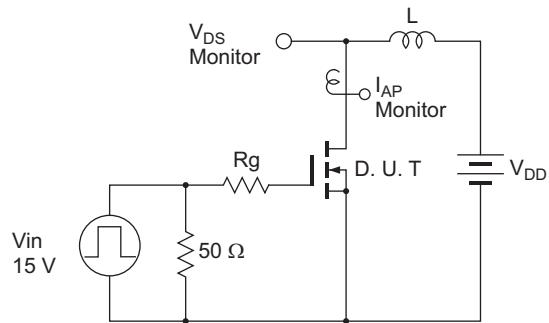




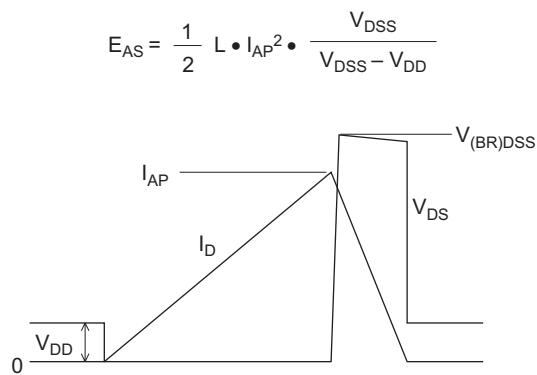
Normalized Transient Thermal Impedance vs. Pulse Width



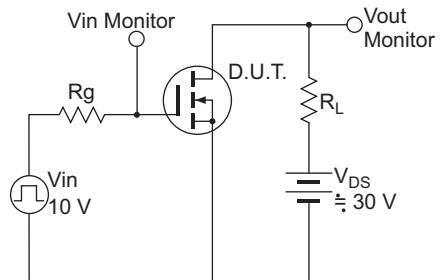
Avalanche Test Circuit



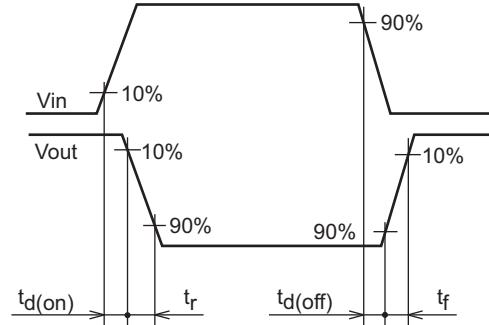
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g	
(Ni/Pd/Au plating)					

Ordering Information

Part No.	Quantity	Shipping Container
RJK0652DPB-00-J5	2500 pcs	Taping

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