

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- $V_{DD} = 2.4$ to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed ($0.03125 \mu\text{s}$: @ 32 MHz operation with high-speed on-chip oscillator or PLL clock)^{Note} to ultra-low speed ($1 \mu\text{s}$: @ 1 MHz operation with high-speed on-chip oscillator or PLL clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register $\times 8$) $\times 4$ banks
- On-chip RAM: 8 KB

Note For industrial applications (M; $T_A = -40$ to $+125^\circ\text{C}$): $0.04167 \mu\text{s}$ @ 24 MHz operation with high-speed on-chip oscillator or PLL clock

Code flash memory

- Code flash memory: 32 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD} = 2.4$ to 5.5 V

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy:
 $\pm 2.0\%$ ($V_{DD} = 2.4$ to 5.5 V, $T_A = -40$ to $+105^\circ\text{C}$)
 $\pm 3.0\%$ ($V_{DD} = 2.4$ to 5.5 V, $T_A = -40$ to $+125^\circ\text{C}$)

Operating ambient temperature

- $T_A = -40$ to $+105^\circ\text{C}$ (G: Industrial applications)
- $T_A = -40$ to $+125^\circ\text{C}$ (M: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 7 levels)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event link controller (ELC)

- Event signals of 16 types can be linked to the specified peripheral function.

Serial interfaces

- CSI: 2 channels
- UART: 2 channels (UART with LIN-bus supported: 1 channel)
- I²C/simplified I²C: 2 channels

Timer

- 16-bit timer: 8 channels
(Timer Array Unit (TAU): 6 channels, timer RJ: 1 channel, timer RG: 1 channel)
- Interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

Analog front-end (AFE) power supply

- Sensor power supply (SBIAS) output: 0.5 V to 2.2 V

24-bit $\Delta\Sigma$ A/D converter with programmable gain instrumentation amplifier

- 24-bit second-order $\Delta\Sigma$ A/D converter ($AV_{DD} = 2.7$ to 5.5 V)
- SNDR: 85 dB (TYP.)
- Output data rate:
 - 488 sps to 15.625 ksps in normal mode
 - 61 sps to 1.953 ksps in low power mode
- Programmable gain instrumentation amplifier input: 3 or 4 channels
(differential input mode or single-ended input mode can be specified for each input channel)
- DAC for offset adjustment
- Variable gain: x1 to x64
- On-chip temperature sensor

10-bit A/D converter

- 8-bit/10-bit successive approximation A/D converter ($AV_{DD} = 2.7$ to 5.5 V)
- Analog input: 8 or 10 channels, sensor power supply (SBIAS), and internal reference voltage
- Internal reference voltage (1.45 V)

Configurable amplifier

- Matrix configuration that consists of 3 operational amplifier channels and a configurable switch ($AV_{DD} = 2.7$ to 5.5 V)
- Can be used as a 2- or 3-channel general operational amplifier
- Operational amplifier output: 3 channels
- General-purpose Analog I/O ports: 5 or 6 channels
- Offset voltage calibration

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/I1E	
			32 pins	36 pins
32 KB	4 KB	8 KB	R5F11CBC	R5F11CCC

D/A converter

- 12-bit R-2R resistor ladder type D/A converter ($AV_{DD} = 2.7$ to 5.5 V)
- Analog output: 1 channel (via configurable amplifier)

I/O port

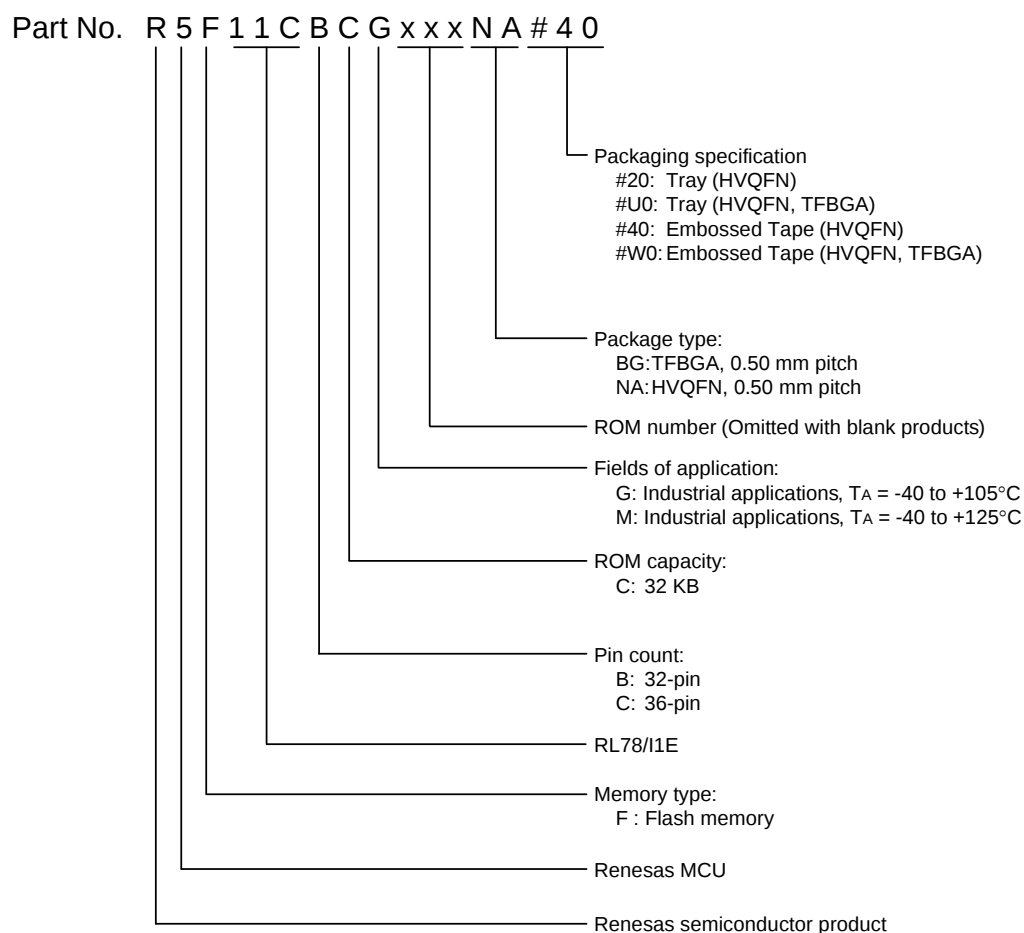
- CMOS I/O: 10 to 14 (N-ch open drain I/O [withstanding voltage of V_{DD}]: 6, CMOS I/O: 7 to 11, CMOS input: 3)
- Can be set to TTL input buffer and on-chip pull-up resistor
- Different potential interface: Can connect to a 2.5/3 V device
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/I1E



Pin count	Package	Fields of Application Note	Ordering Part Number
32 pins	32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)	G	R5F11CBCGNA#20 R5F11CBCGNA#40
		M	R5F11CBCMNA#U0 R5F11CBCMNA#W0
36 pins	36-pin plastic TFBGA (4 × 4 mm, 0.5 mm pitch)	G	R5F11CCCGBG#U0 R5F11CCCGBG#W0
		M	R5F11CCCMBG#U0 R5F11CCCMBG#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/I1E**.

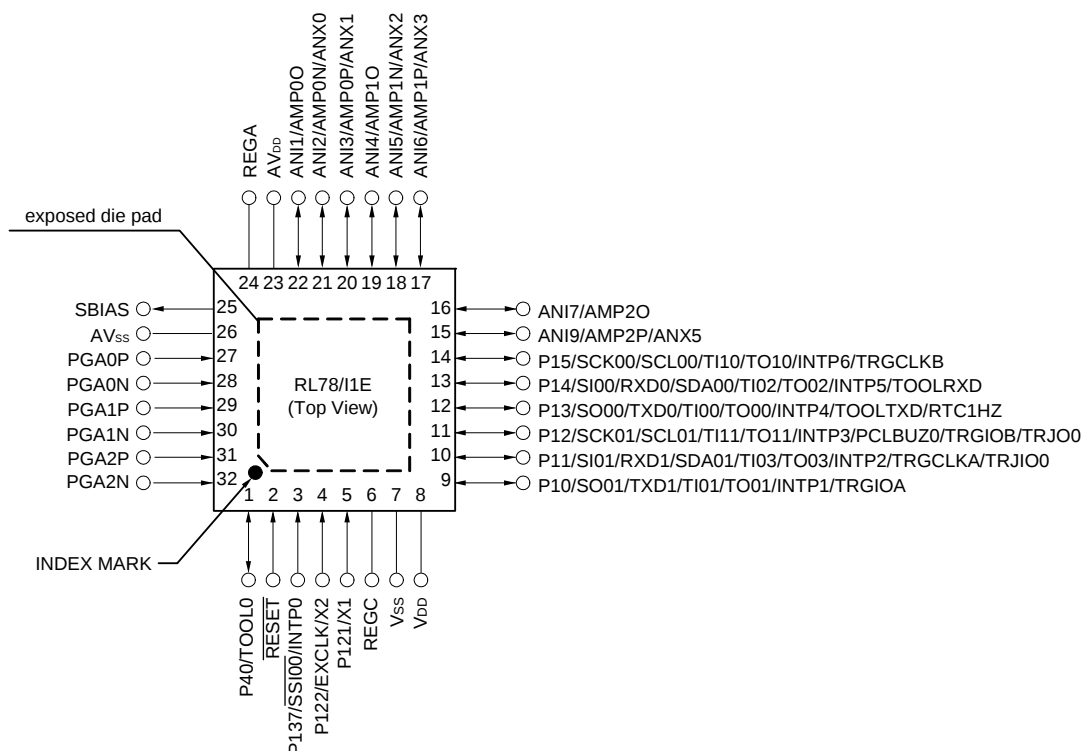
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 32-pin products

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- 32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to the Vss pin via a capacitor (0.47 to 1 μ F).

Caution 2. Connect the REGA pin to the AVss pin via a capacitor (0.22 μ F).

Caution 3. Make the AVss pin the same potential as the Vss pin.

Caution 4. Make the AVDD pin the same potential as the VDD pin.

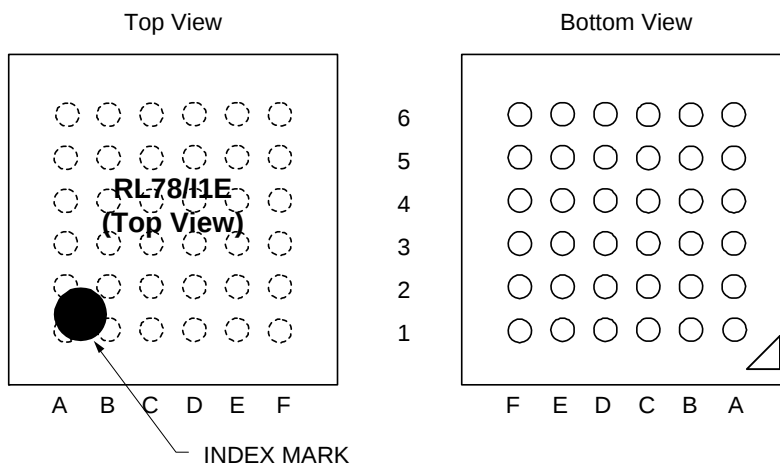
Caution 5. Connect the SBIAS pin to the AVss pin via a capacitor (0.22 μ F).

Remark 1. It is recommended to connect an exposed die pad to Vss.

1.3.2 36-pin products

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- 36-pin plastic TFBGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	PGA2P	PGA1N	PGA1P	PGA0P	PGA3P	AVss	6
5	PGA2N	P40/TOOL0	PGA0N	PGA3N	REGA	SBIAS	5
4	RESET	P137/SSI00/ INTP0	P11/SI01/RXD1/ SDA01/TI03/ TO03/INTP2/ TRGCLKA/ TRJIO0	P12/SCK01/ SCL01/TI11/ TO11/INTP3/ PCLBUZ0/ TRGIOB/TRJO0	ANI0	AVDD	4
3	P122/EXCLK/X2	P15/SCK00/ SCL00/TI10/ TO10/INTP6/ TRGCLKB	P10/SO01/TXD1/ TI01/TO01/ INTP1/TRGIOA	ANI3/AMP0P/ ANX1	ANI2/AMP0N/ ANX0	ANI1/AMP0O	3
2	P121/X1	REGC	P14/SI00/RXD0/ SDA00/TI02/ TO02/INTP5/ TOOLRXD	P41/ANI6/ AMP1P/ANX3	P42/ANI5/ AMP1N/ANX2	ANI4/AMP1O	2
1	VDD	Vss	P13/SO00/TXD0/ TI00/TO00/INTP4/ TOOLTXD/ RTC1HZ	P16/INTP7/ANI9/ AMP2P/ANX5	P17/ANI8/ AMP2N/ANX4	ANI7/AMP2O	1
	A	B	C	D	E	F	

Caution 1. Connect the REGC pin to the Vss pin via a capacitor (0.47 to 1 μ F).

Caution 2. Connect the REGA pin to the AVss pin via a capacitor (0.22 μ F).

Caution 3. Make the AVss pin the same potential as the Vss pin.

Caution 4. Make the AVDD pin the same potential as the VDD pin.

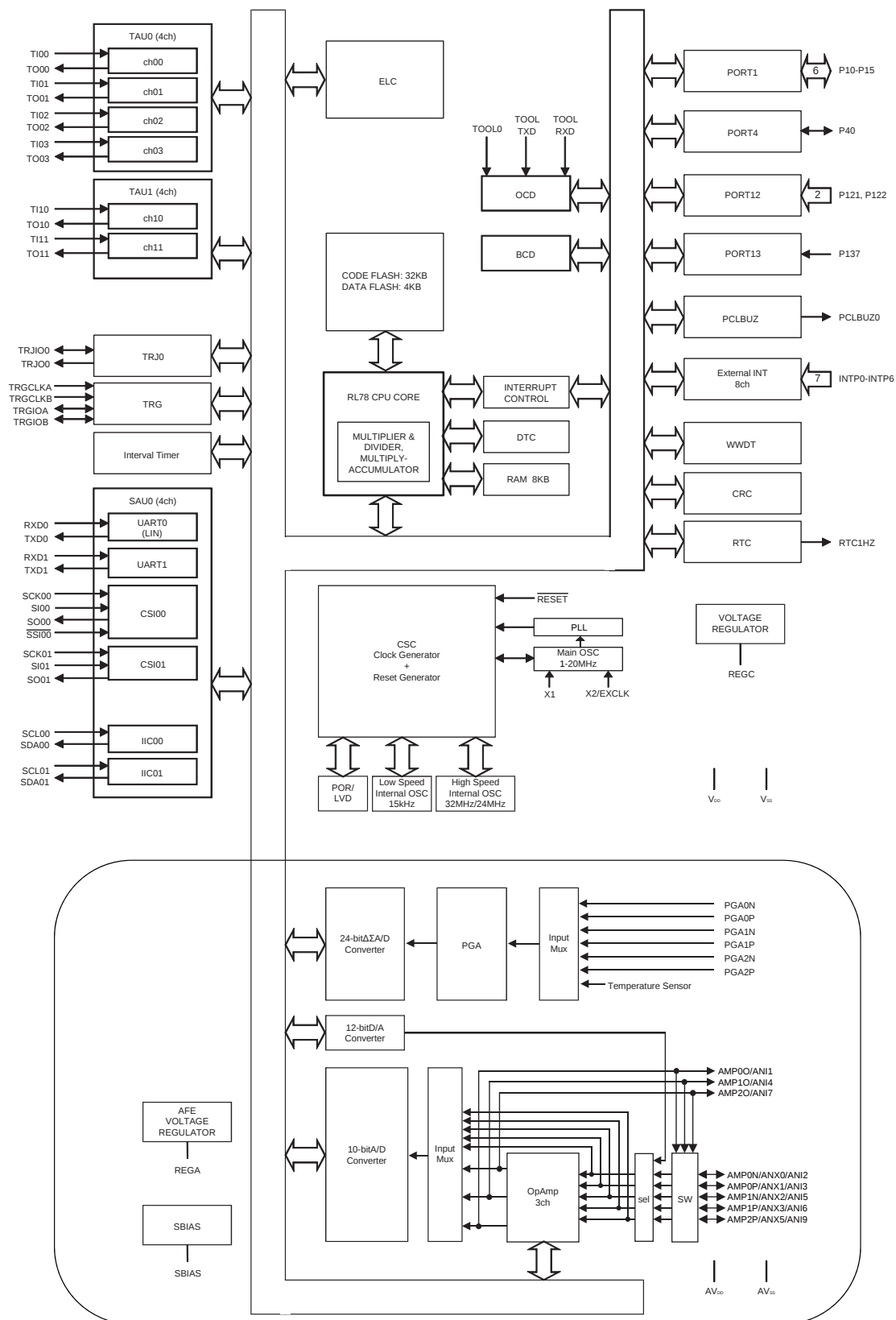
Caution 5. Connect the SBIAS pin to the AVss pin via a capacitor (0.22 μ F).

1.4 Pin Identification

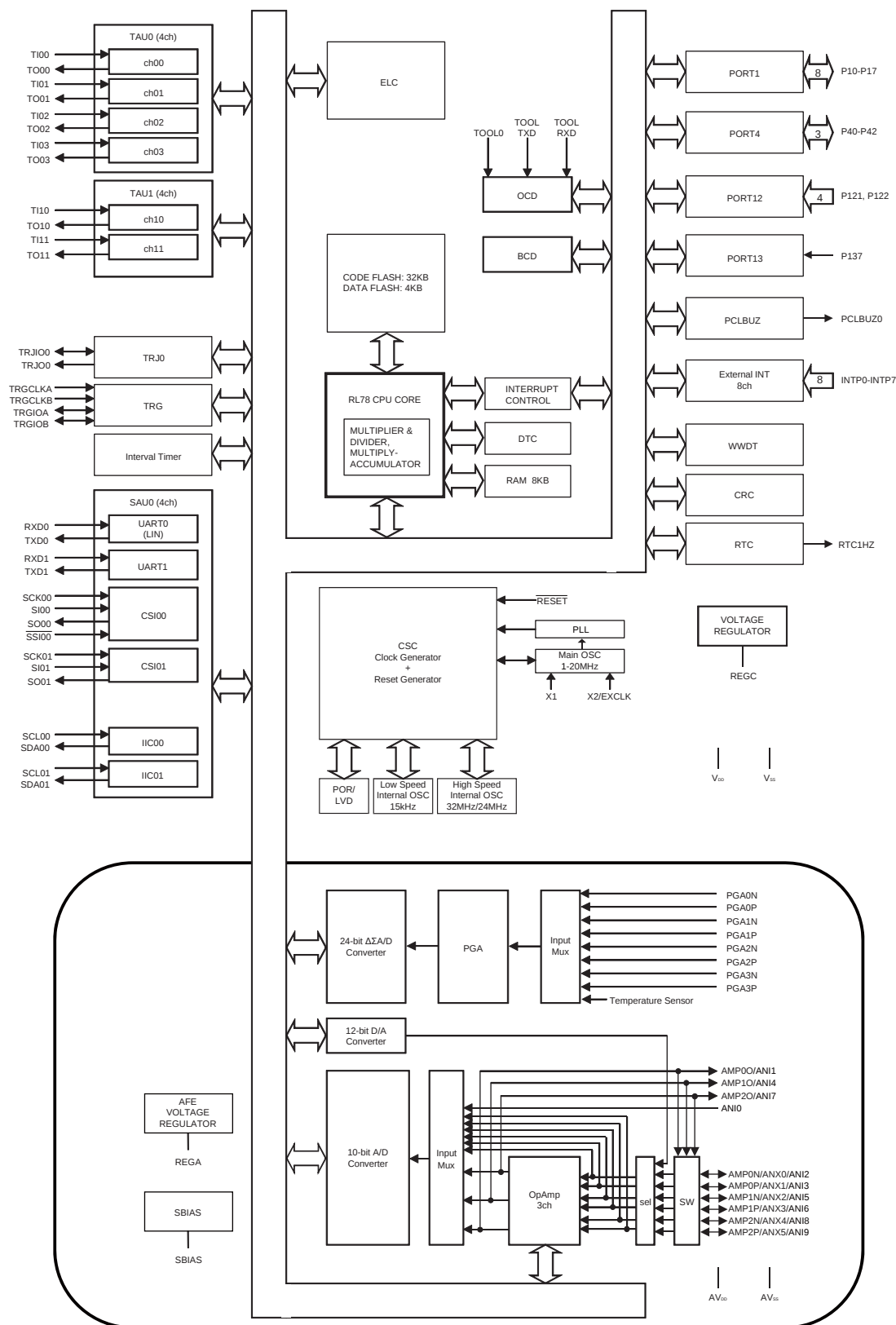
ANI0 to ANI9:	Analog input	RESET:	Reset
AMP0P to AMP2P:	Operational amplifier positive input	REGA:	Regulator capacitance for analog
AMP0N to AMP2N:	Operational amplifier negative input	REGC:	Regulator capacitance
AMP0O to AMP2O:	Operational amplifier output	RTC1HZ:	Real-time clock correction
ANX0 to ANX5:	General-purpose analog ports for operational amplifier	RxD0, RxD1:	Receive data
AVDD:	Power supply for analog	SBIAS:	Bias output for MEMS sensor
AVSS:	Ground for analog	SCK00, SCK01:	Serial clock input/output
EXCLK:	External clock input (main system clock)	SCL00, SCL01:	Serial clock output
INTP0 to INTP7:	External interrupt input	SI00, SI01:	Serial data input
P10 to P17:	Port 1	SO00, SO01:	Serial data output
P40 to P42:	Port 4	TI00 to TI03, TI10, TI11:	Timer input
P121, P122:	Port 12	TO00 to TO03, TO10, TO11,	Timer output
P137:	Port 13	TRJ00:	
PCLBUZ0:	Programmable clock output/ buzzer output	TOOL0:	Data input/output for tools
PGA0N to PGA3N:	PGA negative analog input	TOOLRxD, TOOLTxD:	Data input/output for external devices
PGA0P to PGA3P:	PGA positive analog input	TRGCLKA, TRGCLKB:	Timer external clock input
		TRGIOA, TRGIOB, TRJIO0:	Timer input/output
		TxD0, TxD1:	Transmit data
		VDD:	Power supply
		VSS:	Ground
		X1, X2:	Crystal oscillator (main system clock)

1.5 Block Diagram

1.5.1 32-pin products



1.5.2 36-pin products



1.6 Outline of Functions

[32-pin, 36-pin products]

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Item		32-pin	36-pin
		R5F11CBC	R5F11CCC
Code flash memory		32 KB	
Data flash memory		4 KB	
RAM		8 KB	
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: $V_{DD} = 2.7$ to 5.5 V, 1 to 16 MHz: $V_{DD} = 2.4$ to 2.7 V	
	High-speed on-chip oscillator clock (f_{IH})	1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V) ^{Note 1} 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V)	
	PLL clock (f_{PLL} divided by 2, 4, or 8)	3 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V) ^{Note 2} 3 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V)	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μ s (high-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation) ^{Note 3}	
		0.03125 μ s (PLL clock: $f_{PLL} = 64$ MHz, $f_{IH} = 32$ MHz operation) ^{Note 4}	
		0.05 μ s (high-speed system clock: $f_{MX} = 20$ MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	10	14
	CMOS I/O	7	11
	CMOS input	3	3
Timer	16-bit timer	8 channels (TAU: 6 channels, Timer RJ: 1 channel, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	Interval timer	1 channel	
	Timer output	Timer outputs: 10 channels PWM outputs: 9 channels	
	RTC output	1	
Clock output/buzzer output		1	
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation)	
8/10-bit A/D converter		8 channels	10 channels
Serial interface		CSI: 2 channels/UART: 2 channels (UART supporting LIN-bus: 1 channel)/simplified I ² C: 2 channels	

Note 1. 1 to 24 MHz ($V_{DD} = 2.7$ to 5.5 V) for M products (industrial applications, $T_A = -40$ to $+125^\circ\text{C}$)

Note 2. 3 to 24 MHz ($V_{DD} = 2.7$ to 5.5 V) for M products (industrial applications, $T_A = -40$ to $+125^\circ\text{C}$)

Note 3. 0.04167 μ s (high-speed on-chip oscillator clock: $f_{IH} = 24$ MHz operation) for M products (industrial applications, $T_A = -40$ to $+125^\circ\text{C}$)

Note 4. 0.04167 μ s (PLL clock: $f_{PLL} = 64$ MHz, $f_{IH} = 24$ MHz operation) for M products (industrial applications, $T_A = -40$ to $+125^\circ\text{C}$)

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Item		32-pin	36-pin
		R5F11CBC	R5F11CCC
Data transfer controller (DTC)		22 sources	
Event link controller (ELC)		Event input: 16 Event trigger output: 7	
Vectored interrupt sources	Internal	23	23
	External	7	8
$\Delta\Sigma$ A/D converter	24-bit	3 channels	4 channels
	AFE temperature sensor	1 channel	
Operational amplifier	3-pin	3 channels Note 1	3 channels
	General-purpose port	5 channels	6 channels
D/A converter	12-bit	1 channel	
Reset		- Reset by $\overline{\text{RESET}}$ pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution Note 2 - Internal reset by RAM parity error - Internal reset by illegal-memory access	
Power-on-reset circuit		- Power-on-reset: 1.56 $\pm$ 0.03 V - Power-down-reset: 1.55 $\pm$ 0.03 V	
Voltage detector		- At rise: 2.55 V to 4.64 V (7 steps) - At fall: 2.61 V to 4.74 V (7 steps)	
On-chip debug function		Provided	
Power supply voltage		$V_{DD} = 2.4$ to 5.5 V	
Operating ambient temperature		$T_A = -40$ to $+105^\circ\text{C}$ (G: Industrial applications), $T_A = -40$ to $+125^\circ\text{C}$ (M: Industrial applications)	

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- Note 1.** When each of the 3 channels is in use as an independent amplifier, at least one channel must be in a voltage follower configuration.
- Note 2.** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)

This chapter describes the electrical specifications for the products “G: Industrial applications (T_A = -40 to +105°C)”.

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product.

Caution 3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products “M: Industrial applications”. For details, refer to **2.1** to **2.10**.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings

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Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	AV _{DD}	AV _{DD} = V _{DD}	-0.5 to +6.5	V
	AV _{SS}	AV _{SS} = V _{SS}	-0.5 to +0.3	V
REGC pin input voltage	V _I REGC	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 Note 1	V
REGA pin input voltage	V _I REGA	REGA	-0.3 to +2.8 and -0.3 to AV _{DD} + 0.3 Note 2	V
Input voltage	V _{I1}	P10 to P15, P40, P121, P122, P137, EXCLK, RESET	-0.3 to V _{DD} + 0.3 Note 3	V
Alternate-function pin input voltage	V _{I2}	P16, P17, P41, P42 (36-pin products only)	Digital input voltage	-0.3 to V _{DD} + 0.3 Note 3
			Analog input voltage	-0.3 to AV _{DD} + 0.3 Note 3
Analog input voltage	V _{IA}	PGA0P to PGA3P, PGA0N to PGA3N, ANI0 to ANI9, ANX0 to ANX5	-0.3 to AV _{DD} + 0.3 Note 3	V
Output voltage	V _{O1}	P10 to P15, P40	-0.3 to V _{DD} + 0.3 Note 3	V
Alternate-function pin output voltage	V _{O2}	P16, P17, P41, P42 (36-pin products only)	Digital output voltage	-0.3 to V _{DD} + 0.3 Note 3
			Analog output voltage	-0.3 to AV _{DD} + 0.3 Note 3
Analog output voltage	V _{OA}	SBIAS, AMP0O to AMP2O, ANX0 to ANX5	-0.3 to AV _{DD} + 0.3 Note 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the REGA pin to AV_{SS} via a capacitor (0.22 μF). This value regulates the absolute maximum rating of the REGA pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. V_{SS} is used as the reference voltage.

Absolute Maximum Ratings**(2/2)**

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P10 to P17, P40 to P42	-40	mA
		Total of all pins	P10 to P17, P41, P42 ^{Note}	-100	mA
Analog output current, high	IOHA	Per pin	AMP00 to AMP20	-12	mA
			ANX0 to ANX5	-0.12	mA
		Total of all pins	AMP00 to AMP20, ANX0 to ANX5	-18	mA
Output current, low	IOL1	Per pin	P10 to P17, P40 to P42	40	mA
		Total of all pins	P10 to P17, P41, P42 ^{Note}	100	mA
Analog output current, low	IOLA	Per pin	AMP00 to AMP20	12	mA
			ANX0 to ANX5	0.12	mA
		Total of all pins	AMP00 to AMP20, ANX0 to ANX5	18	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	Tstg			-65 to +150	°C

Note This indicates the total current value when P16, P17, P41, and P42 are used as digital input pins.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. V_{ss} is used as the reference voltage.

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f _{IH}	2.7 V ≤ VDD ≤ 5.5 V		1		32	MHz
		2.4 V ≤ VDD < 2.7 V		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-40 to +105°C	2.4 V ≤ VDD ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.2.3 PLL characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
PLL output frequency ^{Notes 1, 2, 3}	f _{PLL}	f _{MX} = 8 MHz	DSFRDIV = 0	DSCM = 0		48		MHz
				DSCM = 1		64		MHz
			DSFRDIV = 1	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
		f _{MX} = 4 MHz	DSFRDIV = 0	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
Lockup wait time		Time from when PLL output is enabled to when the phase is locked			40			μs
Interval wait time		Time from when the PLL stops operating to when the setting to start PLL operation is specified			4			μs
Setup wait time		Time required from when the PLL input clock stabilizes and the PLL setting is determined to when the PLL is activated			1			μs

Note 1. When using a PLL, input a clock of 4 MHz or 8 MHz to the PLL.

Note 2. Be sure to specify one of these settings when using a PLL.

Note 3. When using the PLL output as the CPU clock, f_{IH} is divided by 2, 4, or 8 according to the setting of the RDIV1 and RDIV0 bits.

2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

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Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P10 to P17 and P40 to P42 ^{Note 2}	-40°C < TA ≤ +85°C		-10.0 ^{Note 3}	mA
			85°C < TA ≤ 105°C		-3.0 ^{Note 3}	mA
		Total of P10 to P17, P41, and P42 ^{Note 2} (When duty ≤ 70% ^{Note 4})	4.0 V ≤ VDD ≤ 5.5 V -40°C < TA ≤ +85°C		-80.0	mA
			4.0 V ≤ VDD ≤ 5.5 V 85°C < TA ≤ 105°C		-30.0	mA
			2.7 V ≤ VDD < 4.0 V		-19.0	mA
			2.4 V ≤ VDD < 2.7 V		-10.0	mA
Output current, low ^{Note 1}	IOL1	Per pin for P10 to P17 and P40 to P42 ^{Note 2}	-40°C < TA ≤ +85°C		20.0 ^{Note 3}	mA
			85°C < TA ≤ 105°C		8.5 ^{Note 3}	mA
		Total of P10 to P17, P41, and P42 ^{Note 2} (When duty ≤ 70% ^{Note 4})	4.0 V ≤ VDD ≤ 5.5 V -40°C < TA ≤ +85°C		80.0	mA
			4.0 V ≤ VDD ≤ 5.5 V 85°C < TA ≤ 105°C		40.0	mA
			2.7 V ≤ VDD < 4.0 V		35.0	mA
			2.4 V ≤ VDD < 2.7 V		20.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pin to an output pin.

Note 2. This indicates the total current value when P16, P17, P41, and P42 are used as digital I/O ports. When using these pins as analog function (AFE) pins, refer to **2.1 Absolute Maximum Ratings**.

Note 3. Do not exceed the total current value.

Note 4. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

Example: n = 80% when IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(2/3)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P10 to P17 and P40 to P42	Normal input buffer	0.8 VDD		VDD	V
	VIH2	P11, P12, P14, P15	TTL input buffer, 4.0 V ≤ VDD ≤ 5.5 V	2.2		VDD	V
			TTL input buffer, 3.3 V ≤ VDD < 4.0 V	2.0		VDD	V
			TTL input buffer, 2.4 V ≤ VDD < 3.3 V	1.5		VDD	V
	VIH3	P121, P122, P137, EXCLK, RESET		0.8 VDD		VDD	V
Input voltage, low	VIL1	P10 to P17 and P40 to P42	Normal input buffer	0		0.2 VDD	V
	VIL2	P11, P12, P14, P15	TTL input buffer, 4.0 V ≤ VDD ≤ 5.5 V	0		0.8	V
			TTL input buffer, 3.3 V ≤ VDD < 4.0 V	0		0.5	V
			TTL input buffer, 2.4 V ≤ VDD < 3.3 V	0		0.32	V
	VIL3	P121, P122, P137, EXCLK, RESET		0		0.2 VDD	V
Output voltage, high	VOH1	P10 to P17 and P40 to P42	4.0 V ≤ VDD ≤ 5.5 V, TA = -40 to +85°C, IOH1 = -10.0 mA	VDD - 1.5			V
			4.0 V ≤ VDD ≤ 5.5 V, 85°C < TA ≤ 105°C, IOH1 = -3.0 mA	VDD - 0.7			V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -2.0 mA	VDD - 0.6			V
			2.4 V ≤ VDD ≤ 5.5 V, IOH1 = -1.5 mA	VDD - 0.5			V
Output voltage, low	VOL1	P10 to P17 and P40 to P42	4.0 V ≤ VDD ≤ 5.5 V, TA = -40 to +85°C, IOL1 = 20.0 mA			1.3	V
			4.0 V ≤ VDD ≤ 5.5 V, 85°C < TA ≤ 105°C, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA			0.4	V
			2.4 V ≤ VDD ≤ 5.5 V, IOL1 = 0.6 mA			0.4	V

Caution The maximum VIH value on P10 to P15 is VDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(3/3)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P10 to P17, and P40 to P42	V _I = V _{DD}			1	μA
	ILI _{H2}	P137, $\overline{\text{RESET}}$	V _I = V _{DD}			1	μA
	ILI _{H3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{DD}	In input port mode or when using external clock input		1	μA
				When a resonator is connected		10	μA
Input leakage current, low	ILI _{L1}	P10 to P17, and P40 to P42	V _I = V _{SS}			-1	μA
	ILI _{L2}	P137, $\overline{\text{RESET}}$	V _I = V _{SS}			-1	μA
	ILI _{L3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{SS}	In input port mode or when using external clock input		-1	μA
				When a resonator is connected		-10	μA
On-chip pull-up resistance	R _U	P10 to P15, P40	V _I = V _{SS} , in input port mode	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode Note 2	fHOCO = 32 MHz, fMAIN = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1		mA
					VDD = 3.0 V		2.1		
			fHOCO = 32 MHz, fMAIN = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.7	mA
					VDD = 3.0 V		4.8	8.7	
			fHOCO = 24 MHz, fMAIN = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.7	
					VDD = 3.0 V		3.8	6.7	
			fHOCO = 16 MHz, fMAIN = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.9	
					VDD = 3.0 V		2.8	4.9	
			fMX = 20 MHz, fMAIN = 20 MHz Note 4, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.7	mA
					Resonator connection		3.5	5.8	
			fMX = 20 MHz, fMAIN = 20 MHz Note 4, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.7	
					Resonator connection		3.5	5.8	
			fMX = 10 MHz, fMAIN = 10 MHz Note 4, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.4	
					Resonator connection		2.1	3.5	
			fMX = 10 MHz, fMAIN = 10 MHz Note 4, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.4	
					Resonator connection		2.1	3.5	
			fMX = 8 MHz, fMAIN = 32 MHz Note 5, VDD = 5.0 V	Normal operation	Square wave input		5.2	9.2	mA
					Resonator connection		5.3	9.3	
			fMX = 8 MHz, fMAIN = 32 MHz Note 5, VDD = 3.0 V	Normal operation	Square wave input		5.2	9.2	
					Resonator connection		5.3	9.3	
			fMX = 8 MHz, fMAIN = 24 MHz Note 5, VDD = 5.0 V	Normal operation	Square wave input		5.1	9.1	
					Resonator connection		5.2	9.2	
			fMX = 8 MHz, fMAIN = 24 MHz Note 5, VDD = 3.0 V	Normal operation	Square wave input		5.1	9.1	
					Resonator connection		5.2	9.2	

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RTC, interval timer, watchdog timer, LVD circuit, AFE, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. The relationship between the operation voltage range and the CPU operating frequency is as below.

2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 32 MHz

2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz

Note 3. When the high-speed system clock is stopped

Note 4. When the high-speed on-chip oscillator and the PLL are stopped

Note 5. When the high-speed on-chip oscillator is stopped and the PLL is operating

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency

Remark 3. fMAIN: Main system clock frequency

Remark 4. The temperature condition for the TYP. value is TA = 25°C

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode Note 3	fHOCO = 32 MHz, fMAIN = 32 MHz Note 4	VDD = 5.0 V		0.54	3.67	mA		
				VDD = 3.0 V		0.54	3.67			
			fHOCO = 24 MHz, fMAIN = 24 MHz Note 4	VDD = 5.0 V		0.44	2.85			
				VDD = 3.0 V		0.44	2.85			
			fHOCO = 16 MHz, fMAIN = 16 MHz Note 4	VDD = 5.0 V		0.40	2.08			
				VDD = 3.0 V		0.40	2.08			
			fMX = 20 MHz, fMAIN = 20 MHz Note 5, VDD = 5.0 V	Square wave input		0.28	2.45	mA		
				Resonator connection		0.49	2.57			
			fMX = 20 MHz, fMAIN = 20 MHz Note 5, VDD = 3.0 V	Square wave input		0.28	2.45			
				Resonator connection		0.49	2.57			
			fMX = 10 MHz, fMAIN = 10 MHz Note 5, VDD = 5.0 V	Square wave input		0.19	1.28		mA	
				Resonator connection		0.30	1.36			
			fMX = 10 MHz, fMAIN = 10 MHz Note 5, VDD = 3.0 V	Square wave input		0.19	1.28			
				Resonator connection		0.30	1.36			
			fMX = 8 MHz, fMAIN = 32 MHz Note 6, VDD = 5.0 V	Square wave input		0.91	4.17	mA		
				Resonator connection		1.01	4.27			
				fMX = 8 MHz, fMAIN = 32 MHz Note 6, VDD = 3.0 V	Square wave input		0.91		4.17	
					Resonator connection		1.01		4.27	
				fMX = 8 MHz, fMAIN = 24 MHz Note 6, VDD = 5.0 V	Square wave input		0.76		3.27	
					Resonator connection		0.86		3.37	
			fMX = 8 MHz, fMAIN = 24 MHz Note 6, VDD = 3.0 V	Square wave input		0.76	3.27			
				Resonator connection		0.86	3.37			
	IDD3 Note 7	STOP mode	TA = -40°C				0.38		1.14	μA
			TA = +25°C				0.50		1.14	
			TA = +50°C				0.66		4.52	
			TA = +70°C				1.04		7.98	
			TA = +85°C				2.92	16.0		
			TA = +105°C				11.0	100.0		

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RTC, interval timer, watchdog timer, LVD circuit, AFE, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during writing to the data flash.

Note 2. During HALT instruction execution from flash memory

Note 3. The relationship between the operation voltage range and the CPU operating frequency is as below.

2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 32 MHz

2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz

Note 4. When the high-speed system clock is stopped

Note 5. When the high-speed on-chip oscillator and the PLL are stopped

Note 6. When high-speed on-chip oscillator is stopped and the PLL is operating

Note 7. The MAX. value includes the leakage current in STOP mode.

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency

Remark 3. fMAIN: Main system clock frequency

Remark 4. The temperature condition for the TYP. value is TA = 25°C, except the operation in STOP mode.

• Peripheral functions

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3	fMX = 4 MHz, RTCCL = 00H (fMX/122)			22		μA
Interval timer operating current	IIT Notes 1, 2, 4	fMX = 4 MHz, RTCCL = 00H (fMX/122)			22		μA
Watchdog timer operating current	IWDT Notes 1, 5, 6	fIL = 15 kHz			0.22		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 8				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 9				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	A/D converter operationNotes 10,	The mode is performed		0.50	1.10	mA
			During A/D conversion, AVDD = VDD = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to VDD

Note 2. When the high-speed on-chip oscillator is stopped

Note 3. Current flowing only to the real-time clock (RTC). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock is operating in operation mode or HALT mode.

Note 4. Current flowing only to the interval timer. The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the interval timer is operating in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, also add IFIL.

Note 5. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 6. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.

Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is operating.

Note 8. Current flowing during self-programming

Note 9. Current flowing during writing to the data flash

Note 10. The current flowing into the AVDD is included.

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fIL: Low-speed on-chip oscillator clock frequency

Remark 3. The temperature condition for the TYP. value is TA = 25°C

- AFE functions

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
24-bit ΔΣ A/D converter operating current	IDSAD	Normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS IOUT = 0 mA		0.94	1.46	mA
		Low power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS IOUT = 0 mA		0.60	0.91	mA
10-bit A/D converter operating current	IADC	During conversion at the highest speed Notes 1, 2 AVDD = 5.0 V		1.30	1.70	mA
Configurable amplifier operating current	IAMP	Normal mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier IL = 0 mA Per channel		0.13	0.24	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier IL = 0 mA Per channel		0.30	0.45	mA
12-bit D/A converter operating current	IDAC	When AVDD is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR and internal reference voltage (VREFDA)		0.61	0.97	mA

Note 1. Current flowing to AVDD

Note 2. Current flowing only to the circuits that operate shown in the Conditions column.

2.4 AC Characteristics

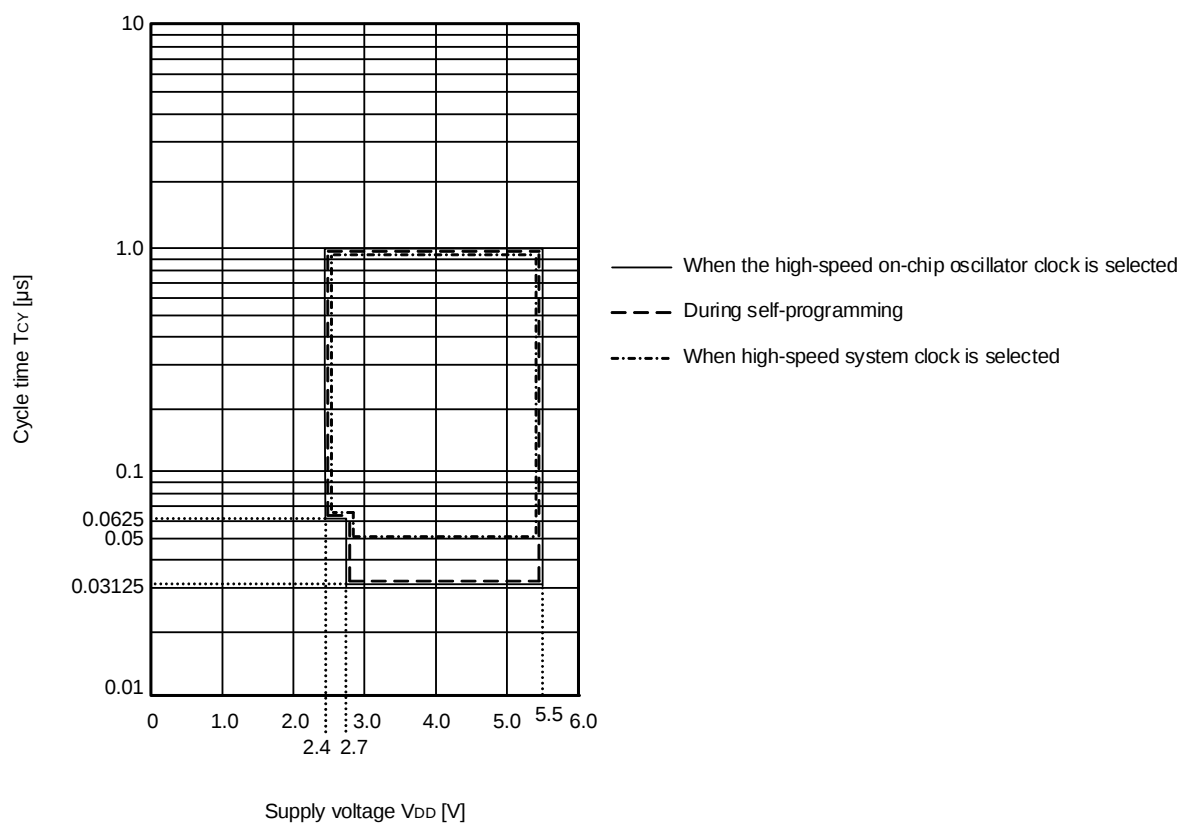
(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
			2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
		In the self-programming mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
			2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
External system clock frequency	fEX	2.7 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V		1.0		16.0	MHz
External system clock input high-level width, low-level width	tEXH, tEXL	2.7 V ≤ VDD ≤ 5.5 V		24			ns
		2.4 V ≤ VDD < 2.7 V		30			ns
TI00 to TI03, TI10, TI11 input high-level width, low-level width	tTIIH, tTIL			1/fMCK + 10			ns
Timer RJ input cycle	fc	TRJIO0	2.7 V ≤ VDD ≤ 5.5 V	100			ns
			2.4 V ≤ VDD < 2.7 V	300			ns
Timer RJ input high- level width, low-level width	tTJIH, tTJIL	TRJIO0	2.7 V ≤ VDD ≤ 5.5 V	40			ns
			2.4 V ≤ VDD < 2.7 V	120			ns
Timer RG input high- level width, low-level width	tTRGIH, tTRGIL	TRGIOA, TRGIOB		2.5/fCLK			ns
TO00 to TO03, TO10, TO11, TRJIO0, TRJO0, TRGIOA, TRGIOB output frequency	fTO		4.0 V ≤ VDD ≤ 5.5 V			16	MHz
			2.7 V ≤ VDD ≤ 4.0 V			8	MHz
			2.4 V ≤ VDD < 2.7 V			4	MHz
PCLBUZ0 output frequency	fPCL		4.0 V ≤ VDD ≤ 5.5 V			16	MHz
			2.7 V ≤ VDD ≤ 4.0 V			8	MHz
			2.4 V ≤ VDD < 2.7 V			4	MHz
Interrupt input high- level width, low-level width	tINTH, tINTL	INTP1 to INTP7		1			μs
RESET low-level width	tRSL			10			μs

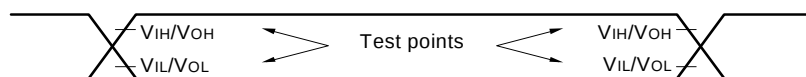
Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

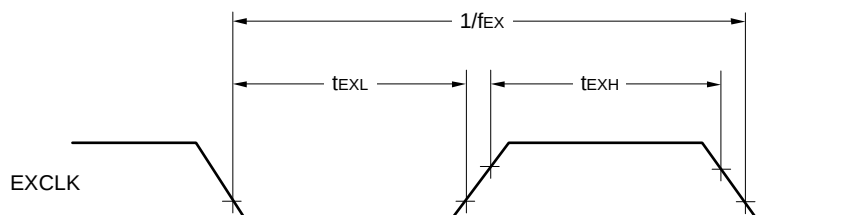
Minimum Instruction Execution Time During Main System Clock Operation

T_{CY} vs V_{DD}

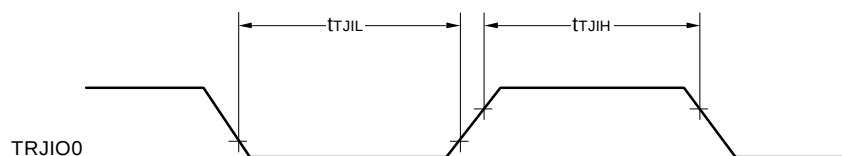
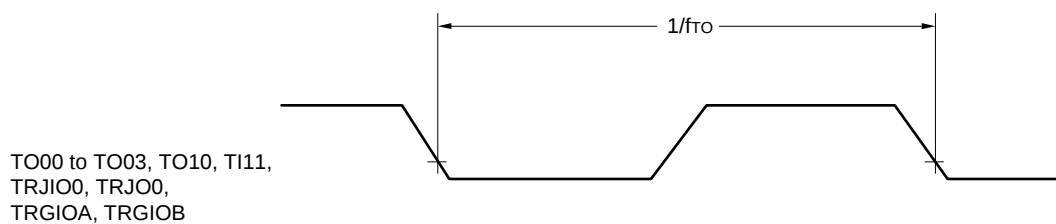
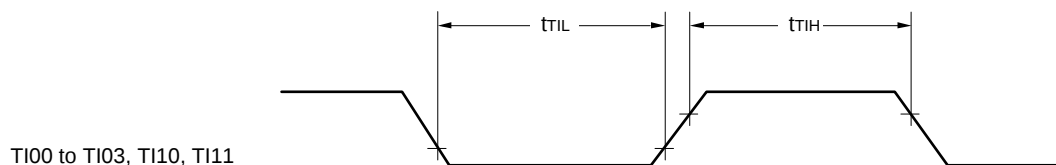
AC Timing Test Points

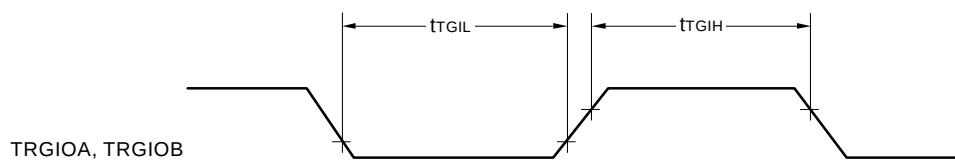


External System Clock Timing

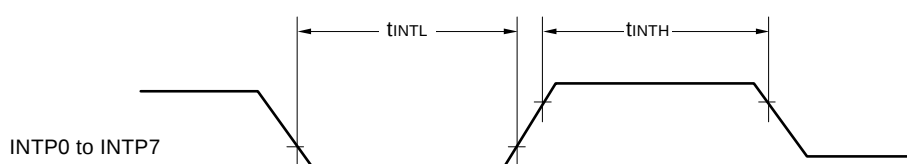
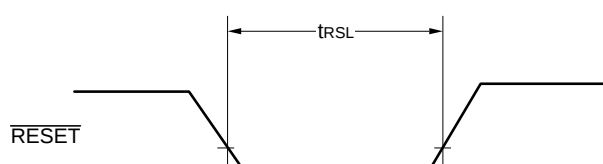


TI/TO Timing



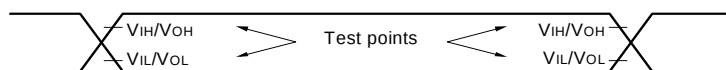


Interrupt Request Input Timing

 $\overline{\text{RESET}}$ Input Timing

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 2		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

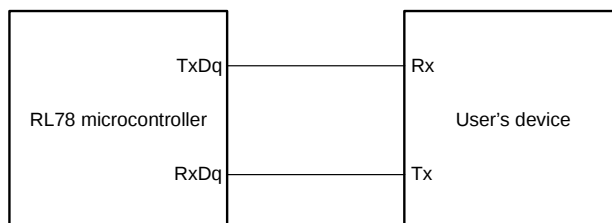
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

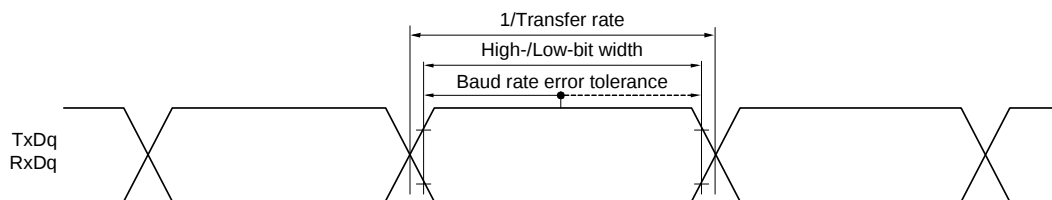
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 2.7 V ≤ V _{DD} ≤ 5.5 V	250		ns
			500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 24		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 36		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 76		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V	66		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	66		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{SI1}		38		ns
Delay time from SCKp↓ to SOp output ^{Note 2}	t _{KSO1}	C = 30 pF ^{Note 3}		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM number (g = 1)

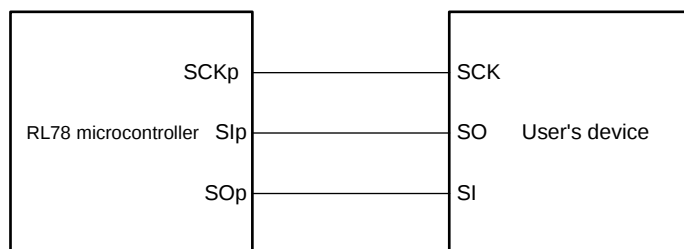
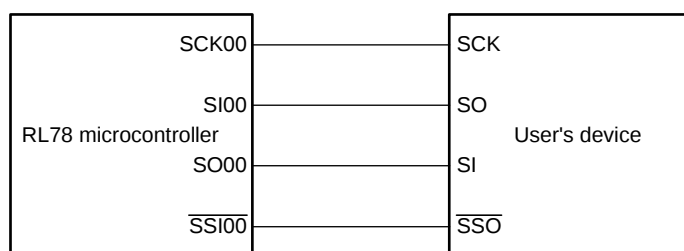
Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

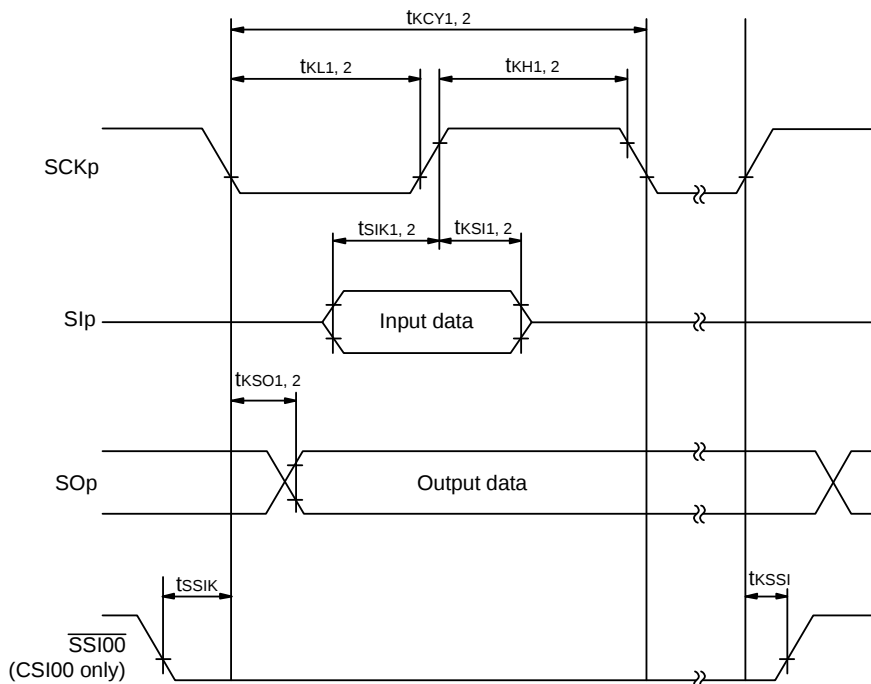
Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 20 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	16 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		12/f _{MCK} and 1000		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 14		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 16		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 36		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	2.7 V ≤ V _{DD} ≤ 5.5 V		1/f _{MCK} + 40		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SIK2}			1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} + 66	ns
			2.4 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} + 113	ns
SSI00 setup time	t _{SSIK}	DAPmn = 0	2.7 V ≤ V _{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 400		ns
SSI00 hold time	t _{KSSI}	DAPmn = 0	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ V _{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	400		ns

Note 1. The maximum transfer rate in the SNOOZE mode is 1 Mbps.**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 4.** C is the load capacitance of the SOp output lines.**Caution** Select the normal input buffer for the Slp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remark 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM number (g = 1)**Remark 2.** f_{MCK}: Serial array unit operation clock frequency

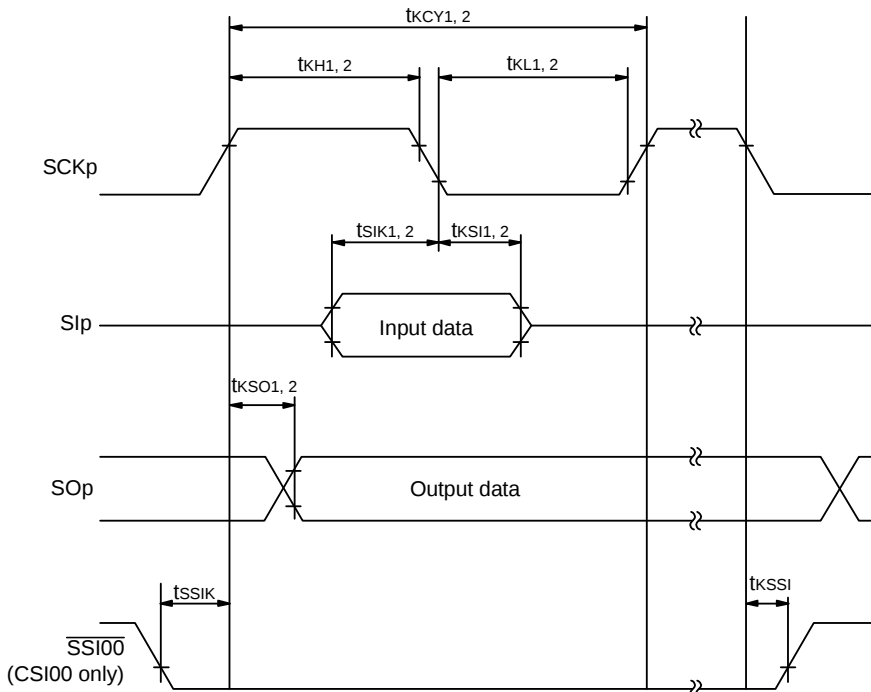
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))****Remark 1.** p: CSI number (p = 00, 01)**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)

Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

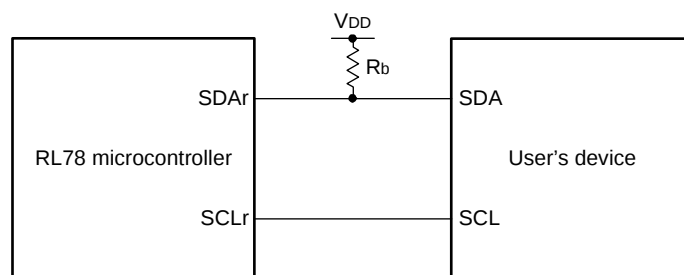
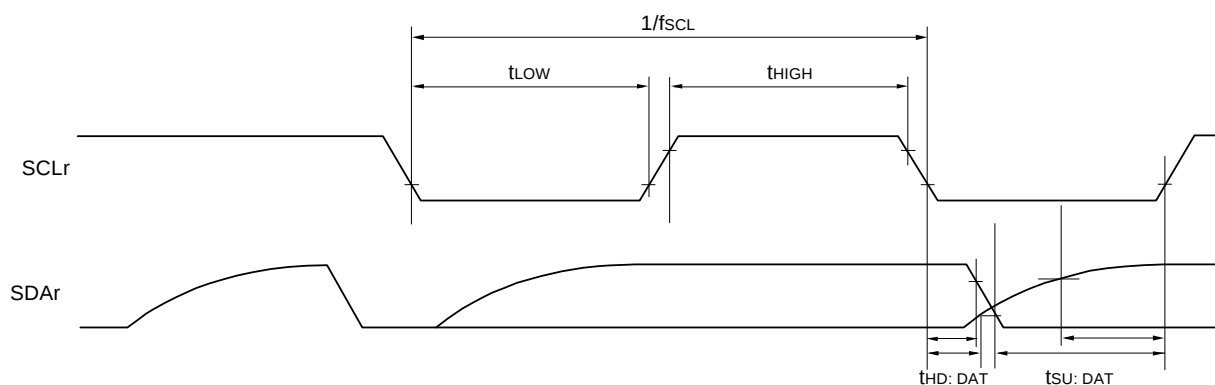
(4) During communication at same potential (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	4600		ns
Data setup time (reception)	t _{SU: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 220 Note 2		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 580 Note 2		ns
Data hold time (transmission)	t _{HD: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Remark 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01), g: PIM number (g = 1), h: POM number (h = 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),

n: Channel number (n = 0, 1), mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.6	Mbps
			2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.6	Mbps
			2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb [V]: Communication line voltage**Remark 2.** q: UART number (q = 0, 1), g: PIM or POM number (g = 1)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.6 Note 2	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ VDD ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ VDD < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

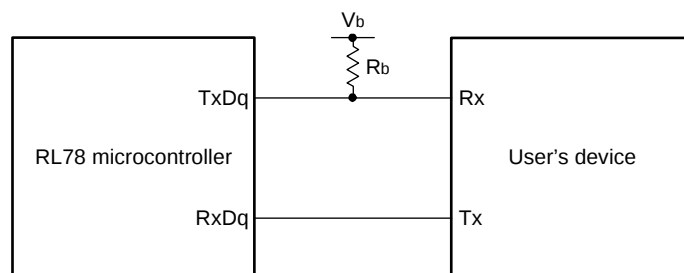
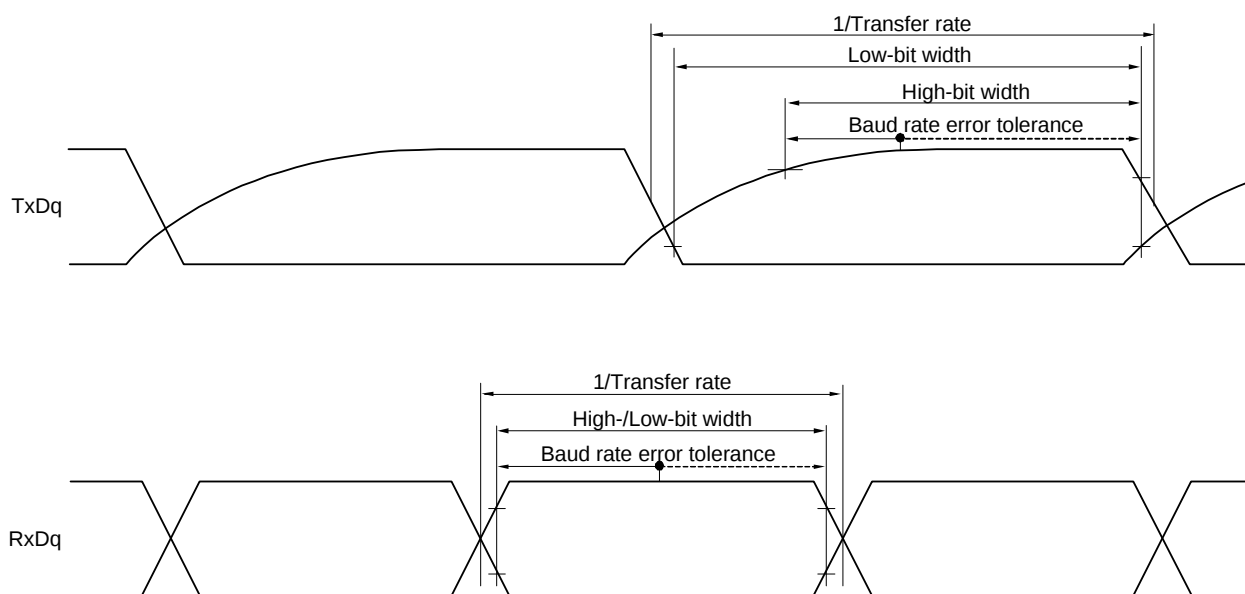
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

Remark 1. R_b [Ω]: Communication line (TxDq) pull-up resistance,
 C_b [F]: Communication line (TxDq) load capacitance, V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	600		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	1000		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	2300		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 150		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 340		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 916		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 24		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 36		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 100		ns

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	162		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	354		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) ^{Note}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output ^{Note}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		200	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		390	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

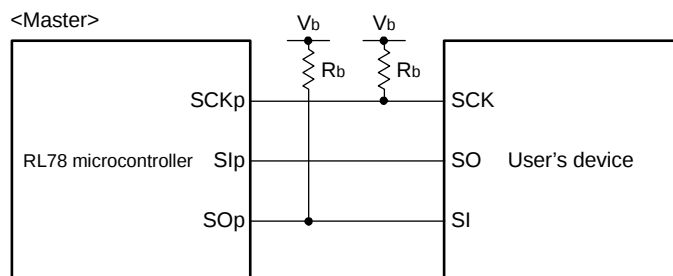
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	88		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	88		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) ^{Note}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		50	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		50	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

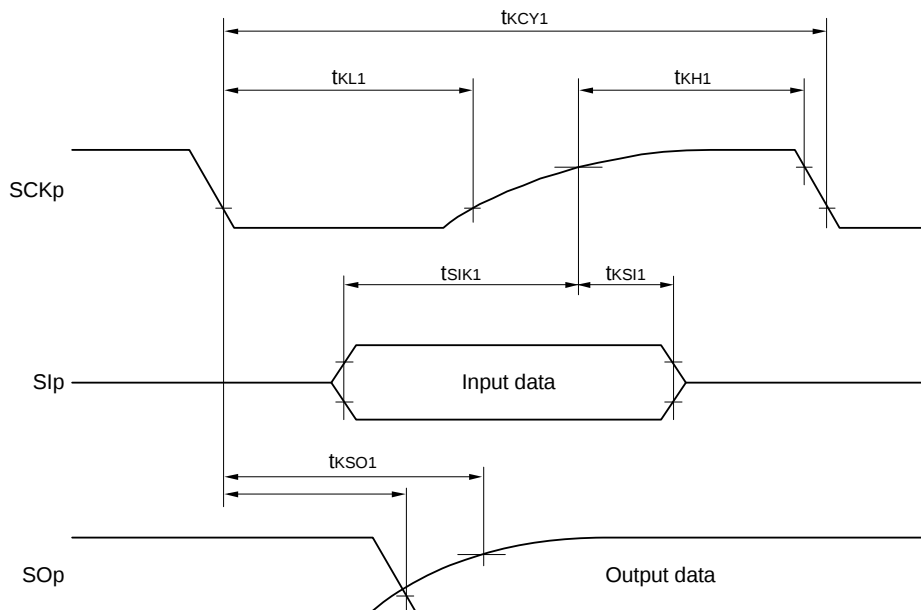
Remark 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

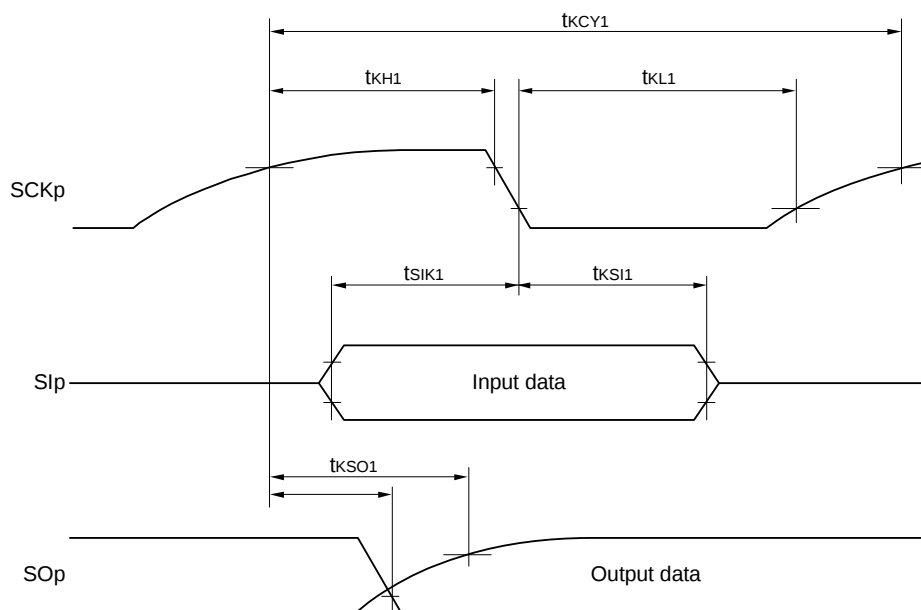
Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

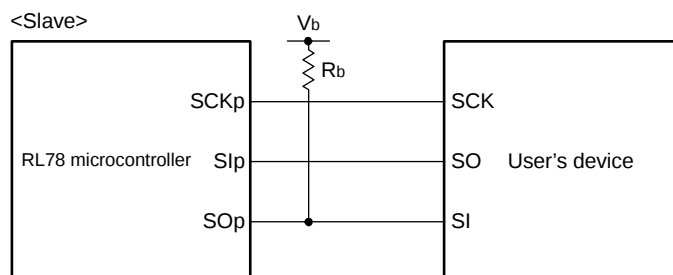
(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	28/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	40/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	24 MHz < f _{MCK}	96/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 - 24		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 - 36		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		t _{KCY2} /2 - 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 40		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 40		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}			1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOP output ^{Note 3}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 240	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns

(Notes, Cautions, and Remarks are listed on the next page.)

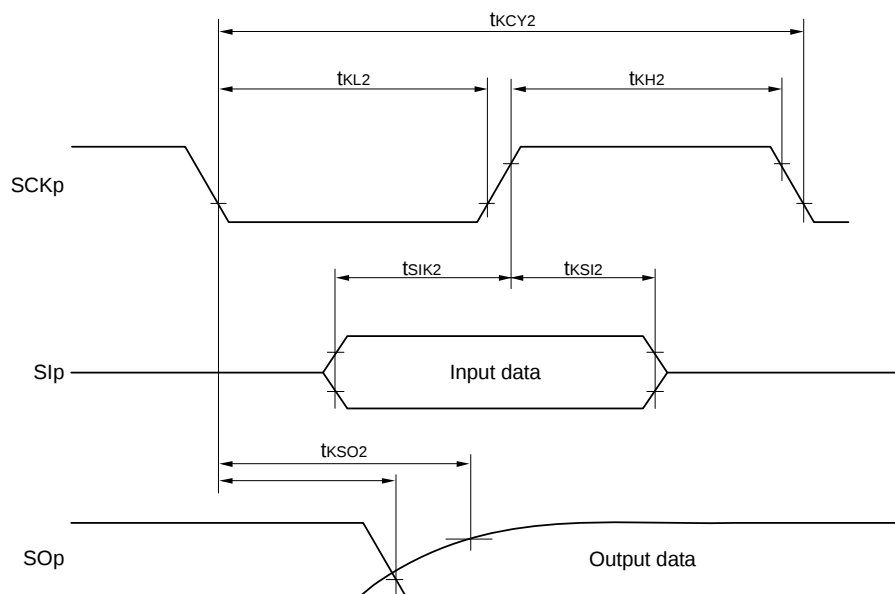
- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (VDD tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

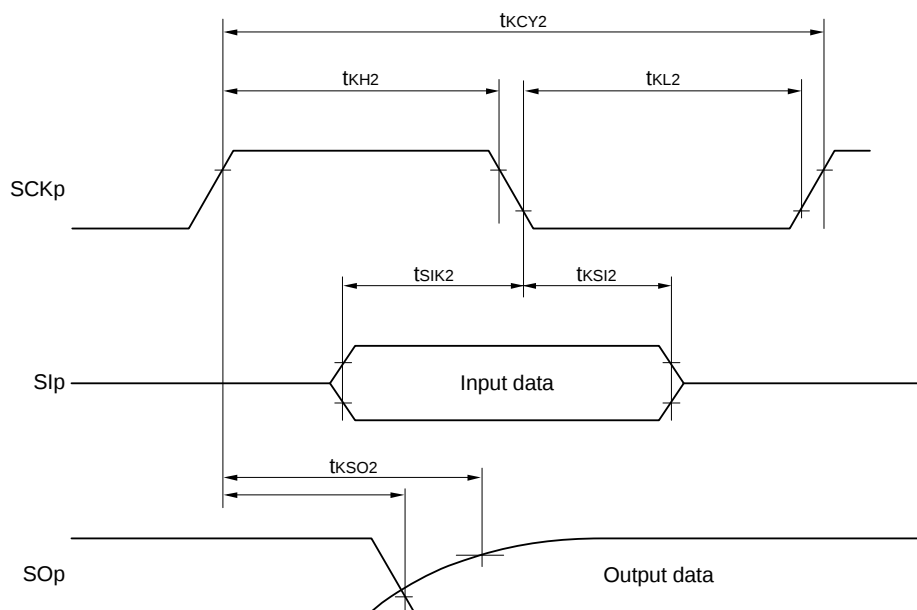


- Remark 1.** Rb [Ω]: Communication line (SOp) pull-up resistance, Cb [F]: Communication line (SOp) load capacitance, Vb [V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)
- Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))
- Remark 4.** Communication at different potential cannot be performed during clocked serial communication with the slave select function.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

Remark 2. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	4600		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	4600		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	620		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	500		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	2700		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	2400		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1830		ns

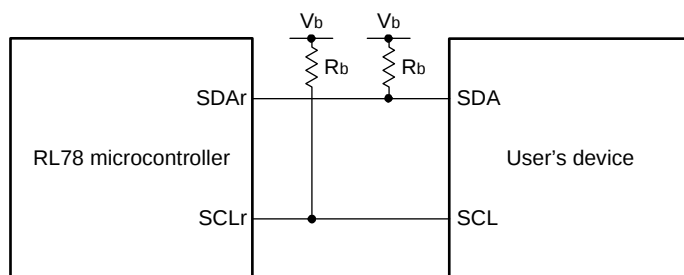
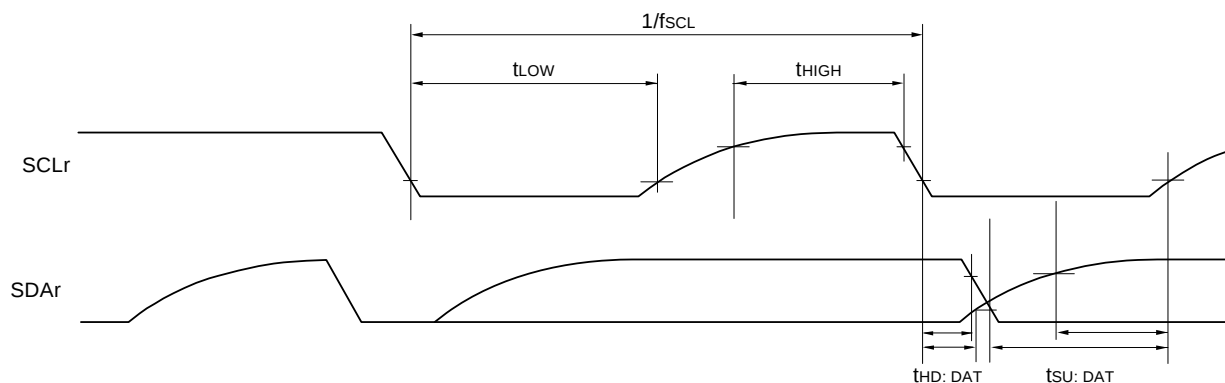
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 2		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 2		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 570 Note 2		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	0	1215	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Remark 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01), g: PIM, POM number (g = 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00, 01)

2.6 Analog Characteristics

2.6.1 Programmable gain instrumentation amplifier and 24-bit $\Delta\Sigma$ A/D converter

(1) Analog input in differential input mode

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Full-scale differential input voltage range	V _{ID}	V _{ID} = (PGAxP - PGAxN) (x = 0 to 3)		± 800 /G _{TOTAL}		mV
Input voltage range	V _I	Each of PGAxP and PGAxN pins (x = 0 to 3)	0.2		1.8	V
Common mode input voltage	V _{COM}	doFR = 0 mV	0.2+(V _{ID} x G _{SET1})/2		1.8-(V _{ID} x G _{SET1})/2	V
Input bias current	I _{IN}	V _I = 1.0 V			±50	nA
Input offset current	I _{INOFFR}	V _I = 1.0 V			±20	nA

(2) Analog input in single-ended input mode

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	V _I	Each of PGAxP and PGAxN pins (x = 0 to 3) G _{SET1} = 1, G _{SET2} = 1	0.2		1.8	V
Input bias current	I _{IN}	V _I = 1.0 V			±50	nA

(3) Programmable gain instrumentation amplifier and 24-bit $\Delta\Sigma$ A/D converter

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used, in differential input mode) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				24	bit
Sampling frequency	fs1	Normal mode		1		MHz
	fs2	Low power mode		0.125		MHz
Output data rate	fDATA1	Normal mode	0.48828		15.625	ksps
	fDATA2	Low power mode	61.03615		1953.125	sps
Gain setting range	G _{TOTAL}	G _{TOTAL} = G _{SET1} × G _{SET2}	1		64	V/V
1st gain setting range	G _{SET1}	In differential input mode only		1, 2, 3, 4, 8		V/V
2nd gain setting range	G _{SET2}	In differential input mode only		1, 2, 4, 8		V/V
Offset adjustment bit range	doFFB			5		bit
Offset adjustment range	doFR	Referred to input	-164/G _{SET1}		+164/G _{SET1}	mV
Offset adjustment steps	doFS	Referred to input		11/G _{SET1}		mV

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksp/s, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sp/s, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used, in differential input mode) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain error	EG	TA = 25°C GSET1 = 1, GSET2 = 1 Excluding SBIAS error		±0.2	±2.7	%
		TA = 25°C GSET1 = 8, GSET2 = 4 Excluding SBIAS error		±0.1		%
Gain drift ^{Note}	dEG	GSET1 = 1, GSET2 = 1 Excluding SBIAS drift		(5.6)	(22.0)	ppm/°C
		GSET1 = 8, GSET2 = 4 Excluding SBIAS drift		(9.1)		ppm/°C
Offset error	Eos	TA = 25°C GSET1 = 1, GSET2 = 1 Referred to input		±0.32	±2.90	mV
		TA = 25°C GSET1 = 8, GSET2 = 4 Referred to input		±0.03		mV
Offset drift ^{Note}	dEos	GSET1 = 1, GSET2 = 1 Referred to input		(±0.02)	(±6.00)	μV/°C
		GSET1 = 8, GSET2 = 4 Referred to input		(±0.02)		μV/°C
SND ratio	SNDR	GSET1 = 1, GSET2 = 1, fin = 50 Hz Normal mode, pin = -1 dBFS	(82)	(85)		dB
		GSET1 = 8, GSET2 = 4, fin = 50 Hz Normal mode, pin = -1 dBFS	(73)	(80)		dB
Noise	Vn	GSET1 = 1, GSET2 = 1, OSR = 2048		(13)		μVRms
		GSET1 = 8, GSET2 = 4, OSR = 2048		(0.6)		μVRms
Integral non-linearity error	INL	GSET1 = 1, GSET2 = 1, OSR = 2048		(±10)		ppmFS
Common mode rejection ratio	CMRR	VCOM = 1.0±0.8 V, fin = 50 Hz GSET1 = 1, GSET2 = 1 Differential input mode	(72)	(90)		dB
Power supply rejection ratio	PSRR	AVDD = 2.7 to 5.5 V GSET1 = 1, GSET2 = 1 Differential input mode		(85)		dB
ΔΣ A/D converter input clock frequency	fADC		3.8	4	4.2	MHz

Note Calculate the gain drift and offset drift by using the following expression (for 105°C products):
 For gain drift: (MAX(EG(T(-40) to T(105))) - MIN(EG(T(-40) to T(105)))) / (105°C - (-40°C))
 For offset drift: (MAX(Eos(T(-40) to T(105))) - MIN(Eos(T(-40) to T(105)))) / (105°C - (-40°C))
 MAX(EG(T(-40) to T(105))): The maximum value of gain error when the temperature range is -40°C to 105°C
 MIN(EG(T(-40) to T(105))): The minimum value of gain error when the temperature range is -40°C to 105°C
 MAX(Eos(T(-40) to T(105))): The maximum value of offset error when the temperature range is -40°C to 105°C
 MIN(Eos(T(-40) to T(105))): The minimum value of offset error when the temperature range is -40°C to 105°C

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2.6.2 Sensor power supply (SBIAS)

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, COUT = 0.22 μF, VOUT = 1.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	VOUT		0.5		2.2	V
Output voltage setting steps	VSTEP			0.1		V
Output voltage precision	VA	IOUT = 1 mA	(-3)		(+3)	%
Maximum output current	IOUT		5			mA
Short circuit current	ISHORT	VOUT = 0 V		40	65	mA
Load regulation	LR	1 mA ≤ IOUT ≤ 5 mA			(15)	mV
Power supply rejection ratio	PSRR	AVDD = 5.0 V + 0.1 Vpp ripple f = 100 Hz, IOUT = 2.5 mA	(45)	(50)		dB

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2.6.3 Temperature sensor

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature coefficient for sensor	TCSNS			(756)		μV/°C
Sensor output voltage	VTEMP	TA = 25°C		226.4		mV

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2.6.4 A/D converter characteristics

- (1) When positive reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(TA = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = AV_{DD}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V		1.2	±6.5	LSB
			2.7 V ≤ AV _{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution	4.0 V ≤ AV _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ AV _{DD} ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±3.5	LSB
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI9		AV _{SS}		AV _{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The number of pins depends on the product. For details, see a list of pin functions.

- (2) When positive reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(TA = -40 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = V_{BGR}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E _{ZS}	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±1.0	LSB
Internal reference voltage (+)	V _{BGR}	2.7 V ≤ AV _{DD} ≤ 5.5 V		V _{BGR} Note 3			V
Analog input voltage	V _{AIN}	ANI0 to ANI9		0		V _{BGR}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See the Internal reference voltage characteristics.

2.6.5 12-bit D/A converter

(1) When positive reference voltage (+) = AVDD (DACVRF = 0)

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, positive reference voltage (+) = AVDD)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		AVDD-0.47	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution			±20	mV
Settling time	DAtset	12-bit resolution, CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.

(2) When positive reference voltage (+) = internal reference voltage (DACVRF = 1)

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, positive reference voltage (+) = VREFDA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(8)	bit
Internal reference voltage	VREFDA	8-bit resolution	1.34	1.45	1.54	V
Output voltage range	DAOUT	8-bit resolution	0.35		VREFDA	V
Integral non-linearity error	DAILE	8-bit resolution			±1.0	LSB
Differential non-linearity error	DADLE	8-bit resolution			±1.0	LSB
Offset error	DAErr	8-bit resolution			±30	mV
Gain error	DAEG	8-bit resolution			±20	mV
Settling time	DAtset	8-bit resolution, CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.

Remark 3. Offset error and gain error do not include error in the internal reference voltage.

2.6.6 Configurable amplifier

(TA = -40 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, VCOM = 1/2 AVDD, internally connected voltage follower)

AMP0 configuration SW setting: Positive (+) pin = ANX1, negative (-) pin = ANX0

AMP1 configuration SW setting: Positive (+) pin = ANX3, negative (-) pin = ANX2

AMP2 configuration SW setting: Positive (+) pin = ANX5, negative (-) pin = ANX4

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	VIN		AVSS		AVDD	V
Output voltage	VOL	IL = -1 mA, AVDD = 2.7 to 5.5 V		AVSS +0.02	AVSS +0.07	V
	VOH	IL = 1 mA, AVDD = 2.7 to 5.5 V	AVDD -0.15	AVDD -0.02		V
Maximum output current	IOUT	4.5 V ≤ AVDD ≤ 5.5 V	±10			mA
		2.7 V ≤ AVDD ≤ 5.5 V	±5			mA
Input-referred offset voltage	VOFF	TA = 25°C without trimming IL = 0 mA, VCOM = 1.0 V		±1	±4	mV
		TA = 25°C with trimming IL = 0 mA, VCOM = 1.0 V			±0.35	mV
Temperature coefficient for input-referred offset voltage	VOTC	IL = 0 mA		(±2)	(±8)	μV/°C
Slew rate	SR1	Normal mode CL = 50 pF, RL = 10 kΩ		(0.1)		V/μs
	SR2	High-speed mode CL = 50 pF, RL = 10 kΩ		(0.8)		V/μs
Gain bandwidth	GBW1	Normal mode CL = 50 pF, RL = 10 kΩ		(350)		kHz
	GBW2	High-speed mode CL = 50 pF, RL = 10 kΩ		(1.8)		MHz
Phase margin	θM1	Normal mode CL = 50 pF, RL = 10 kΩ		(70)		deg
	θM2	High-speed mode CL = 50 pF, RL = 10 kΩ		(60)		deg
Settling time	tset1	Normal mode CL = 50 pF, RL = 10 kΩ		(20)		μs
	tset2	High-speed mode CL = 50 pF, RL = 10 kΩ		(10)		μs
Peak-to-peak voltage noise	Enb	0.1 to 10 Hz Normal mode CL = 50 pF, RL = 10 kΩ		(2.0)		μVrms
Input-referred noise	En	f = 1 kHz, Normal mode CL = 50 pF, RL = 10 kΩ		(70)		nV/√Hz
Common mode rejection ratio	CMRR	f = 1 kHz, CL = 50 pF, RL = 10 kΩ		(70)		dB
Power supply rejection ratio	PSRR	2.7 V ≤ AVDD ≤ 5.5 V f = 1 kHz, CL = 50 pF, RL = 10 kΩ		(62)		dB

(Remarks are listed on the next page.)

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The TYP. conditions are the conditions when TA = 25°C and AVDD = 5.0 V.

Remark 3. Unless otherwise specified, offset trimming has proceeded.

Remark 4. Unless otherwise specified, values are for operation in normal mode.

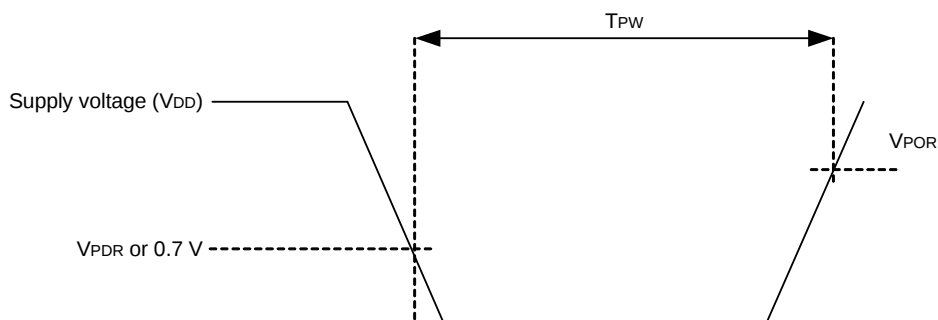
2.6.7 POR characteristics

(TA = -40 to +105°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.48	1.56	1.62	V
	VPDR	Voltage threshold on VDD falling ^{Note 1}	1.47	1.55	1.61	V
Minimum pulse width ^{Note 2}	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.8 LVD characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(TA = -40 to +105°C, VPDR ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVD0	Rising edge	4.62	4.74	4.84	V
		Falling edge	4.52	4.64	4.74	V
	VLVD1	Rising edge	4.50	4.62	4.72	V
		Falling edge	4.40	4.52	4.62	V
	VLVD2	Rising edge	4.30	4.42	4.51	V
		Falling edge	4.21	4.32	4.41	V
	VLVD3	Rising edge	3.13	3.22	3.29	V
		Falling edge	3.07	3.15	3.22	V
	VLVD4	Rising edge	2.95	3.02	3.09	V
		Falling edge	2.89	2.96	3.02	V
	VLVD5	Rising edge	2.74	2.81	2.87	V
		Falling edge	2.68	2.75	2.81	V
	VLVD6	Rising edge	2.55	2.61	2.67	V
		Falling edge	2.49	2.55	2.61	V
Minimum pulse width	tLW		300			μs
Detection delay time					300	μs

(2) LVD detection voltage in interrupt & reset mode

(TA = -40 to +105°C, VPDR ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVD6	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage		2.49	2.55	2.61	V
	VLVD4	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.09	V
			Falling interrupt voltage	2.89	2.96	3.02	V
	VLVD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		2.68	2.75	2.81	V
	VLVD2	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.51	V
			Falling interrupt voltage	4.21	4.32	4.41	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.68	2.75	2.81	V
	VLVD1	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.72	V
			Falling interrupt voltage	4.40	4.52	4.62	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.68	2.75	2.81	V
	VLVD3	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	VLVD0	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.84	V
			Falling interrupt voltage	4.52	4.64	4.74	V

2.6.9 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				50	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

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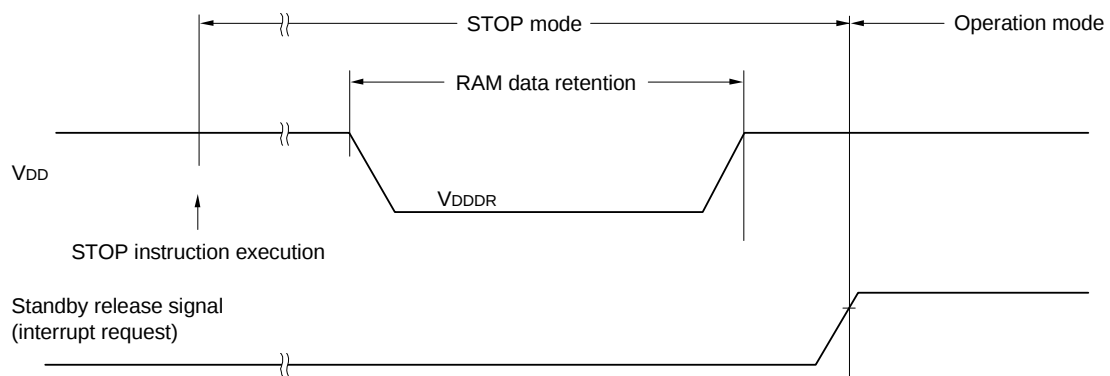
2.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.47 Notes 1, 2		5.5	V

Note 1. The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Note 2. Enter STOP mode before the supply voltage falls below the recommended operating voltage.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years T _A = 85°CNote 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T _A = 25°CNote 4		1,000,000		
		Retained for 5 years T _A = 85°CNote 4	100,000			
		Retained for 20 years T _A = 85°CNote 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

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2.9 Dedicated Flash Memory Programmer Communication (UART)

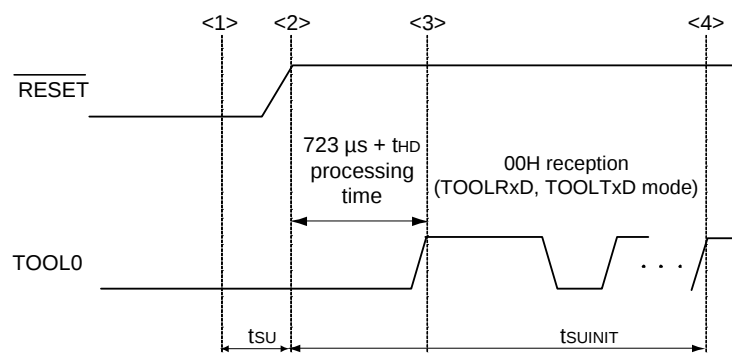
(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing for Switching Flash Memory Programming Modes

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (M: T_A = -40 to +125°C)

This chapter describes the electrical specifications for the products “M: Industrial applications (T_A = -40 to +125°C)”.

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Alternate functions other than AFE in the RL78/I1E User's Manual.

Caution 3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85 to +125°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark The electrical characteristics of the products M: Industrial applications (T_A = -40 to +125°C) are different from those of the products “G: Industrial applications”. For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	AV _{DD}	AV _{DD} = V _{DD}	-0.5 to +6.5	V
	AV _{SS}	AV _{SS} = V _{SS}	-0.5 to +0.3	V
REGC pin input voltage	V _I REGC	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 Note 1	V
REGA pin input voltage	V _I REGA	REGA	-0.3 to +2.8 and -0.3 to AV _{DD} + 0.3 Note 2	V
Input voltage	V _{I1}	P10 to P15, P40, P121, P122, P137, EXCLK, RESET	-0.3 to V _{DD} + 0.3 Note 3	V
Alternate-function pin input voltage	V _{I2}	P16, P17, P41, P42 (36-pin products only)	Digital input voltage	-0.3 to V _{DD} + 0.3 Note 3
			Analog input voltage	-0.3 to AV _{DD} + 0.3 Note 3
Analog input voltage	V _{IA}	PGA0P to PGA3P, PGA0N to PGA3N, ANI0 to ANI9, ANX0 to ANX5	-0.3 to AV _{DD} + 0.3 Note 3	V
Output voltage	V _{O1}	P10 to P15, P40	-0.3 to V _{DD} + 0.3 Note 3	V
Alternate-function pin output voltage	V _{O2}	P16, P17, P41, P42 (36-pin products only)	Digital output voltage	-0.3 to V _{DD} + 0.3 Note 3
			Analog output voltage	-0.3 to AV _{DD} + 0.3 Note 3
Analog output voltage	V _{OA}	SBIAS, AMP0O to AMP2O, ANX0 to ANX5	-0.3 to AV _{DD} + 0.3 Note 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the REGA pin to AV_{SS} via a capacitor (0.22 μF). This value regulates the absolute maximum rating of the REGA pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. V_{SS} is used as the reference voltage.

Absolute Maximum Ratings**(2/2)**

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P10 to P17, P40 to P42	-40	mA
		Total of all pins	P10 to P17, P41, P42 ^{Note}	-100	mA
Analog output current, high	IOHA	Per pin	AMP00 to AMP20	-12	mA
			ANX0 to ANX5	-0.12	mA
		Total of all pins	AMP00 to AMP20, ANX0 to ANX5	-18	mA
Output current, low	IOL1	Per pin	P10 to P17, P40 to P42	40	mA
		Total of all pins	P10 to P17, P41, P42 ^{Note}	100	mA
Analog output current, low	IOLA	Per pin	AMP00 to AMP20	12	mA
			ANX0 to ANX5	0.12	mA
		Total of all pins	AMP00 to AMP20, ANX0 to ANX5	18	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +125	°C
		In flash memory programming mode			
Storage temperature	Tstg			-65 to +150	°C

Note This indicates the total current value when P16, P17, P41, and P42 are used as digital input pins.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. V_{ss} is used as the reference voltage.

3.2 Oscillator Characteristics

3.2.1 X1 characteristics

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/I1E User's Manual..

3.2.2 On-chip oscillator characteristics

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f _{IH}	2.7 V ≤ VDD ≤ 5.5 V	1		24	MHz
		2.4 V ≤ VDD < 2.7 V	1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-40 to +105°C	-2.0		+2.0	%
		+105 to +125°C	-3.0		+3.0	%
Low-speed on-chip oscillator clock frequency	f _{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

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3.2.3 PLL characteristics

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
PLL output frequency ^{Notes 1, 2, 3}	f _{PLL}	f _{MX} = 8 MHz	DSFRDIV = 0	DSCM = 0		48		MHz
			DSFRDIV = 1	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
		f _{MX} = 4 MHz	DSFRDIV = 0	DSCM = 0		24		MHz
				DSCM = 1		32		MHz
Lockup wait time		Time from when PLL output is enabled to when the phase is locked			40			μs
Interval wait time		Time from when the PLL stops operating to when the setting to start PLL operation is specified			4			μs
Setup wait time		Time required from when the PLL input clock stabilizes and the PLL setting is determined to when the PLL is activated			1			μs

Note 1. When using a PLL, input a clock of 4 MHz or 8 MHz to the PLL.

Note 2. Be sure to specify one of these settings when using a PLL.

Note 3. When using the PLL output as the CPU clock, f_{1H} is divided by 2, 4, or 8 according to the setting of the RDIV1 and RDIV0 bits.

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(1/3)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P10 to P17 and P40 to P42 ^{Note 2}	4.0 V ≤ VDD ≤ 5.5 V		-3.0 ^{Note 3}	mA
			2.4 V ≤ VDD < 4.0 V		-1.0 ^{Note 3}	mA
		Total of P10 to P17, P41, and P42 ^{Note 3} (When duty ≤ 70% ^{Note 4})	4.0 V ≤ VDD ≤ 5.5 V		-30.0	mA
			2.7 V ≤ VDD < 4.0 V		-19.0	mA
			2.4 V ≤ VDD < 2.7 V		-10.0	mA
Output current, low ^{Note 1}	IOL1	Per pin for P10 to P17 and P40 to P42 ^{Note 2}	4.0 V ≤ VDD ≤ 5.5 V		8.5 ^{Note 3}	mA
			2.7 V ≤ VDD < 4.0 V		1.5 ^{Note 3}	mA
			2.4 V ≤ VDD < 2.7 V		0.6 ^{Note 3}	mA
		Total of P10 to P17, P41, and P42 ^{Note 2} (When duty ≤ 70% ^{Note 4})	4.0 V ≤ VDD ≤ 5.5 V		40.0	mA
			2.7 V ≤ VDD < 4.0 V		35.0	mA
			2.4 V ≤ VDD < 2.7 V		20.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pin to an output pin.

Note 2. This indicates the total current value when P16, P17, P41, and P42 are used as digital I/O ports. When using these pins as analog function (AFE) pins, refer to **3.1 Absolute Maximum Ratings**.

Note 3. Do not exceed the total current value.

Note 4. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

Example: n = 80% when IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(2/3)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P10 to P17 and P40 to P42	Normal input buffer	0.8 VDD		VDD	V
	VIH2	P11, P12, P14, P15	TTL input buffer, 4.0 V ≤ VDD ≤ 5.5 V	2.2		VDD	V
			TTL input buffer, 3.3 V ≤ VDD < 4.0 V	2.0		VDD	V
			TTL input buffer, 2.4 V ≤ VDD < 3.3 V	1.28		VDD	V
	VIH3	P121, P122, P137, EXCLK, RESET		0.8 VDD		VDD	V
Input voltage, low	VIL1	P10 to P17 and P40 to P42	Normal input buffer	0		0.2 VDD	V
	VIL2	P11, P12, P14, P15	TTL input buffer, 4.0 V ≤ VDD ≤ 5.5 V	0		0.8	V
			TTL input buffer, 3.3 V ≤ VDD < 4.0 V	0		0.5	V
			TTL input buffer, 2.4 V ≤ VDD < 3.3 V	0		0.32	V
	VIL3	P121, P122, P137, EXCLK, RESET		0		0.2 VDD	V
Output voltage, high	VOH1	P10 to P17 and P40 to P42	4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA	VDD - 0.7			V
			2.4 V ≤ VDD ≤ 5.5 V, IOH1 = -1.0 mA	VDD - 0.5			V
Output voltage, low	VOL1	P10 to P17 and P40 to P42	4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA			0.5	V
			2.4 V ≤ VDD ≤ 5.5 V, IOL1 = 0.6 mA			0.4	V

Caution The maximum VIH value on P10 to P15 is VDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(3/3)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P10 to P17, and P40 to P42	V _I = V _{DD}			1	μA
	ILI _{H2}	P137, $\overline{\text{RESET}}$	V _I = V _{DD}			1	μA
	ILI _{H3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{DD}	In input port mode or when using external clock input		1	μA
				When a resonator is connected		10	μA
Input leakage current, low	ILI _{L1}	P10 to P17, and P40 to P42	V _I = V _{SS}			-1	μA
	ILI _{L2}	P137, $\overline{\text{RESET}}$	V _I = V _{SS}			-1	μA
	ILI _{L3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{SS}	In input port mode or when using external clock input		-1	μA
				When a resonator is connected		-10	μA
On-chip pull-up resistance	R _U	P10 to P15, P40	V _I = V _{SS} , in input port mode	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current current Note 1	IDD1	Operating mode Note 2	fHOCO = 24 MHz, fMAIN = 24 MHz Note 3	Basic operation	VDD = 5.0 V		1.7		mA
					VDD = 3.0 V		1.7		
			fHOCO = 24 MHz, fMAIN = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	7.6	mA
					VDD = 3.0 V		3.8	7.6	
			fHOCO = 16 MHz, fMAIN = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	5.6	
					VDD = 3.0 V		2.8	5.6	
			fMX = 20 MHz, fMAIN = 20 MHz Note 4, VDD = 5.0 V	Normal operation	Square wave input		3.3	6.5	mA
					Resonator connection		3.5	6.6	
			fMX = 20 MHz, fMAIN = 20 MHz Note 4, VDD = 3.0 V	Normal operation	Square wave input		3.3	6.5	
					Resonator connection		3.5	6.6	
			fMX = 10 MHz, fMAIN = 10 MHz Note 4, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.9	
					Resonator connection		2.1	4.0	
			fMX = 10 MHz, fMAIN = 10 MHz Note 4, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.9	
					Resonator connection		2.1	4.0	

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RTC, interval timer, watchdog timer, LVD circuit, AFE, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. The relationship between the operation voltage range and the CPU operating frequency is as below.

2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 24 MHz

2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz

Note 3. When the high-speed system clock is stopped

Note 4. When the high-speed on-chip oscillator and the PLL are stopped

Note 5. When the high-speed on-chip oscillator is stopped and the PLL is operating

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency

Remark 3. fMAIN: Main system clock frequency

Remark 4. The temperature condition for the TYP. value is TA = 25°C

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode Note 3	fHOCO = 24 MHz, fMAIN = 24 MHz Note 4	VDD = 5.0 V		0.44	3.42	mA		
				VDD = 3.0 V		0.44	3.42			
			fHOCO = 16 MHz, fMAIN = 16 MHz Note 4	VDD = 5.0 V		0.40	2.50		mA	
				VDD = 3.0 V		0.40	2.50			
			fMX = 20 MHz, fMAIN = 20 MHz Note 5, VDD = 5.0 V	Square wave input		0.28	2.94			
				Resonator connection		0.49	3.08			
			fMX = 20 MHz, fMAIN = 20 MHz Note 5, VDD = 3.0 V	Square wave input		0.28	2.94			
				Resonator connection		0.49	3.08			
			fMX = 10 MHz, fMAIN = 10 MHz Note 5, VDD = 5.0 V	Square wave input		0.19	1.54			
				Resonator connection		0.30	1.63			
			fMX = 10 MHz, fMAIN = 10 MHz Note 5, VDD = 3.0 V	Square wave input		0.19	1.54			
				Resonator connection		0.30	1.63			
			fMX = 8 MHz, fMAIN = 24 MHz Note 6, VDD = 5.0 V	Square wave input		0.76	3.92	mA		
				Resonator connection		0.86	4.04			
			fMX = 8 MHz, fMAIN = 24 MHz Note 6, VDD = 3.0 V	Square wave input		0.76	3.92	mA		
				Resonator connection		0.86	4.04			
			IDD3 Note 7	STOP mode	TA = -40°C		0.38	1.14		μA
					TA = +25°C		0.50	1.14		
	TA = +50°C				0.66	4.52				
	TA = +70°C				1.04	7.98				
	TA = +85°C				2.92	16.0				
	TA = +105°C				11.0	100.0				
	TA = +125°C				22.0	200.0				

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the RTC, interval timer, watchdog timer, LVD circuit, AFE, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during writing to the data flash.

Note 2. During HALT instruction execution from flash memory

Note 3. The relationship between the operation voltage range and the CPU operating frequency is as below.

2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 24 MHz

2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz

Note 4. When the high-speed system clock is stopped

Note 5. When the high-speed on-chip oscillator and the PLL are stopped

Note 6. When high-speed on-chip oscillator is stopped and the PLL is operating

Note 7. The MAX. value includes the leakage current in STOP mode.

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency

Remark 3. fMAIN: Main system clock frequency

Remark 4. The temperature condition for the TYP. value is TA = 25°C, except the operation in STOP mode.

• Peripheral functions

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3	fMX = 4 MHz, RTCCL = 00H (fMX/122)			22		μA
Interval timer operating current	IIT Notes 1, 2, 4	fMX = 4 MHz, RTCCL = 00H (fMX/122)			22		μA
Watchdog timer operating current	IWDT Notes 1, 5, 6	fIL = 15 kHz			0.22		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 8				2.00	12.20	mA
BGO operating current	IBGO Notes 1, 9				2.00	12.20	mA
SNOOZE operating current	ISNOZ Note 1	A/D converter operation Notes 10,	The mode is performed		0.50	1.10	mA
			During A/D conversion, AVDD = VDD = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

Note 1. Current flowing to VDD

Note 2. When the high-speed on-chip oscillator is stopped

Note 3. Current flowing only to the real-time clock (RTC). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock is operating in operation mode or HALT mode.

Note 4. Current flowing only to the interval timer. The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the interval timer is operating in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, also add IFIL.

Note 5. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 6. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.

Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is operating.

Note 8. Current flowing during self-programming

Note 9. Current flowing during writing to the data flash

Note 10. The current flowing into the AVDD is included.

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fIL: Low-speed on-chip oscillator clock frequency

Remark 3. The temperature condition for the TYP. value is TA = 25°C

• AFE functions

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
24-bit ΔΣ A/D converter operating current	IDSAD	Normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS IOUT = 0 mA		0.94	1.46	mA
		Low power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA, 24-bit ΔΣ A/D converter, and digital filter Differential input mode OSR = 256 SBIAS IOUT = 0 mA		0.60	0.91	mA
10-bit A/D converter operating current	IADC	During conversion at the highest speed Notes 1, 2 AVDD = 5.0 V		1.30	1.70	mA
Configurable amplifier operating current	IAMP	Normal mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier IL = 0 mA Per channel		0.13	0.24	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and configurable amplifier IL = 0 mA Per channel		0.30	0.45	mA
12-bit D/A converter operating current	IDAC	When AVDD and AVSS are selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR and internal reference voltage (VREFDA)		0.61	0.97	mA

Note 1. Current flowing to AVDD**Note 2.** Current flowing only to the circuits that operate shown in the Conditions column.

3.4 AC Characteristics

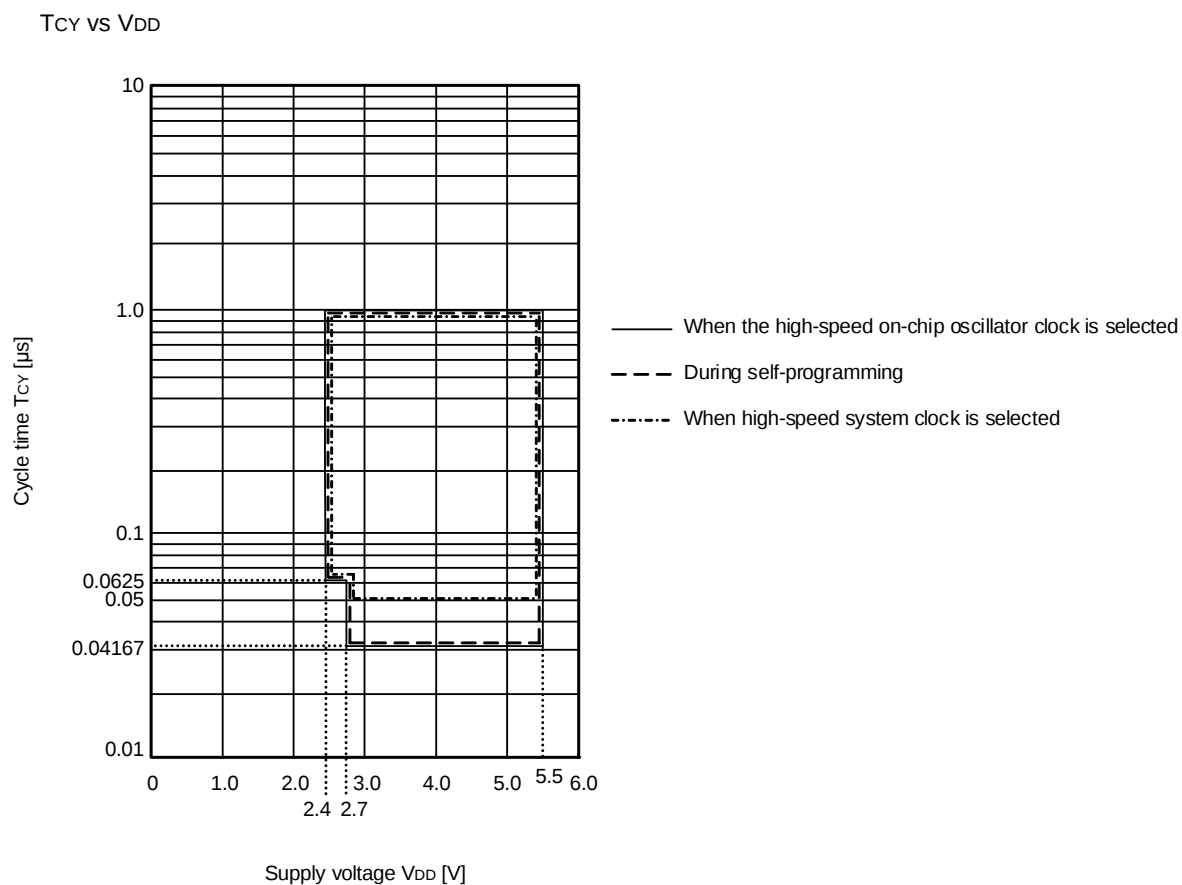
(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	2.7 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
			2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
		In the self-programming mode	2.7 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
			2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
External system clock frequency	fEX	2.7 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V		1.0		8.0	MHz
External system clock input high-level width, low-level width	tEXH, tEXL	2.7 V ≤ VDD ≤ 5.5 V		24			ns
		2.4 V ≤ VDD < 2.7 V		60			ns
TI00 to TI03, TI10, TI11 input high-level width, low-level width	tTIIH, tTIL			1/fMCK + 10			ns
Timer RJ input cycle	fc	TRJIO0	2.7 V ≤ VDD ≤ 5.5 V	100			ns
			2.4 V ≤ VDD < 2.7 V	300			ns
Timer RJ input high- level width, low-level width	tTJIH, tTJIL	TRJIO0	2.7 V ≤ VDD ≤ 5.5 V	40			ns
			2.4 V ≤ VDD < 2.7 V	120			ns
Timer RG input high- level width, low-level width	tTRGIH, tTRGIL	TRGIOA, TRGIOB		2.5/fCLK			ns
TO00 to TO03, TO10, TO11, TRJIO0, TRJO0, TRGIOA, TRGIOB output frequency	fTO		4.0 V ≤ VDD ≤ 5.5 V			12	MHz
			2.7 V ≤ VDD ≤ 4.0 V			6	MHz
			2.4 V ≤ VDD < 2.7 V			3	MHz
PCLBUZ0 output frequency	fPCL		4.0 V ≤ VDD ≤ 5.5 V			12	MHz
			2.7 V ≤ VDD ≤ 4.0 V			6	MHz
			2.4 V ≤ VDD < 2.7 V			3	MHz
Interrupt input high- level width, low-level width	tINTH, tINTL	INTP1 to INTP7		1			μs
RESET low-level width	tRSL			10			μs

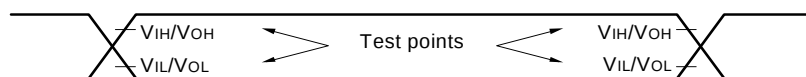
Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

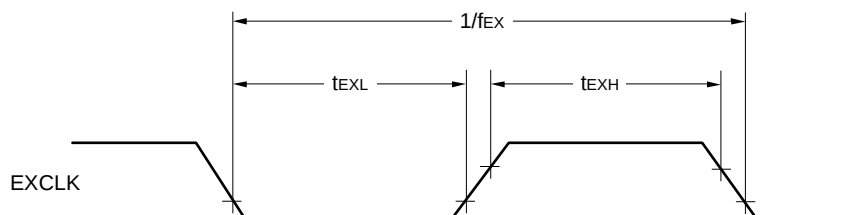
Minimum Instruction Execution Time During Main System Clock Operation



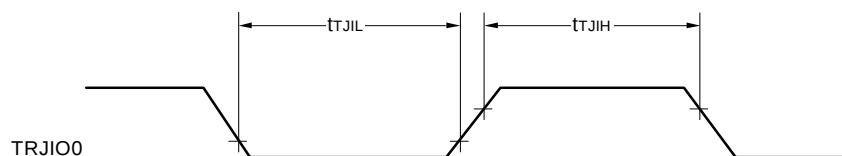
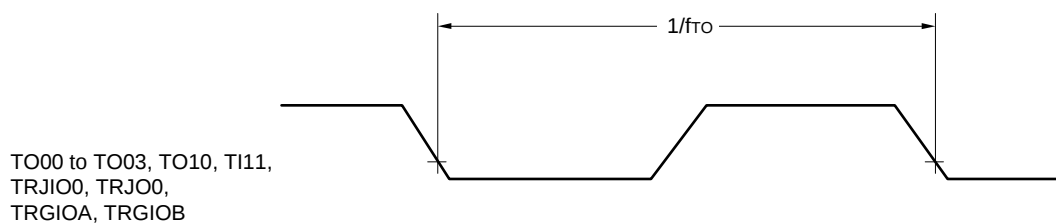
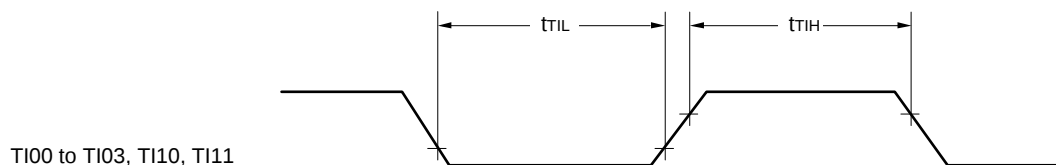
AC Timing Test Points

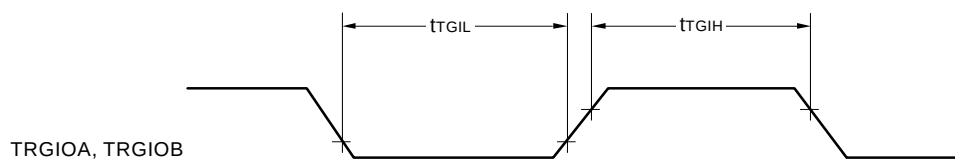


External System Clock Timing

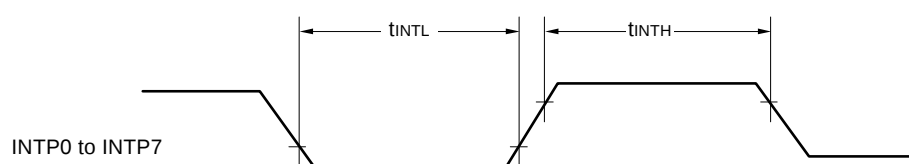
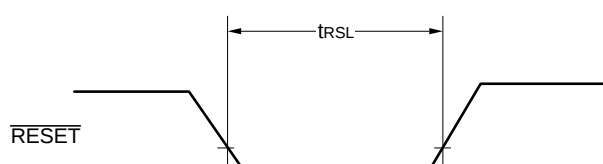


TI/TO Timing



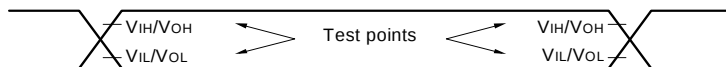


Interrupt Request Input Timing

 $\overline{\text{RESET}}$ Input Timing

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 2		2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

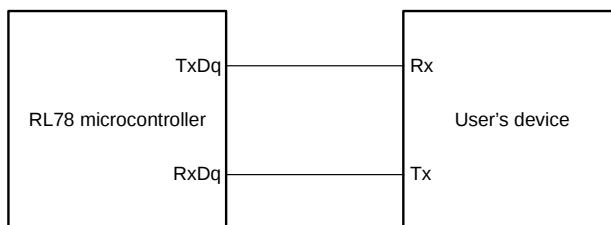
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

24 MHz (2.4 V ≤ VDD ≤ 5.5 V)

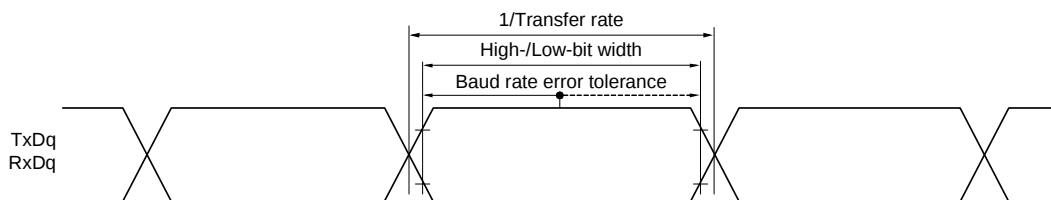
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0, 1), g: PIM or POM number (g = 1)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 2.7 V ≤ V _{DD} ≤ 5.5 V	333		ns
			666		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 24		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 36		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 76		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V	66		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	66		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{SI1}		38		ns
Delay time from SCKp↓ to SOp output ^{Note 2}	t _{KSO1}	C = 30 pF ^{Note 3}		66.6	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

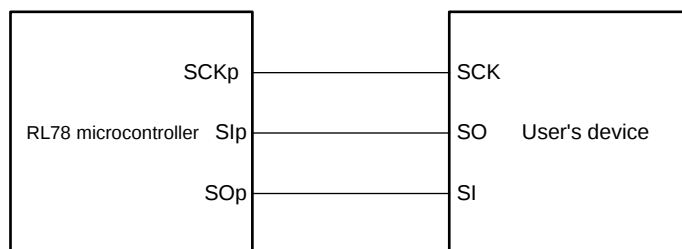
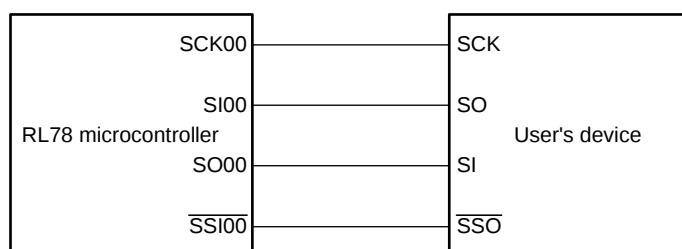
Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

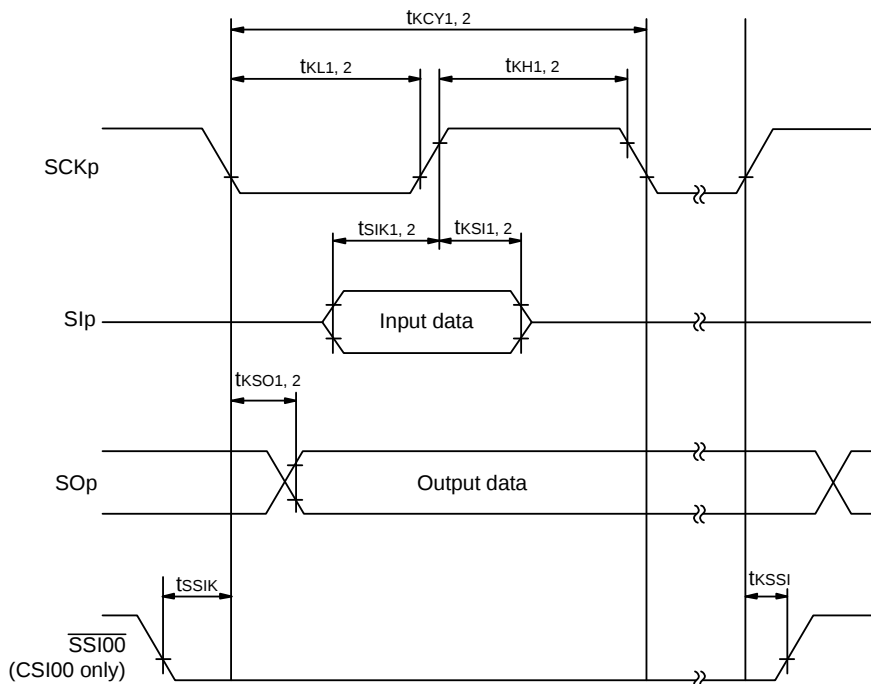
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 20 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	16 MHz < f _{MCK}	16/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		12/f _{MCK} and 1000		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 14		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 16		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		t _{KCY2} /2 - 36		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	2.7 V ≤ V _{DD} ≤ 5.5 V		1/f _{MCK} + 40		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SIK2}			1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} + 66	ns
			2.4 V ≤ V _{DD} ≤ 5.5 V		2/f _{MCK} + 113	ns
SSI00 setup time	t _{SSIK}	DAPmn = 0	2.7 V ≤ V _{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 400		ns
SSI00 hold time	t _{KSSI}	DAPmn = 0	2.7 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	1/f _{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ V _{DD} ≤ 5.5 V	240		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	400		ns

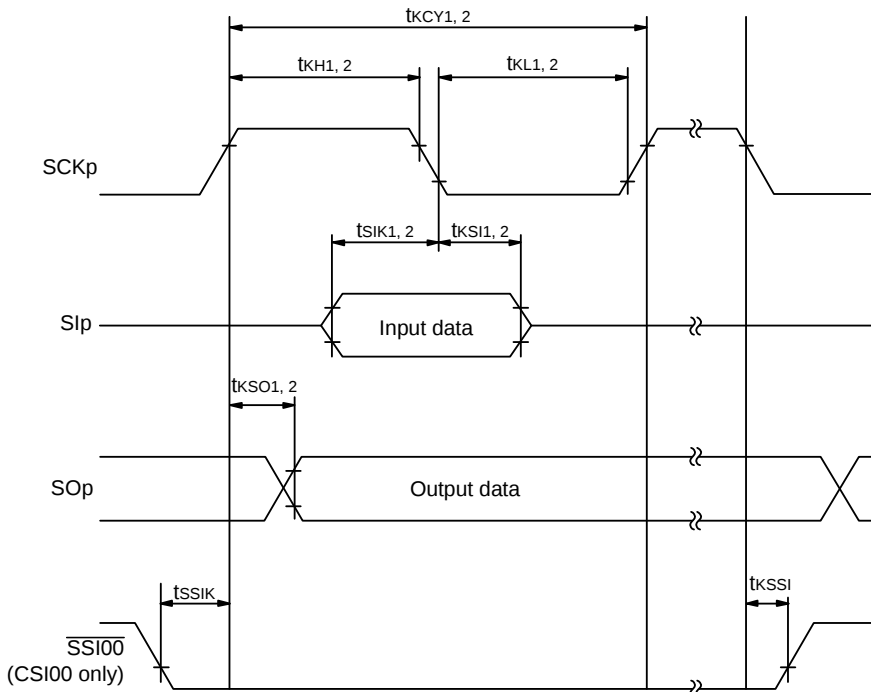
Note 1. The maximum transfer rate in the SNOOZE mode is 1 Mbps.**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 4.** C is the load capacitance of the SOp output lines.**Caution** Select the normal input buffer for the Slp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remark 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM number (g = 1)**Remark 2.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at same potential)**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))****Remark 1.** p: CSI number (p = 00, 01)**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)

Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

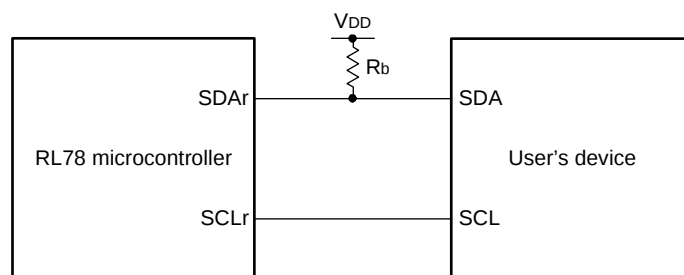
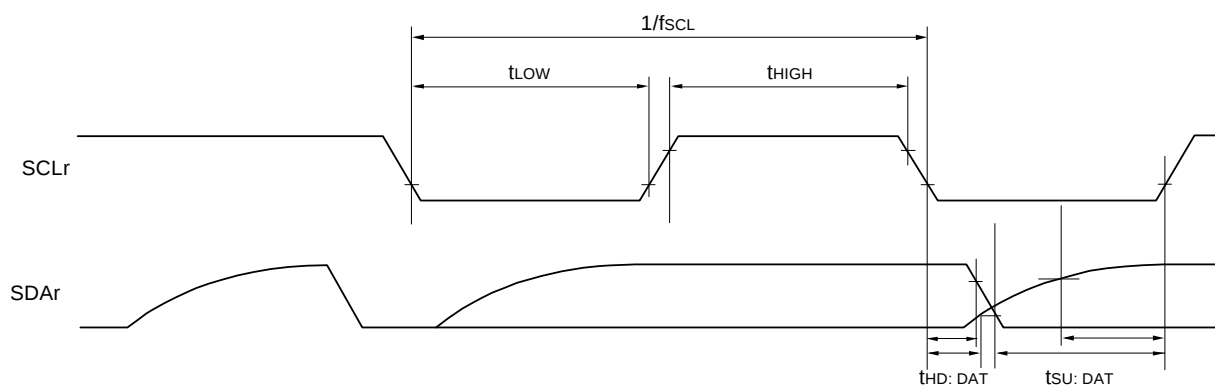
(4) During communication at same potential (simplified I²C mode)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	4600		ns
Data setup time (reception)	t _{SU: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 220 Note 2		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 580 Note 2		ns
Data hold time (transmission)	t _{HD: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.4 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Remark 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01), g: PIM number (g = 1), h: POM number (h = 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),

n: Channel number (n = 0, 1), mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.0	Mbps
			2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.0	Mbps
			2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 2	2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb [V]: Communication line voltage**Remark 2.** q: UART number (q = 0, 1), g: PIM or POM number (g = 1)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
Transfer rate		Transmission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.0 Note 2	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 Note 6	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ VDD ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ VDD < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

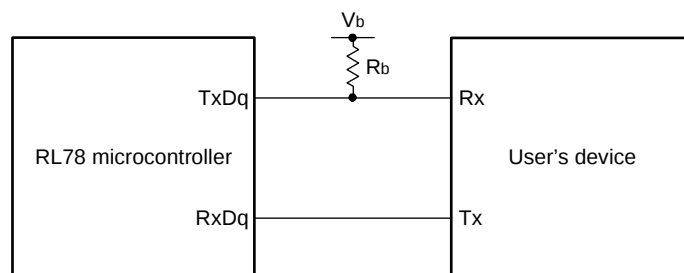
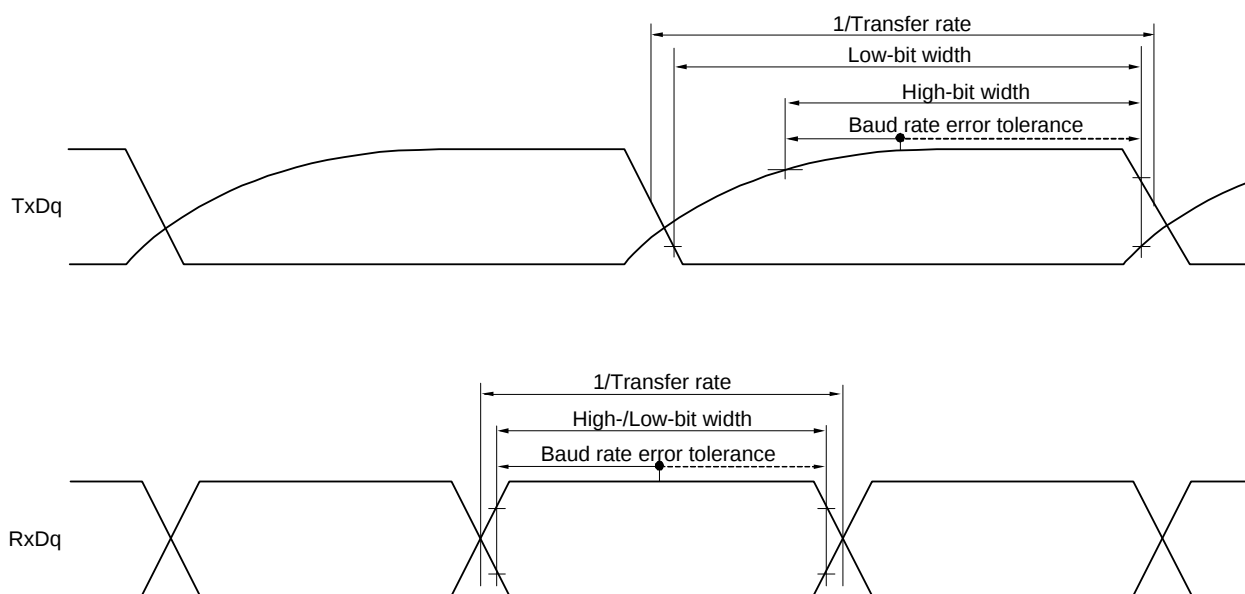
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

- Remark 1.** R_b [Ω]: Communication line (TxDq) pull-up resistance,
 C_b [F]: Communication line (TxDq) load capacitance, V_b [V]: Communication line voltage
- Remark 2.** q: UART number (q = 0, 1), g: PIM or POM number (g = 1)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	600		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	1000		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	2300		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 150		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 340		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 916		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 24		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 36		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 - 100		ns

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	162		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	354		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) ^{Note}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output ^{Note}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		200	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		390	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

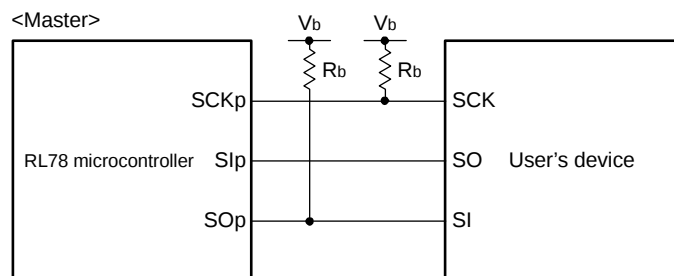
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	88		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	88		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) ^{Note}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	38		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	38		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		50	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		50	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

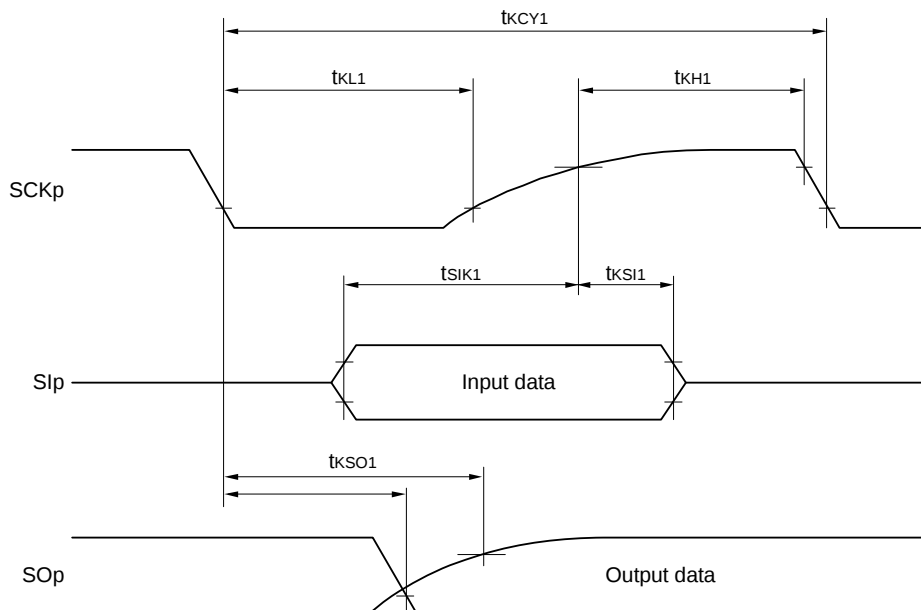
Remark 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

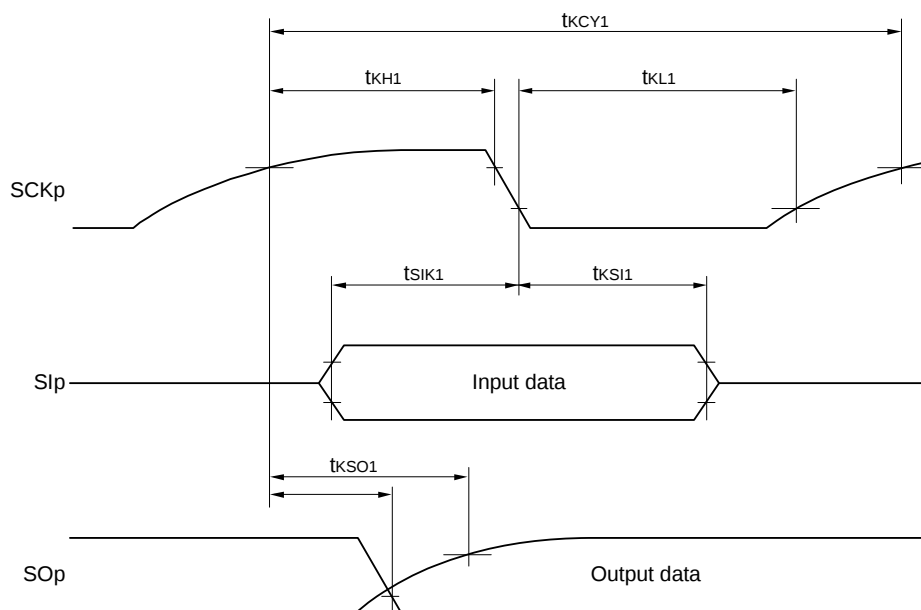
Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

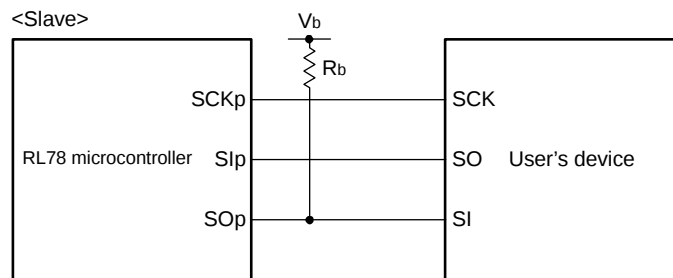
Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 - 24		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 - 36		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		t _{KCY2} /2 - 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 40		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 40		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}			1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 240	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns

(Notes, Cautions, and Remarks are listed on the next page.)

<R>
<R>

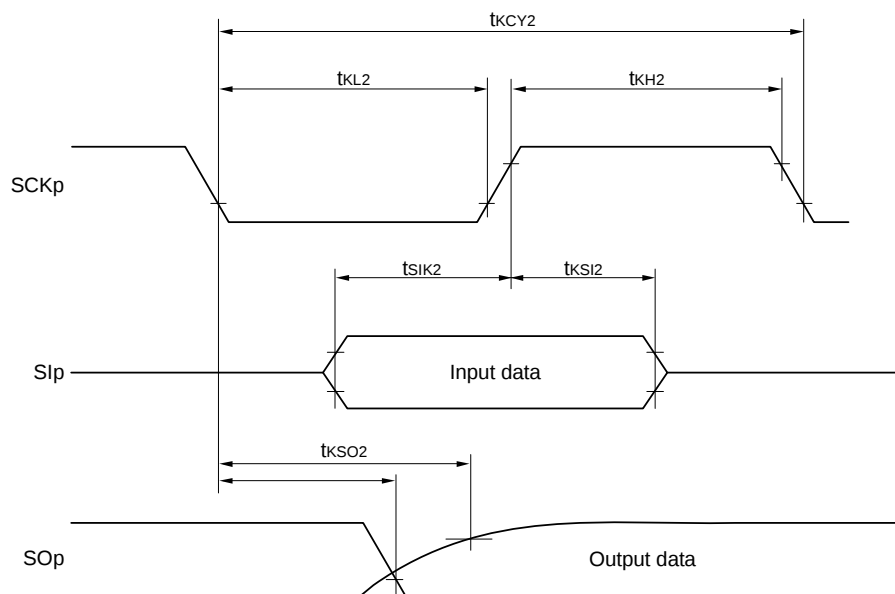
- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (VDD tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

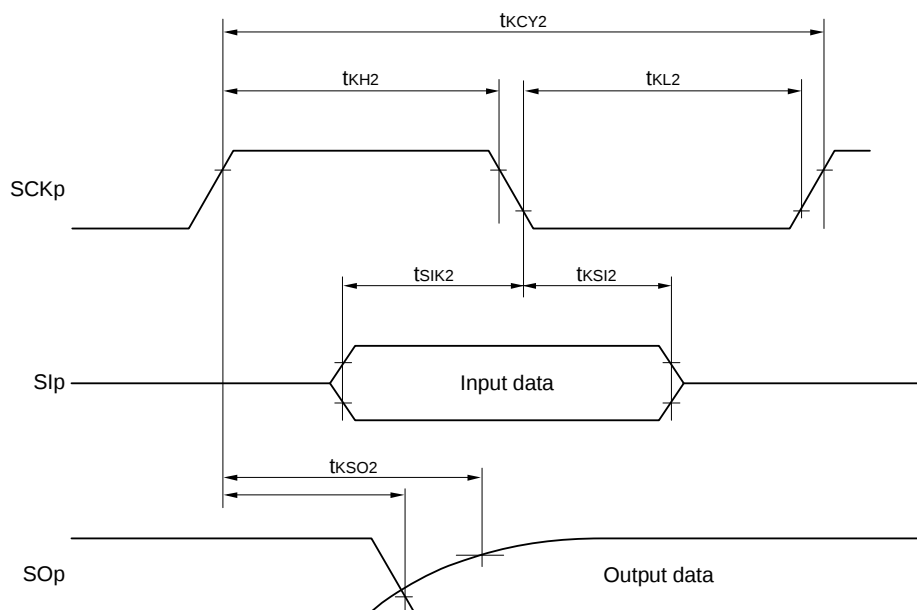


- Remark 1.** Rb [Ω]: Communication line (SOp) pull-up resistance, Cb [F]: Communication line (SOp) load capacitance, Vb [V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)
- Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))
- Remark 4.** Communication at different potential cannot be performed during clocked serial communication with the slave select function.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM or POM number (g = 1)

Remark 2. Communication at different potential cannot be performed during clocked serial communication with the slave select function.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	4600		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	4600		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	620		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	500		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	2700		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	2400		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1830		ns

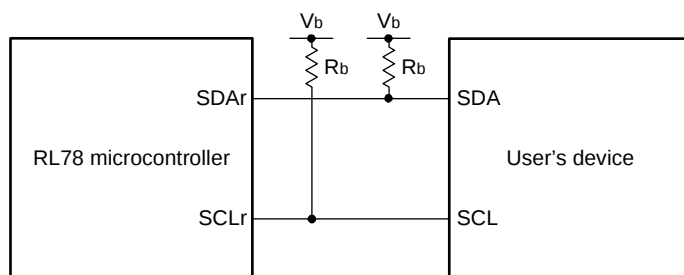
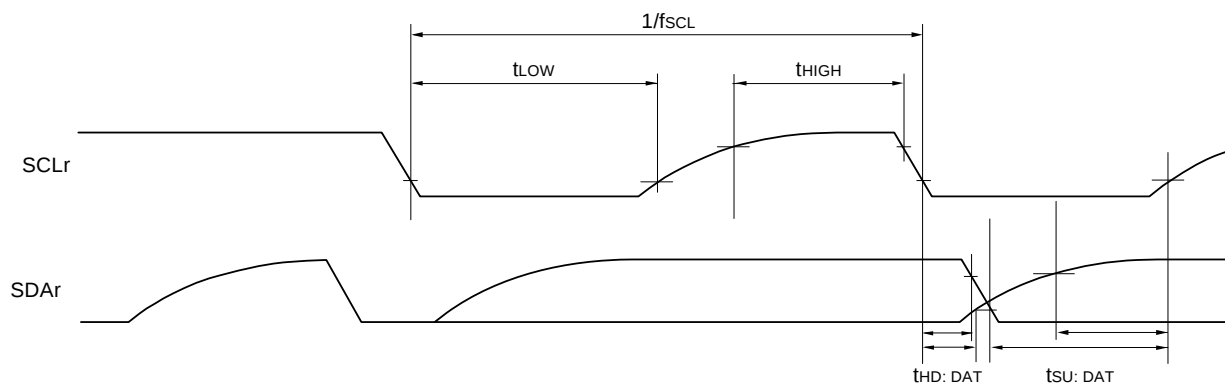
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +125°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 1		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 2		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 570 Note 2		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	0	1215	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Remark 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01), g: PIM, POM number (g = 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00, 01)

3.6 Analog Characteristics

3.6.1 Programmable gain instrumentation amplifier and 24-bit $\Delta\Sigma$ A/D converter

(1) Analog input in differential input mode

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Full-scale differential input voltage range	V _{ID}	V _{ID} = (PGAxP - PGAxN) (x = 0 to 3)		± 800 /G _{TOTAL}		mV
Input voltage range	V _I	Each of PGAxP and PGAxN pins (x = 0 to 3)	0.2		1.8	V
Common mode input voltage	V _{COM}	doFR = 0 mV	0.2+(V _{ID} x G _{SET1})/2		1.8-(V _{ID} x G _{SET1})/2	V
Input bias current	I _{IN}	V _I = 1.0 V			± 50	nA
Input offset current	I _{INOFFR}	V _I = 1.0 V			± 20	nA

(2) Analog input in single-ended input mode

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	V _I	Each of PGAxP and PGAxN pins (x = 0 to 3) G _{SET1} = 1, G _{SET2} = 1	0.2		1.8	V
Input bias current	I _{IN}	V _I = 1.0 V			± 50	nA

(3) Programmable gain instrumentation amplifier and 24-bit $\Delta\Sigma$ A/D converter

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used, in differential input mode) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				24	bit
Sampling frequency	fs1	Normal mode		1		MHz
	fs2	Low power mode		0.125		MHz
Output data rate	f _{DATA1}	Normal mode	0.48828		15.625	ksps
	f _{DATA2}	Low power mode	61.03615		1953.125	sps
Gain setting range	G _{TOTAL}	G _{TOTAL} = G _{SET1} × G _{SET2}	1		64	V/V
1st gain setting range	G _{SET1}	In differential input mode only		1, 2, 3, 4, 8		V/V
2nd gain setting range	G _{SET2}	In differential input mode only		1, 2, 4, 8		V/V
Offset adjustment bit range	doFFB			5		bit
Offset adjustment range	doFR	Referred to input	-164/G _{SET1}		+164/G _{SET1}	mV
Offset adjustment steps	doFS	Referred to input		11/G _{SET1}		mV

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksp/s, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sp/s, SBIAS = 1.2 V, doFR = 0 mV, VCOM = 1.0 V, external clock input used, in differential input mode) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain error	EG	TA = 25°C GSET1 = 1, GSET2 = 1 Excluding SBIAS error		±0.2	±2.7	%
		TA = 25°C GSET1 = 8, GSET2 = 4 Excluding SBIAS error		±0.1		%
Gain drift ^{Note}	dEG	GSET1 = 1, GSET2 = 1 Excluding SBIAS drift		(5.6)	(22.0)	ppm/°C
		GSET1 = 8, GSET2 = 4 Excluding SBIAS drift		(9.1)		ppm/°C
Offset error	Eos	TA = 25°C GSET1 = 1, GSET2 = 1 Referred to input		±0.32	±2.90	mV
		TA = 25°C GSET1 = 8, GSET2 = 4 Referred to input		±0.03		mV
Offset drift ^{Note}	dEos	GSET1 = 1, GSET2 = 1 Referred to input		(±0.02)	(±6.00)	μV/°C
		GSET1 = 8, GSET2 = 4 Referred to input		(±0.02)		μV/°C
SND ratio	SNDR	GSET1 = 1, GSET2 = 1, fin = 50 Hz Normal mode, pin = -1 dBFS	(82)	(85)		dB
		GSET1 = 8, GSET2 = 4, fin = 50 Hz Normal mode, pin = -1 dBFS	(73)	(80)		dB
Noise	Vn	GSET1 = 1, GSET2 = 1, OSR = 2048		(13)		μVRms
		GSET1 = 8, GSET2 = 4, OSR = 2048		(0.6)		μVRms
Integral non-linearity error	INL	GSET1 = 1, GSET2 = 1, OSR = 2048		(±10)		ppmFS
Common mode rejection ratio	CMRR	VCOM = 1.0 ± 0.8 V, fin = 50 Hz GSET1 = 1, GSET2 = 1 Differential input mode	(72)	(90)		dB
Power supply rejection ratio	PSRR	AVDD = 2.7 to 5.5 V GSET1 = 1, GSET2 = 1 Differential input mode		(85)		dB
ΔΣ A/D converter input clock frequency	fADC		3.8	4	4.2	MHz

Note Calculate the gain drift and offset drift by using the following expression (for 125°C products):
 For gain drift: (MAX(EG(T(-40) to T(125))) - MIN(EG(T(-40) to T(125)))) / (125°C - (-40°C))
 For offset drift: (MAX(Eos(T(-40) to T(125))) - MIN(Eos(T(-40) to T(125)))) / (125°C - (-40°C))
 MAX(EG(T(-40) to T(125))): The maximum value of gain error when the temperature range is -40°C to 125°C
 MIN(EG(T(-40) to T(125))): The minimum value of gain error when the temperature range is -40°C to 125°C
 MAX(Eos(T(-40) to T(125))): The maximum value of offset error when the temperature range is -40°C to 125°C
 MIN(Eos(T(-40) to T(125))): The minimum value of offset error when the temperature range is -40°C to 125°C

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

3.6.2 Sensor power supply (SBIAS)

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, COUT = 0.22 μF, VOUT = 1.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	VOUT		0.5		2.2	V
Output voltage setting steps	VSTEP			0.1		V
Output voltage precision	VA	IOUT = 1 mA	(-3)		(+3)	%
Maximum output current	IOUT		5			mA
Short circuit current	ISHORT	VOUT = 0 V		40	65	mA
Load regulation	LR	1 mA ≤ IOUT ≤ 5 mA			(15)	mV
Power supply rejection ratio	PSRR	AVDD = 5.0 V + 0.1 Vpp ripple f = 100 Hz, IOUT = 2.5 mA	(45)	(50)		dB

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

3.6.3 Temperature sensor

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature coefficient for sensor	TCSNS			(756)		μV/°C
Sensor output voltage	VTEMP	TA = 25°C		226.4		mV

Remark In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

3.6.4 A/D converter characteristics

- (1) When positive reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(TA = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = AV_{DD}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V		1.2	±6.5	LSB
			2.7 V ≤ AV _{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution	4.0 V ≤ AV _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ AV _{DD} ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±0.50	%FSR
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution ANI0 to ANI9, SBIAS	4.0 V ≤ AV _{DD} ≤ 5.5 V			±3.5	LSB
			2.7 V ≤ AV _{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI9		AV _{SS}		AV _{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The number of pins depends on the product. For details, see a list of pin functions.

- (2) When positive reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), negative reference voltage (-) = AV_{SS} (ADREFM = 0), pins subject to A/D conversion: ANI0 to ANI9 and SBIAS

(TA = -40 to +125°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, positive reference voltage (+) = V_{BGR}, negative reference voltage (-) = AV_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E _{ZS}	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.7 V ≤ AV _{DD} ≤ 5.5 V			±1.0	LSB
Internal reference voltage (+)	V _{BGR}	2.7 V ≤ AV _{DD} ≤ 5.5 V		V _{BGR} Note 3			V
Analog input voltage	V _{AIN}	ANI0 to ANI9		0		V _{BGR}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See the Internal reference voltage characteristics.

3.6.5 12-bit D/A converter

(1) When positive reference voltage (+) = AVDD (DACVRF = 0)

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, positive reference voltage (+) = AVDD)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		AVDD-0.47	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution			±20	mV
Settling time	DAtset	12-bit resolution, CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.

(2) When positive reference voltage (+) = internal reference voltage (DACVRF = 1)

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, positive reference voltage (+) = VREFDA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES				(8)	bit
Internal reference voltage	VREFDA	8-bit resolution	1.34	1.45	1.54	V
Output voltage range	DAOUT	8-bit resolution	0.35		VREFDA	V
Integral non-linearity error	DAILE	8-bit resolution			±1.0	LSB
Differential non-linearity error	DADLE	8-bit resolution			±1.0	LSB
Offset error	DAErr	8-bit resolution			±30	mV
Gain error	DAEG	8-bit resolution			±20	mV
Settling time	DAtset	8-bit resolution, CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The 12-bit D/A converter characteristics are the values obtained with the configurable amplifier connected.

Remark 3. Offset error and gain error do not include error in the internal reference voltage.

3.6.6 Configurable amplifier

(TA = -40 to +125°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, VCOM = 1/2 AVDD, internally connected voltage follower)

AMP0 configuration SW setting: Positive (+) pin = ANX1, negative (-) pin = ANX0

AMP1 configuration SW setting: Positive (+) pin = ANX3, negative (-) pin = ANX2

AMP2 configuration SW setting: Positive (+) pin = ANX5, negative (-) pin = ANX4

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	VIN		AVSS		AVDD	V
Output voltage	VOL	IL = -1 mA, AVDD = 2.7 to 5.5 V		AVSS +0.02	AVSS +0.07	V
	VOH	IL = 1 mA, AVDD = 2.7 to 5.5 V	AVDD -0.15	AVDD -0.02		V
Maximum output current	IOUT	4.5 V ≤ AVDD ≤ 5.5 V	±10			mA
		2.7 V ≤ AVDD ≤ 5.5 V	±5			mA
Input-referred offset voltage	VOFF	TA = 25°C without trimming IL = 0 mA, VCOM = 1.0 V		±1	±4	mV
		TA = 25°C with trimming IL = 0 mA, VCOM = 1.0 V			±0.35	mV
Temperature coefficient for input-referred offset voltage	VOTC	IL = 0 mA		(±2)	(±8)	μV/°C
Slew rate	SR1	Normal mode CL = 50 pF, RL = 10 kΩ		(0.1)		V/μs
	SR2	High-speed mode CL = 50 pF, RL = 10 kΩ		(0.8)		V/μs
Gain bandwidth	GBW1	Normal mode CL = 50 pF, RL = 10 kΩ		(350)		kHz
	GBW2	High-speed mode CL = 50 pF, RL = 10 kΩ		(1.8)		MHz
Phase margin	θM1	Normal mode CL = 50 pF, RL = 10 kΩ		(70)		deg
	θM2	High-speed mode CL = 50 pF, RL = 10 kΩ		(60)		deg
Settling time	tset1	Normal mode CL = 50 pF, RL = 10 kΩ		(20)		μs
	tset2	High-speed mode CL = 50 pF, RL = 10 kΩ		(10)		μs
Peak-to-peak voltage noise	Enb	0.1 to 10 Hz Normal mode CL = 50 pF, RL = 10 kΩ		(2.0)		μVrms
Input-referred noise	En	f = 1 kHz Normal mode CL = 50 pF, RL = 10 kΩ		(70)		nV/√Hz
Common mode rejection ratio	CMRR	f = 1 KHz, CL = 50 pF, RL = 10 kΩ		(70)		dB
Power supply rejection ratio	PSRR	2.7 V ≤ AVDD ≤ 5.5 V CL = 50 pF, RL = 10 kΩ		(62)		dB

(Remarks are listed on the next page.)

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

Remark 2. The TYP. conditions are the conditions when TA = 25°C and AVDD = 5.0 V.

Remark 3. Unless otherwise specified, offset trimming has proceeded.

Remark 4. Unless otherwise specified, values are for operation in normal mode.

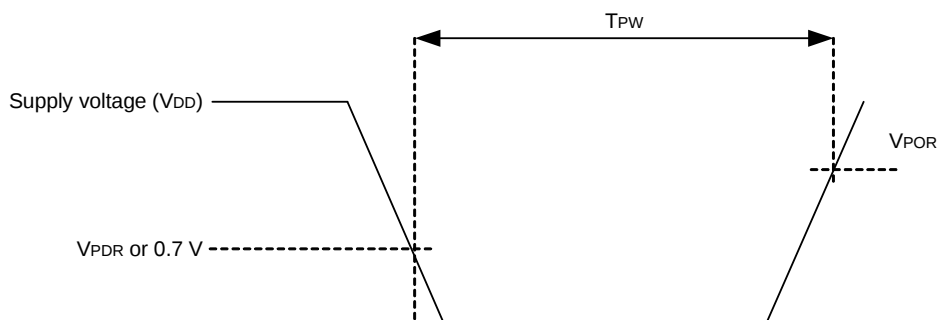
3.6.7 POR characteristics

(TA = -40 to +125°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.48	1.56	1.62	V
	VPDR	Voltage threshold on VDD falling ^{Note 1}	1.47	1.55	1.61	V
Minimum pulse width ^{Note 2}	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.8 LVD characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(TA = -40 to +125°C, VPDR ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVD0	Rising edge	4.62	4.74	4.94	V
		Falling edge	4.52	4.64	4.84	V
	VLVD1	Rising edge	4.50	4.62	4.82	V
		Falling edge	4.40	4.52	4.71	V
	VLVD2	Rising edge	4.30	4.42	4.61	V
		Falling edge	4.21	4.32	4.51	V
	VLVD3	Rising edge	3.13	3.22	3.39	V
		Falling edge	3.07	3.15	3.31	V
	VLVD4	Rising edge	2.95	3.02	3.17	V
		Falling edge	2.89	2.96	3.09	V
	VLVD5	Rising edge	2.74	2.81	2.95	V
		Falling edge	2.68	2.75	2.88	V
	VLVD6	Rising edge	2.55	2.61	2.74	V
		Falling edge	2.49	2.55	2.67	V
Minimum pulse width	tlw		300			μs
Detection delay time					300	μs

(2) LVD detection voltage in interrupt & reset mode

(TA = -40 to +125°C, VPDR ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVD6	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage		2.49	2.55	2.67	V
	VLVD4	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.17	V
			Falling interrupt voltage	2.89	2.96	3.09	V
	VLVD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		2.68	2.75	2.88	V
	VLVD2	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.61	V
			Falling interrupt voltage	4.21	4.32	4.51	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.68	2.75	2.88	V
	VLVD1	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.82	V
			Falling interrupt voltage	4.40	4.52	4.71	V
	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.68	2.75	2.88	V
	VLVD3	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	VLVD0	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.94	V
			Falling interrupt voltage	4.52	4.64	4.84	V

3.6.9 Power supply voltage rising slope characteristics

(TA = -40 to +125°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				50	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 3.4 AC Characteristics.

<R>

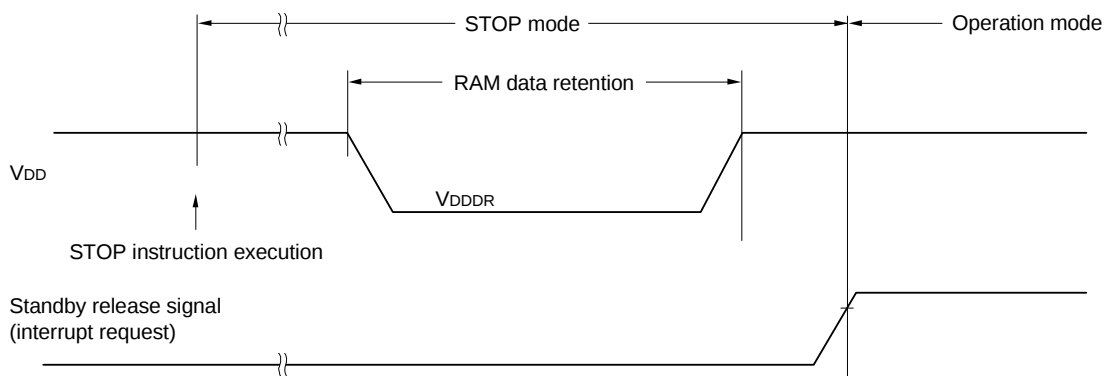
3.7 RAM Data Retention Characteristics

(TA = -40 to +125°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.47 Notes 1, 2		5.5	V

Note 1. The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Note 2. Enter STOP mode before the supply voltage falls below the recommended operating voltage.



3.8 Flash Memory Programming Characteristics

(TA = -40 to +125°C^{Note 4}, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cenwr	Retained for 20 years TA = 85°C ^{Note 5}	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C ^{Note 5}		1,000,000		
		Retained for 5 years TA = 85°C ^{Note 5}	100,000			
		Retained for 20 years TA = 85°C ^{Note 5}	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. The range is from TA = -40 to +105°C when if the flash memory programmer is in use.

Note 5. This temperature is the average value at which data are retained.

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3.9 Dedicated Flash Memory Programmer Communication (UART)

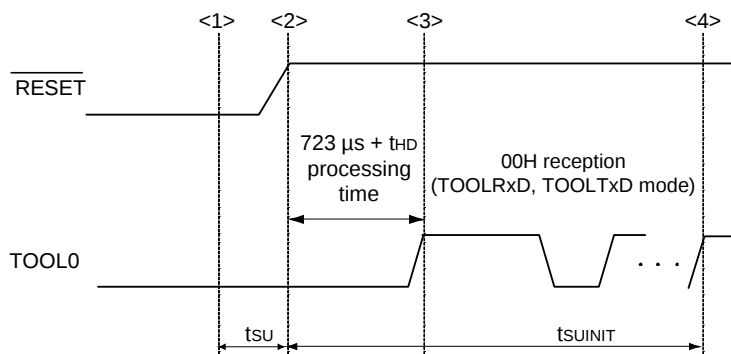
(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing for Switching Flash Memory Programming Modes

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	thd	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

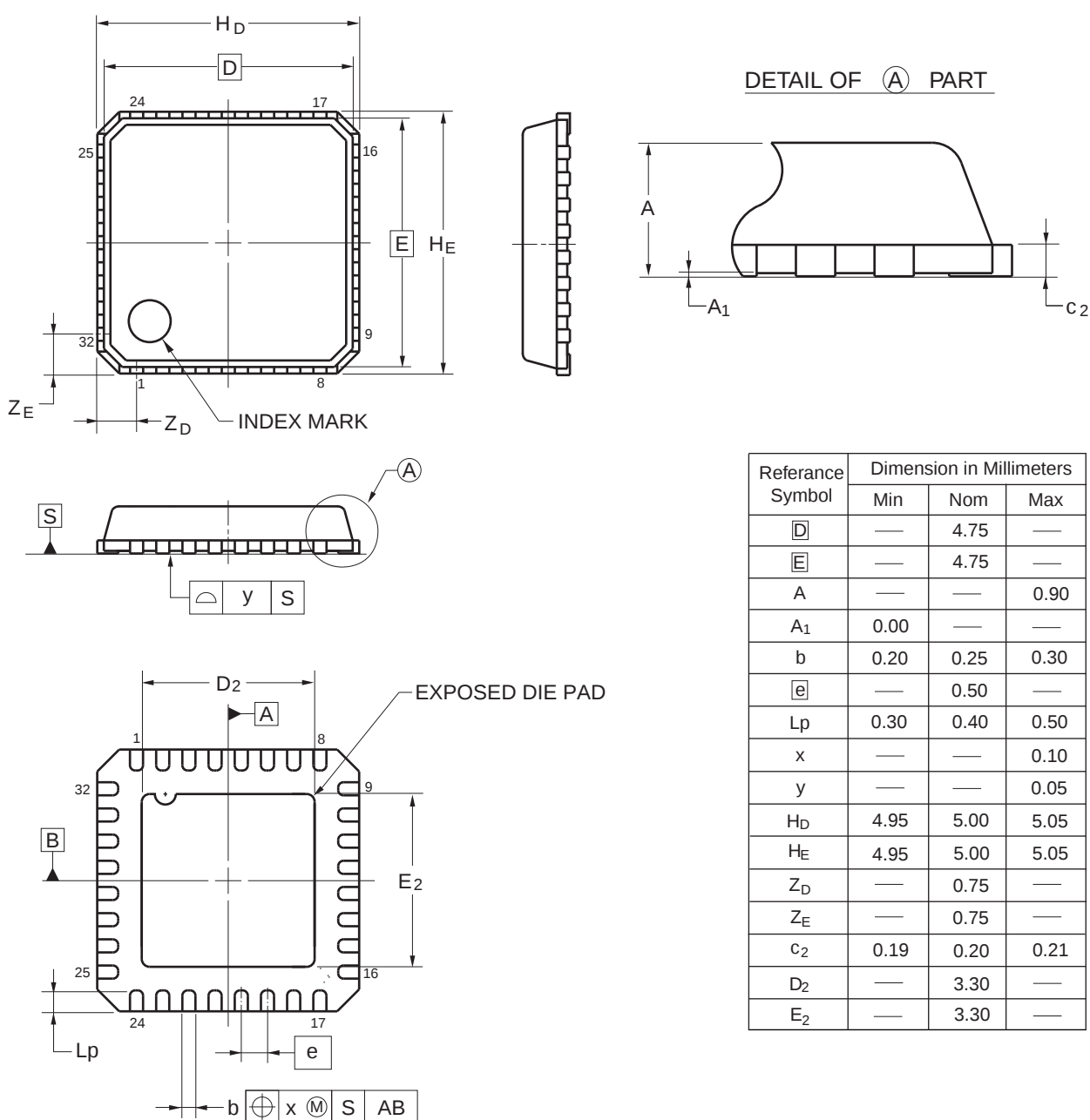
thd: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 32-pin products

R5F11CBCGNA, R5F11CBCMNA

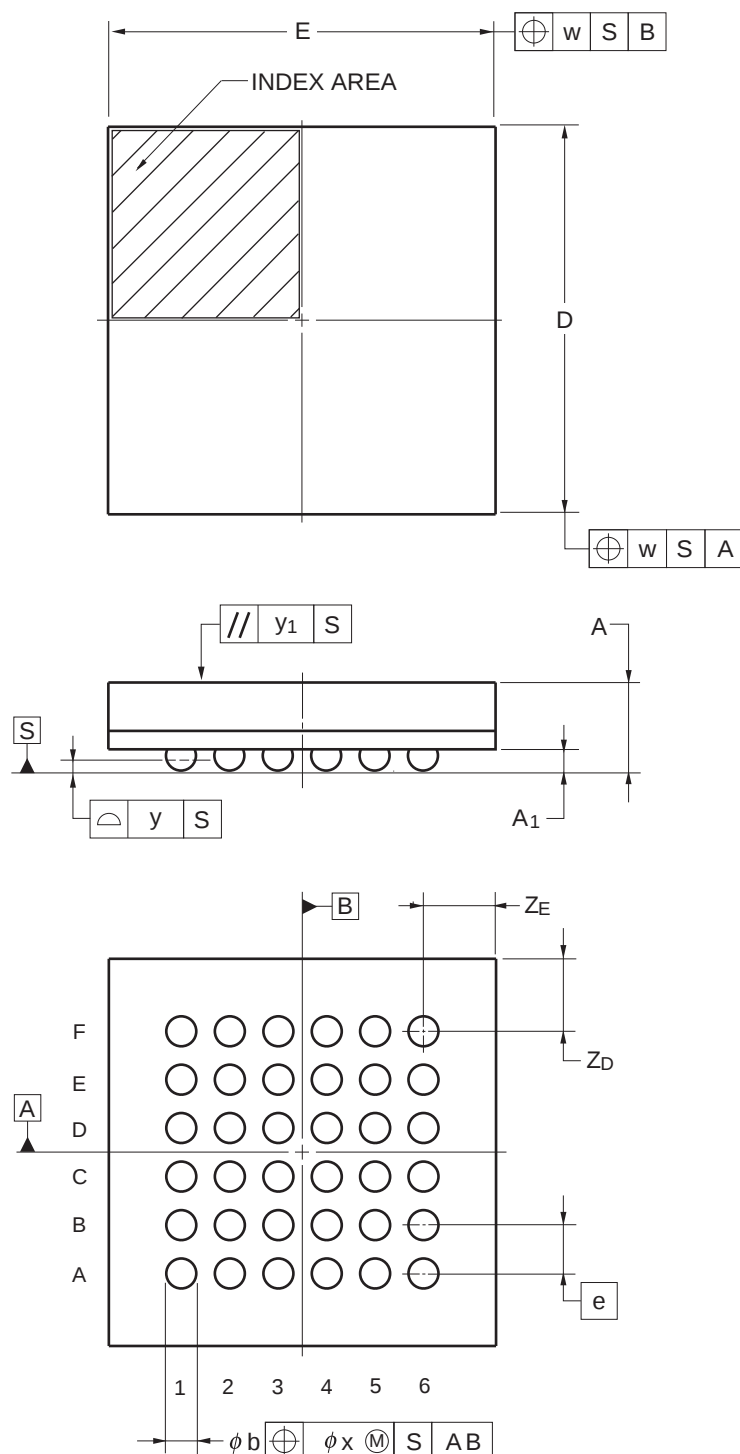
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KE-A	P32K9-50B-BAH	0.058



4.2 36-pin products

R5F11CCCGBG, R5F11CCCMBG

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TFBGA36-4x4-0.50	PTBG0036KA-A	P36F1-50-AA6	0.027



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.90	4.00	4.10
E	3.90	4.00	4.10
A	—	—	1.10
A ₁	0.17	0.22	0.27
e	—	0.50	—
b	0.26	0.31	0.36
x	—	—	0.05
y	—	—	0.08
y ₁	—	—	0.20
Z _D	—	0.75	—
Z _E	—	0.75	—
w	—	—	0.20

REVISION HISTORY	RL78/I1E Datasheet
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Rev.	Date	Description	
		Page	Summary
1.10	Jun 30, 2016	4	Addition of products name in 1.3.1 32-pin products
		5	Addition of products name in 1.3.2 36-pin products
		10	Change of DTC in 1.6 Outline of Functions
		10	Addition of Note1 in 1.6 Outline of Functions
		43	Change of 2.5.1 (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock in input)
		57	Change of 2.7 RAM Data Retention Characteristics
		57	Change of 2.8 Flash Memory Programming Characteristics
		62	Change of 3.2.2 On-chip oscillator characteristics
		91	Change of 3.5.1 (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock in input)
		105	Change of 3.7 RAM Data Retention Characteristics
		105	Change of 3.8 Flash Memory Programming Characteristics
1.00	Jul 31, 2015	—	First Edition issued

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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