User's Guide
SLWU006F–December 2004–Revised August 2010

DAC5686 EVM

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1 Overview

This user's guide document gives a general overview of the DAC5686 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

1.1 Purpose

The DAC5686 EVM provides a platform for evaluating the DAC5686 digital-to-analog converter (DAC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with CMOS level signals up to 160 MSPS through two 34-pin headers. This enables the user to provide high-speed digital data to the DAC5686 device.

The analog outputs from the DAC are available via SMA connectors. Because of its flexible design the analog output of the DAC5686 device can be configured to drive a doubly terminated 50-Ω cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to AVDD.

The EVM allows for different clock configurations. The user can input a single-ended, differential ECL/PECL or TTL/CMOS level signal, to be used to generate a single-ended or differential clock source. See Section 4.1 for proper configuration and operation.

Power connections to the EVM are via banana jack sockets.

In addition to the internal bandgap reference provided by the DAC5686 device, options on the EVM allow an external reference to be provided to the DAC.

The DAC5686 EVM allows the user to program the DAC5686 internal registers with the supplied computer parallel port cable and serial interface software. The interface allows read and write access to all registers that define the operation mode of the DAC5686 device.

1.3 Power Requirements

The demonstration board requires a minimum of two power supplies. For non-PLL and 3.3-V I/O operation, connect 3.3 Vdc to banana jack J7 with the return connected to J9. Connect 1.8 Vdc to banana jack J8 and the return to J10. Jumper W2 selects the digital I/O voltage level and jumper W3 enables the PLL.

1.3.1 Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 Software Installation

All necessary software to operate the serial interface is provided on the enclosed CD-ROM.

1. Insert the CD-ROM into the computer to be used to operate the serial interface.
2. Unzip the contents of the DAC5686SPI_Installv1p1.zip into the C:\temp directory on the PC.
3. Run the file called **setup.exe** in the C:\temp\Installer directory.
4. The software will install the appropriate files to the C:\Program Files\TI.fdr directory.
5. Once the installation is complete, the computer should be rebooted. The software is launched by running **C:\ProgramFiles\TI.fdr\DAC5686_SPI\DAC5686_SPI.exe**.

A shortcut for that program can be created and placed on the desktop or any other relevant location. See Section 2, *DAC5686 EVM Operational Procedure*, for instructions on operating the serial interface software.

1.5 Hardware Configuration

The DAC5686 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with the following factory-set configuration:

- Differential clock mode using transformers T3 and T4. Input single-ended clocks are required at J3 and J4.
- Transformer-coupled outputs using transformers T1 and T2.
- The converter is set to operate with internal reference. Jumper W1 is installed between pins 2 and 3.
- Full-scale output current set to 20 mA through RBIAS resistor R1.
- The DAC5686 output is enabled (sleep mode disabled).
- TXENABLE is set high to enable the DAC5686 device to process data.
- Internal PLL disabled. Jumper W3 is installed between pins 2 and 3.
- Input data level is set to +3.3VDC. Jumper W2 is installed between pins 1 and 2.

To prepare the DAC5686 EVM for evaluation, connect the following:

1. 3.3 V to J7 and the return to J9.
2. 1.8 V to J8 and the return to J10.
3. Provide a single-ended, 300-mV_{PP} , 0-V offset sine-wave signal to SMA connector J3 (CLK1) if the internal PLL is to be used. Connect this signal to SMA connector J4 (CLK2) if the PLL is disabled. A second sine-wave source is required only for dual clock mode. In this mode, the signal on CLK1 is used to clock data into the DAC5686 and the signal on CLK2 is used to clock the internal DAC. CLK1 and CLK2 must be phase-aligned for this option to work properly. In order to preserve the specified performance of the DAC5686 converter, the clock sources must feature very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.
4. Use a digital test pattern generator with 50-Ω outputs to provide 3.3-V CMOS logic level inputs to connectors J13 and J14. Adjust the digital inputs to provide the proper setup and hold times at the DAC5686 inputs. See the DAC5686 data sheet (SLWS147) for timing information.
5. Connect one end of the supplied serial interface cable to the parallel port of a PC. Connect the other end of the cable to J1 on the EVM.
6. The DAC5686 outputs can be monitored using SMA connector J5 for IOUTA and SMA connector J19 for IOUTB.

2 DAC5686 EVM Operational Procedure

This chapter describes the serial interface GUI.

To prepare the DAC5686 EVM for operation, connect one end of the supplied serial interface cable to the parallel port of a PC and the other end of the cable to J1 on the EVM.

2.1 Starting the Serial Interface Program

Power up the EVM. After power up, depress switch S1 to reset the DAC5686. Start the software by running **DAC5686_SPI.exe**. If the EVM is powered on with the parallel port connected properly, then the GUI shown in Figure 1 is displayed with the default settings read from the device. If there is a problem with the communication, such as the EVM is not powered on or the parallel port cable is not connected, an error message will be displayed instructing the user to correct the problem. Once corrected, hit the Read All button to read the default settings of the device.

For normal operation, the user needs only to select values and switches as desired. The values are automatically sent to the device and read back to verify their configuration.

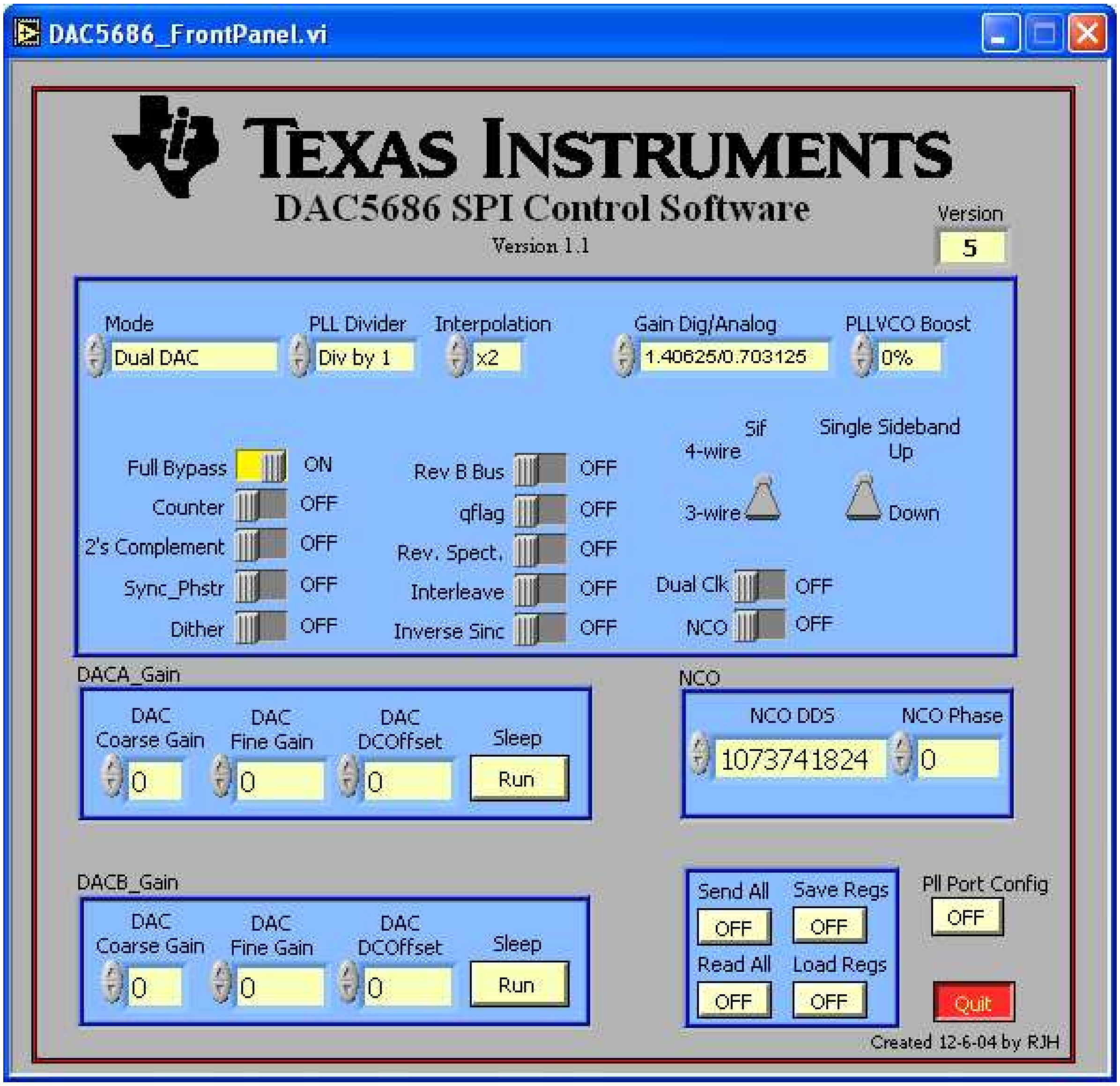

Figure 1. Serial Interface GUI

2.2 DAC5686 EVM Initial Setup Tests

There are several initial tests with the DAC5686 that can be done without any input data. The following setup steps are suggested to familiarize the user with the DAC5686 and EVM software and verify that the DAC5686 is functioning properly.

1. Provide a CLK2 input and disable the internal PLL (W3 between pins 2 and 3). Do not provide parallel input data.
2. Power up the EVM with 1.8 V DVDD and 3.3 V AVDD
3. Start the DAC5686_SPI software.
4. Turn "Full Bypass" off, change Interpolation to "x4", set Mode to "Single Sideband" and the Coarse Gain for both DACs to 15. The GUI should now look as shown in Figure 2.

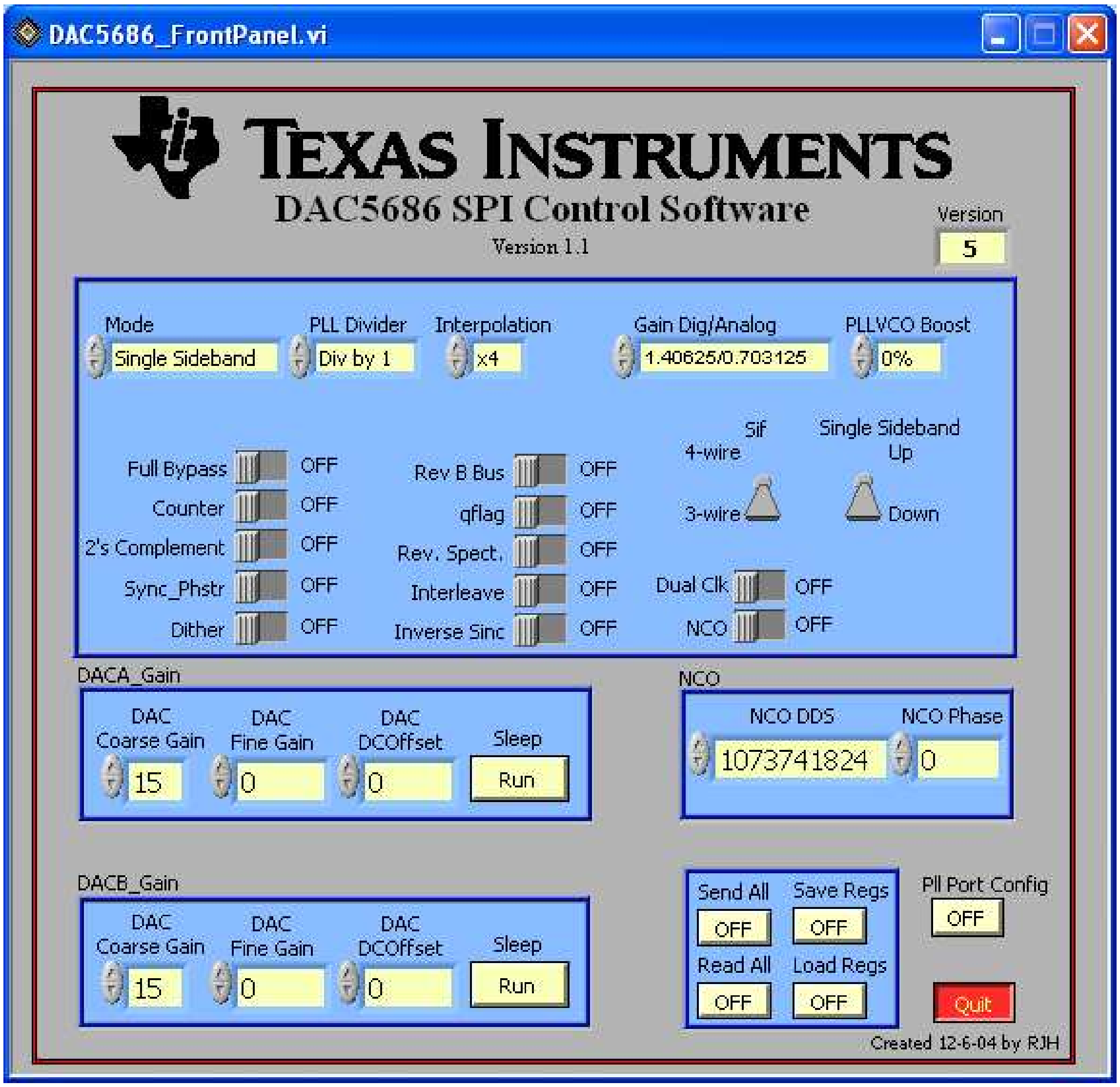

Figure 2. DAC5686 Setup for X4 Interpolation, Single Sideband Mode and Tone at Fdac/4

A tone at a frequency of CLK2/4 should now be present at connectors J5 (IOUTA) and J19 (IOUTB). In the case of CLK2 = 500 MHz, the output spectrum should be similar to Figure 3, with a tone at 125MHz.

This tone is being generated by the DAC5686 Fdac/4 Coarse Mixer as with no input data provided to connectors J13 and J14, the Channel A and B data bus inputs will all be zeros, or a full scale negative value in the default offset binary format.

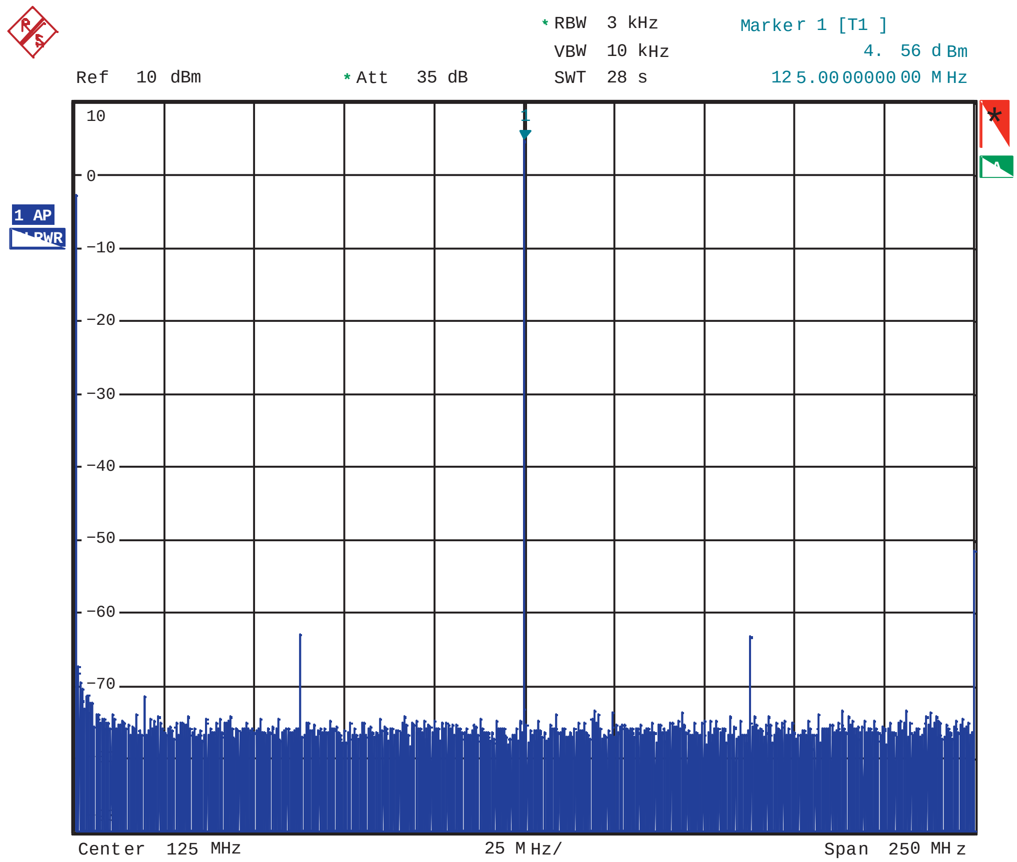

Figure 3. Spectrum with CLK2 = 500 MHz, X4 Interpolation, Single Sideband Mode, NCO Off

5. Reduce the CLK2 frequency to less than 320MHz. Enable the NCO and change the NCO DDS to 536870912. Doing this will generate a tone at Fdac/8. For CLK2 = 320 MHz, the tone corresponds to 40 MHz. The output spectrum should be similar to the one in Figure 4.

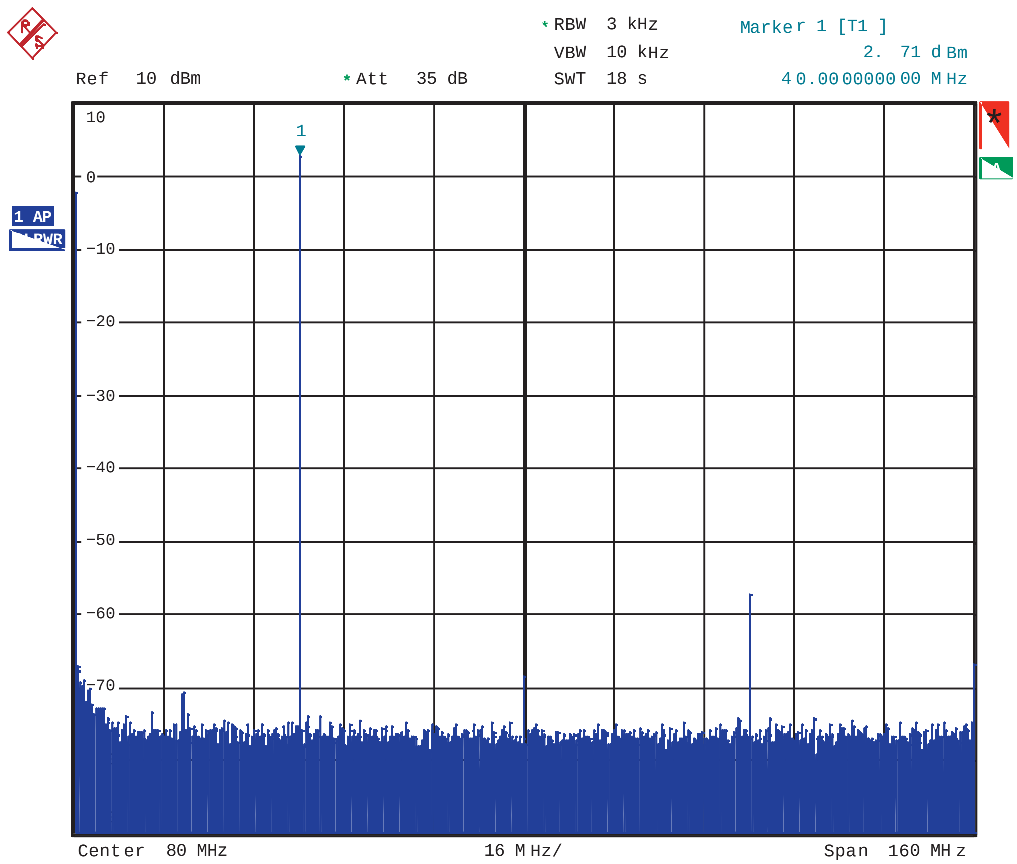

Figure 4. Spectrum with CLK2 = 320 MHz, X4 Interpolation, Single Sideband Mode and NCO Frequency = 536870912

6. Changing the NCO DDS to 268435456 will now result at an output tone at 20 MHz.

2.3 DAC5686 GUI Register Descriptions

The following section provides a brief description of each control:

2.3.1 Register Controls

- **Load Regs**: Loads register values from a saved file to the DAC5686 and updates the GUI.
- **Save Regs**: Saves current GUI registers settings to a text file for future use.
- **Read All**: Reads the current registers of the DAC5686. This is used to verify settings on the front panel.
- **Send All**: Sends the current front panel registers to the device. This is generally only used when the EVM power has recycled or the device has been reset and the user wants to load the displayed settings to the device.

2.3.2 Configuration Controls

- **Full Bypass**: When set, all interpolation and NCO functions are bypassed. User can only use CLK2/CLK2C inputs in this mode.
- **Counter**: Uses an input counter ramp as the input data to the DAC. See the DAC5686 data sheet for more information.
- **2's Comp**: When set, input data is interpreted as 2's complement. When cleared, input data is interpreted as offset binary.
- **Sync_Phstr**: Enables the PHSTR input as a sync input to the clock dividers in external single clock mode. For example, in external single clock mode (PLLVDD = 0), with 16x interpolation, the CLK2/CLK2C signal is divided by 16 and output on the PLLLOCK pin. If this bit is set, a rising edge on the PHSTR pin will be sampled by the CLK2/CLK2C clock, and used to restart the divide by 16 circuit.
- **Dither**: Enables dithering in the PLL.
- **Rev B Bus**: When cleared, DB input data MSB to LSB order is DB(15)= MSB and DB(0)=LSB. When set, DB input data MSB to LSB order is reversed, DB(15) = LSB and DB(0) = MSB.
- **qflag**: Sets qflag bit. When set, the QFLAG input pin operates as a B sample indicator when interleaved data is enabled. When cleared, the TXENABLE rising determines the A/B timing relationship.
- **Rev. Spect**: When asserted the sin term is negated before being used in mixing. This gives the reverse spectrum in single sideband mode.
- **Interleave**: When set, interleaved input data mode is enabled; both A and B data streams are input at the DA(15:0) input pins. The TXENABLE or QFLAG pin is used to identify the I/Q sequence depending on the value the "Qflag Interleave" bit (see the following)
- **Inverse Sinc**: Enables inverse sinc correction filter.
- **Dual Clk**: Only used when the PLL is disabled. When set, two differential clocks are used to input the data to the chip; CLK1/CLK1C is used to latch the input data into the chip, and CLK2/CLK2C is used as the DAC sample clock.
- **NCO**: When set, enables NCO in Single Sideband or Quad Mod modes. The NCO is operational up to 350 MHz DAC update clock. When cleared, Single Sideband and Quad Mod modes use a fixed fs/4 mix frequency.
- **Sif**: Sets sif_4pin bit. The 4 pin serial interface mode is enabled when on, 3 pin mode when off. The DAC5686 EVM is configured for a 3 pin serial interface, so setting to a 4 bit serial interface makes reading registers impossible with the GUI.
- **Single Sideband**: When set, the data to DACB is inverted to generate upper side band output.
- **Mode**: Used to select the DAC mixer mode.
  - Dual DAC - runs the device in dual DAC mode; no mixing between the A and B datapaths.
  - Quad Mod - runs the device as a quadrature modulator. The DACA circuit is shut off and the output is on the DACB outputs.
  - Single Sideband - The device generates a hilbert transform pair on the DACA and DACB outputs suitable for connection to an analog quadrature modulator.
- **PLL Divider**: Sets PLL VCO divider to div by 1, 2, 4, or 8. Only valid when the PLL is enabled by providing +3.3 V to PLLVDD (W3 between pins 1 and 2). The VCO works best (low phase noise) when biased in the 250 to 500 MHz range. If the device is to be run with a DAC update rate below 250 MHz, set the PLL divider to 2. This allows the user to run the VCO at the 250 to 500 MHz range since the output is divided by 2.
- **Interpolation**: Sets FIR Interpolation factor: {×2, ×4, ×8, ×16}.
- **Gain Dig/Analog**: Sets the gain of the DDS to ensure that the overall gain is less than or equal to 1 (i.e. no clipping). See the DAC5686 data sheet for more information.
- **PLLVCO Boost**: Increases the Vtol current of the PLL VCO from nominal to 45% in 15% increments.

2.3.3 DAC A(B) Gain

- **DAC Coarse Gain**: Sets coarse gain of DAC A(B) full scale current. Range is 0 to 15. See the DAC5686 data sheet for full scale gain equation.
- **DAC Fine Gain**: Sets fine gain of DAC A(B) full scale current. Range is -128 to 127. See the DAC5686 data sheet for full scale gain equation.
- **DAC DCOffset**: Sets DAC A(B) DC offset register. Range is -1024 to 1023.
- **Sleep**: DAC A(B) sleeps when set, operational when cleared.

2.3.4 NCO

- **NCO DDS**: Sets NCO DDS registers. See the DAC5686 data sheet for the formula.
- **NCO Phase**: Sets initial NCO phase registers. See the DAC5686 data sheet for more information.

2.3.5 Additional Control/Monitor Registers

- **Pll Port Config**: Selection of this button will bring up a separate window that shows the parallel port configuration of the software. The EVM Menu should be loaded with "DAC EVM".
- **Quit**: Quits the operation of the DAC5686 software.
- **Version**: Displays the version of the silicon. If a version of 0 is read then the communication is not functioning and an error message will be displayed.

3 Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

3.1 PCB Layout

The EVM is constructed on a 4-layer, 6.5-inch x 4.7-inch, 0.055-inch thick PCB using FR-4 material. Figure 5 through Figure 8 show the PCB layout for the EVM.

3.1.1 PCB Layout Recommendations

The DAC5686 clock is sensitive to fast transitions of input data on pins 34, 35, and 36 (DA15, DA14, and DA13) due to coupling to DVDD pin 32. The noise-like spectral energy of the data line couples into the DAC clock circuit power pin, resulting in increased jitter. To minimize the jitter, a 10-Ω series resistor along with a 10-pF capacitor to ground has been added to DVDD pin 32 on the EVM. Pin 32 only draws around 2 mA of current and the 0.02-V voltage drop across the resistor is acceptable for DVDD voltages within the MINIMUM and MAXIMUM specifications. It is also recommended that the transition rate of the data input lines be slowed by inserting series resistors near the data source. The optimized value of the series resistor depends on the capacitance of the trace between the series resistor and the DAC5686 input pin. For a 2-3 inch trace, a 22-Ω to 47-Ω resistor are recommended.

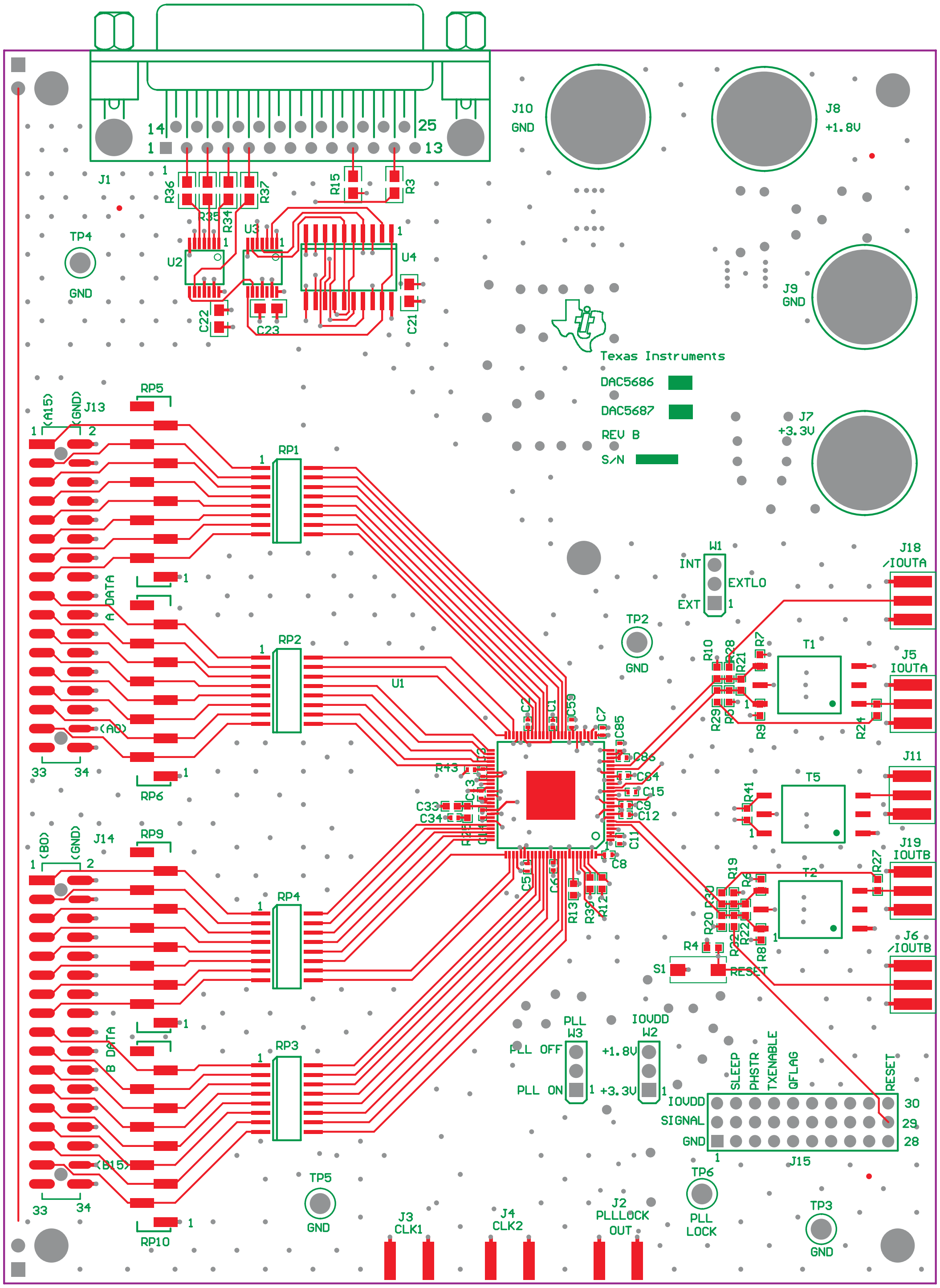

Figure 5. Top Layer 1

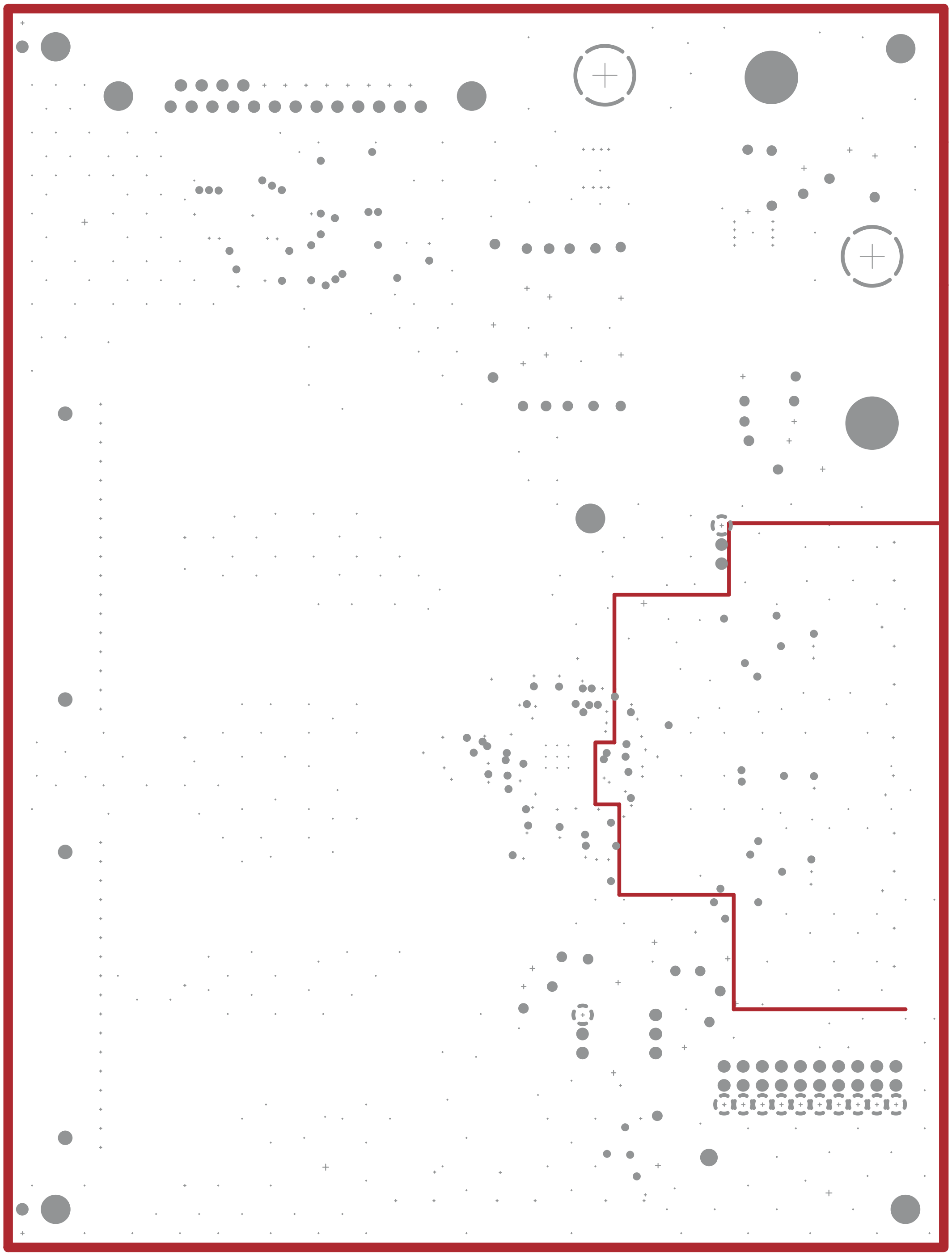

Figure 6. Layer 2, Ground Plane

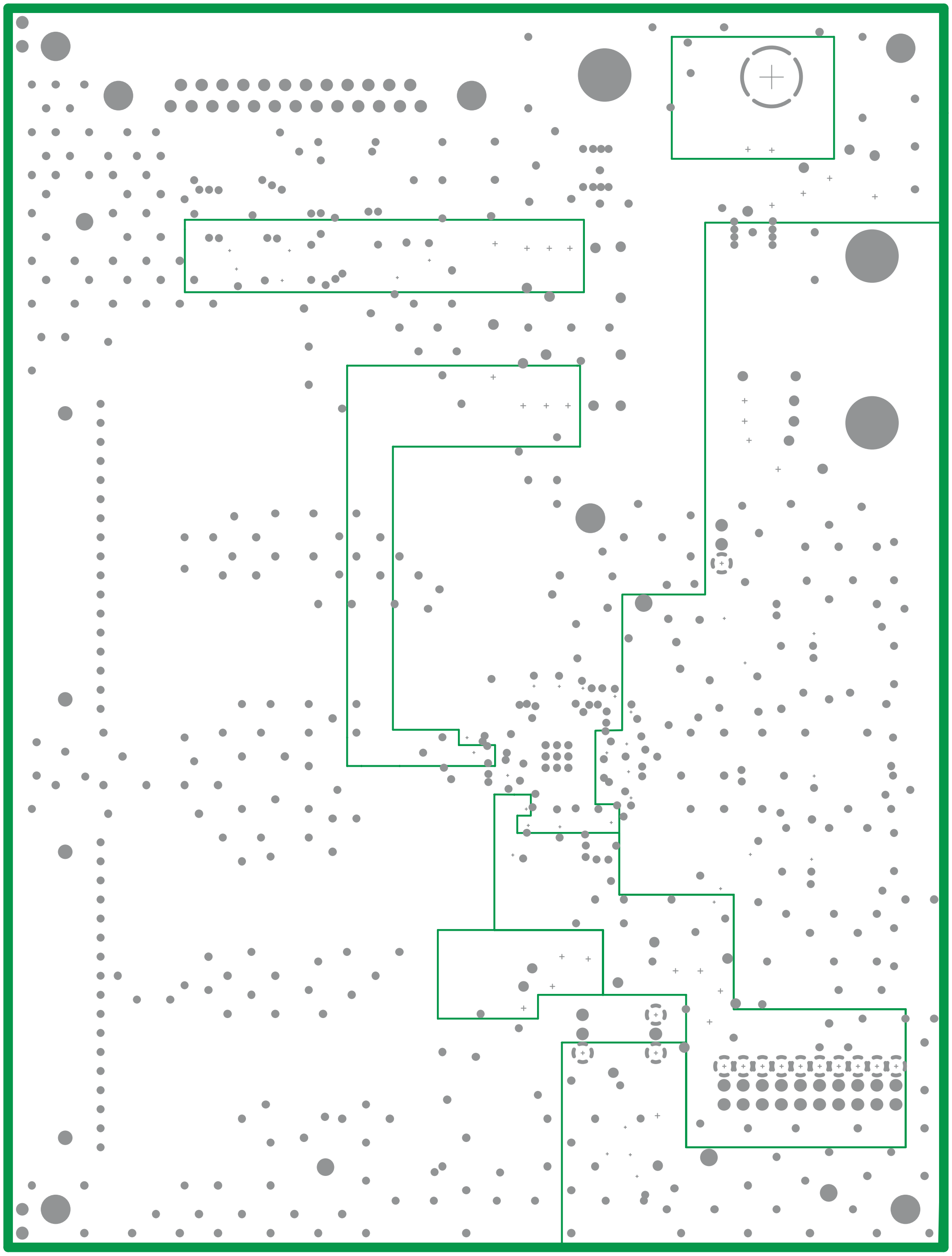

Figure 7. Layer 3, Power Plane

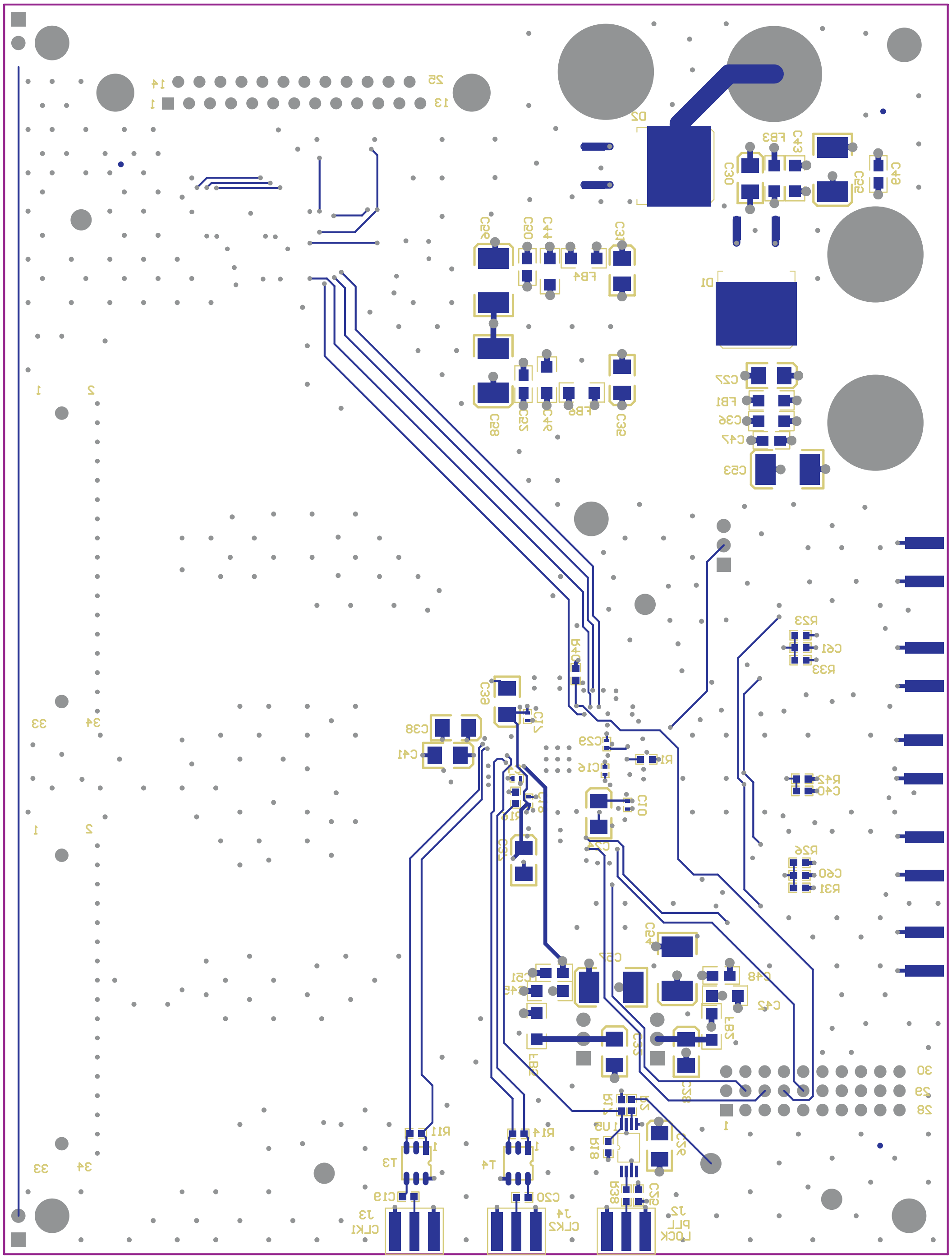

Figure 8. Bottom Layer

3.2 Parts List

Table 1 lists the parts used in constructing the EVM.

Table 1. DAC5686 EVM Parts List

Bill Of Material For DAC5686					
Value	**QTY**	**Part Number**	**Vendor**	**Ref Des**	**Not Installed**
CAPACITORS					
47 μF, tantalum, 20%, 10 V	6	ECS-T1AD476R	Panasonic	C53–C58	
10 μF, 10 V, 20% capacitor	12	ECS-T1AX106R	Panasonic	C24, C26–C28, C30–C32, C35, C37–C39, C41	
1 μF, 16 V, 10% capacitor	6	ECJ-3YB1C105K	Panasonic	C36, C42–C46	
0.1 μF, 16 V, 10% capacitor	1	ECJ-2VB1C104K	Panasonic	C21	
0.01 μF, 50 V, 10% capacitor	6	ECJ-2VB1H103K	Panasonic	C47-C52	
120 pf, 50 V, 5% Capacitor	1	ECJ-1VC1H121J	Panasonic	C33	
0.01 μF, 16 V, 10% capacitor	2	ECJ-1VB1C103K	Panasonic	C19, C20	
0.1 μF, 16 V, 10% capacitor	3	ECJ-1VB1C104K	Panasonic	C25, C60, C61	
0.1 μF, 16 V, +80%, -20% capacitor	21	ECJ-0EF1C104Z	Panasonic	C1, C2, C4–C13, C15–C18, C29, C59, C84–C86	
10 pF, 50 V, ±0.5 pF Capacitor	1	ECU-E1H100DCQ	Panasonic	C3	
15000 pF, 16 V, 10% capacitor	1	ECJ-0EB1C153K	Panasonic	C34	
0.01 μF, 25 V, 10% capacitor	1	ECJ-0EF1E103Z	Panasonic	C14	
120 pF, 50 V, 5% capacitor	1	ECU-V1H121JCV	Panasonic	C33	
RESISTORS					
10-kΩ resistor 1/16 W, 1%	4	ERJ-6ENF1002V	Panasonic	R34–R37	
10-Ω resistor 1/16 W, 1%	1	ERJ-6ENF10R0V	Panasonic	R3	R15
0-Ω resistor, 1/16 W, 1%	2	ERJ-3GEY0R00V	Panasonic	R23, R26	R24, R27–R33
49.9-Ω resistor, 1/16 W, 1%	3	ERJ-3EKF49R9V	Panasonic	R12, R13, R39	R40
127-Ω resistor, 1/16 W, 1%	1	ERJ-3EKF1270V	Panasonic	R25	
200-Ω resistor, 1/16 W, 1%	2	ERJ-3EKF2000V	Panasonic	R11, R14	
1-kΩ resistor, 1/16 W, 1%	2	ERJ-3EKF1001V	Panasonic	R1, R4	
110-Ω resistor, 1/10 W, 1%	0	ERA-3EKF110V	Panasonic		R18
221-Ω resistor, 1/10 W, 1%	0	ERA-3EKF221V	Panasonic		R17
22.1-Ω resistor, 1/10 W, 1%	2	ERJ-3EKF22R1V	Panasonic	R16, R38	
10-Ω resistor, 1/16 W, 1%	1	ERJ-2RFK10R0X	Panasonic	R43	
100-Ω resistor, 1/10 W, 1%	4	ERA-3EKF100V	Panasonic	R5, R10, R19, R20	R21, R22
Surface Mount Socket strips	1	310-93-164-41-105000	Mill-Max	See Note 8	
51-Ω resistor pack	4		CTS	See Note 7	RP5, RP6, RP9, RP10
22-Ω resistor pack	4	4816P-001-220	BOURNS	RP1–RP4	
FERRITE BEADS, CONNECTORS, JUMPERS, JACKS, ICs, etc.					
MBRB2515L	2	MBRB2515LT4	On-Semiconductor	D1, D2	
Ferrite bead	6	EXC-ML32A680U		FB1–FB6	
SMA connectors	8	16F3627	Newark	J2–J6, J11, J18, J19	
Black test point	4	5001K	Keystone	TP2–TP5	
3POS_header	3	HTSW-150-07-L-S	Samtec	W1–W3	
30-pin header	1	HTSW-110-07-L-T	Samtec	J15	
34-pin header	2	TSW-117-01-S-DV-LC	Samtec	J13, J14	
Red banana jacks	2	ST-351A	Allied	J7, J8	

Table 1. DAC5686 EVM Parts List (continued)

Bill Of Material For DAC5686					
Value	**QTY**	**Part Number**	**Vendor**	**Ref Des**	**Not Installed**
Black banana jacks	2	ST-351B	Allied	J9, J10	
DAC5686PZP	1	DAC5686IPZP	TI	U1	
SN74LVC1G125DBVR	1	SN74LVC1G125D BVR	TI	U5	
SN74HC241PW	1	SN74HC241PW	TI	U4	
Transformer	2	T4-1-KK8	Mini-circuit	T1, T2	
Transformer	2	TCM4-1W	Mini-circuit	T3, T4	
DB25F-RA	1	745536-2	AMP	J1	
Mounting screws	2			J1	
Nuts	2			J1	
Switch	1	EVQ-PJX04M	Panasonic	S1	

4 Circuit Description

This chapter describes the circuit functions of the DAC5686 EVM.

4.1 Input Clocks

The initial configuration of this EVM provides transformer-coupled differential clocks from single-ended input sources. A 300-mV_{P-P} , 0-V offset, 50% duty cycle external square wave is applied to SMA connector J3 to be used as the data clock input. The signal is converted to a differential clock by transformer T3 and provides the CLK1 and CLK1C inputs to the DAC5686 device. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5686 converter, the clock source should feature very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.

A 300 mV_{PP} , 0-V offset, 50% duty cycle external square wave is applied to SMA connector J4 to be used as the DAC sample clock. The signal is converted to a differential clock by transformer T4 and provides the CLK2 and CLK2C inputs to the DAC5686 device. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5686 converter, the clock source should feature low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance.

4.2 Input Data

The DAC5686 EVM can accept 1.8-V or 3.3-V CMOS logic level data inputs through the 34-pin headers J13 and J14 per Table 2 and Table 3. The board provides 50-Ω termination option to ground and series dampening resistors to minimize digital ringing and switching noise.

Table 2. Input Connector J13 (Data A Bus)

Pin	Description	Pin	Description
1	CMOS data bit 15 (MSB)	18	GND
2	GND	19	CMOS data bit 6
3	CMOS data bit 14	20	GND
4	GND	21	CMOS data bit 5
5	CMOS data bit 13	22	GND
6	GND	23	CMOS data bit 4
7	CMOS data bit 12	24	GND
8	GND	25	CMOS data bit 3
9	CMOS data bit 11	26	GND
10	GND	27	CMOS data bit 2
11	CMOS data bit 10	28	GND
12	GND	29	CMOS data bit 1

Table 2. Input Connector J13 (Data A Bus) (continued)

Pin	Description	Pin	Description
13	CMOS data bit 9	30	GND
14	GND	31	CMOS data bit 0 (LSB)
15	CMOS data bit 8	32	GND
16	GND	33	
17	CMOS data bit 7	34	GND

Table 3. Input Connector J14 (Data B Bus)

Pin	Description	Pin	Description
1	CMOS data bit 0 (LSB)	18	GND
2	GND	19	CMOS data bit 9
3	CMOS data bit 1	20	GND
4	GND	21	CMOS data bit 10
5	CMOS data bit 2	22	GND
6	GND	23	CMOS data bit 11
7	CMOS data bit 3	24	GND
8	GND	25	CMOS data bit 12
9	CMOS data bit 4	26	GND
10	GND	27	CMOS data bit 13
11	CMOS data bit 5	28	GND
12	GND	29	CMOS data bit 14
13	CMOS data bit 6	30	GND
14	GND	31	CMOS data bit 15 (MSB)
15	CMOS data bit 7	32	GND
16	GND	33	
17	CMOS data bit 8	34	GND

4.3 Output Data

The DAC5686 EVM can be configured to drive a doubly terminated 50-W cable or provide unbuffered differential outputs.

4.3.1 Transformer-Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with single-ended output signals at SMA connectors J5 and J19. The DAC5686 outputs are configured to drive a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer with the center tap of the transformers connected to +3.3 VA as shown in Table 4. When using a 1:1 impedance ratio transformer, configure the EVM as shown in Table 4. The common mode input voltage of T1 and T2 can be adjusted by using the resistor divider networks.

Table 4. Transformer Output Configuration

Configuration	Components Installed [(1)]	Components Not Installed
1:1 Impedance ratio transformer	R5 (49.9), R10 (49.9), R19 (49.9), R20 (49.9), R21–R23, R26, C60, C61, T1(1:1), T2 (1:1)	R24, R27–R33
4:1 Impedance ratio transformer	R5, R10, R19, R20, R23, R26, C60, C61, T1, T2	R21, R22, R24, R27-R33

(1) All component values are per the schematic except where shown in parenthesis.

4.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: remove R21, R22, T1, and T2; install R5 (24.9), R10 (24.9), R19 (24.9), R20 (24.9), R24, R27-R30, and R32. With a 20 mA full-scale output current, this configuration provides a 0.5 V_{PP} output.

4.3.3 PLL Lock

With the internal PLL enabled (W3 installed between pins 1 and 2), when the PLL is locked to the CLK1 input, PLLOCK is driven high. With the internal PLL disabled, the PLLLOCK is an output clock that can be used by external devices to clock the input data to the DAC5686. This signal is the CLK2 signal divided down by the interpolation rate and phase-aligned to allow the user to clock data into the DAC5686 with the required setup and hold times.

4.4 Control Inputs

The DAC5686 device has six discrete inputs to control the operation of the device.

4.4.1 Sleep Mode

The DAC5686 EVM provides a means of placing the DAC5686 device into a power-down mode. This mode is activated by placing a jumper between pins 5 and 6 on header J15.

4.4.2 Reset

The DAC5686 EVM provides a means of resetting the DAC5686 device. Pressing switch S1 or sending J15 pin 29 low provides an active low reset signal to the DAC5686 device.

4.4.3 Phase Synchronization

The DAC5686 EVM provides a means to phase synchronize the DAC5686 device. Placing an active high signal on J15 pin 8 (PHSTR) resets the internal NCO accumulator register.

4.4.4 TxENABLE

TxENABLE must be high to enable the DAC5686 process data. When low, the DAC5686 device is forced to a constant dc output at IOUTA and IOTB. When in the interleaved mode and MEM_QFLAG bit is set to 0, TxENABLE syncronizes the data of channels A and B. When TxENABLE goes high, data present at the next clock rising edge is treated as I data. The next valid data is then treated as Q data and so on. TxENABLE is controlled by J15 pin 11.

4.4.5 QFLAG

QFLAG is an input used to indicate Q sample data during the interleaved mode when the QFLAG interleave bit (3) is set in register #9, MEM_QFLAG. When QFLAG is high, input data is treated as Q data, and when low, data is treated as I data. QFLAG is controlled by J15 pin 14.

4.4.6 PLL_ON_OFF

PLL_ON_OFF allows the user to disable the PLLLOCK output buffer. When PLL_ON_OFF is high, the buffer is disabled. When low, the PLLLOCK output signal is present at SMA connector J2.

4.5 Internal Reference Operation

The full-scale output current is set by applying an external resistor (R1) between the BIASJ pin of the DAC5686 device and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying R1 or changing the externally applied reference voltage. The full-scale output current, IOUTFS, is defined as follows:

$$IOUT_{FS} = 16 \times \left(\frac{V_{EXTIO}}{R1}\right)$$

where VEXTIO is the voltage at pin EXTIO. This voltage is 1.2 V typical when using the internally provided bandgap reference voltage source.

4.6 External Reference Operation

The internal reference can be disabled and overridden by an external reference by connecting a voltage source to terminal TP1 (EXTI/O) and connecting EXTLO to +3.3VA with jumper W1 installed between pins 1 and 2. The specified range for external reference voltages must be observed (see the DAC5686 data sheet (SLWS147) for details).

5 Schematic

This chapter contains the DAC5686 EVM schematic diagrams.

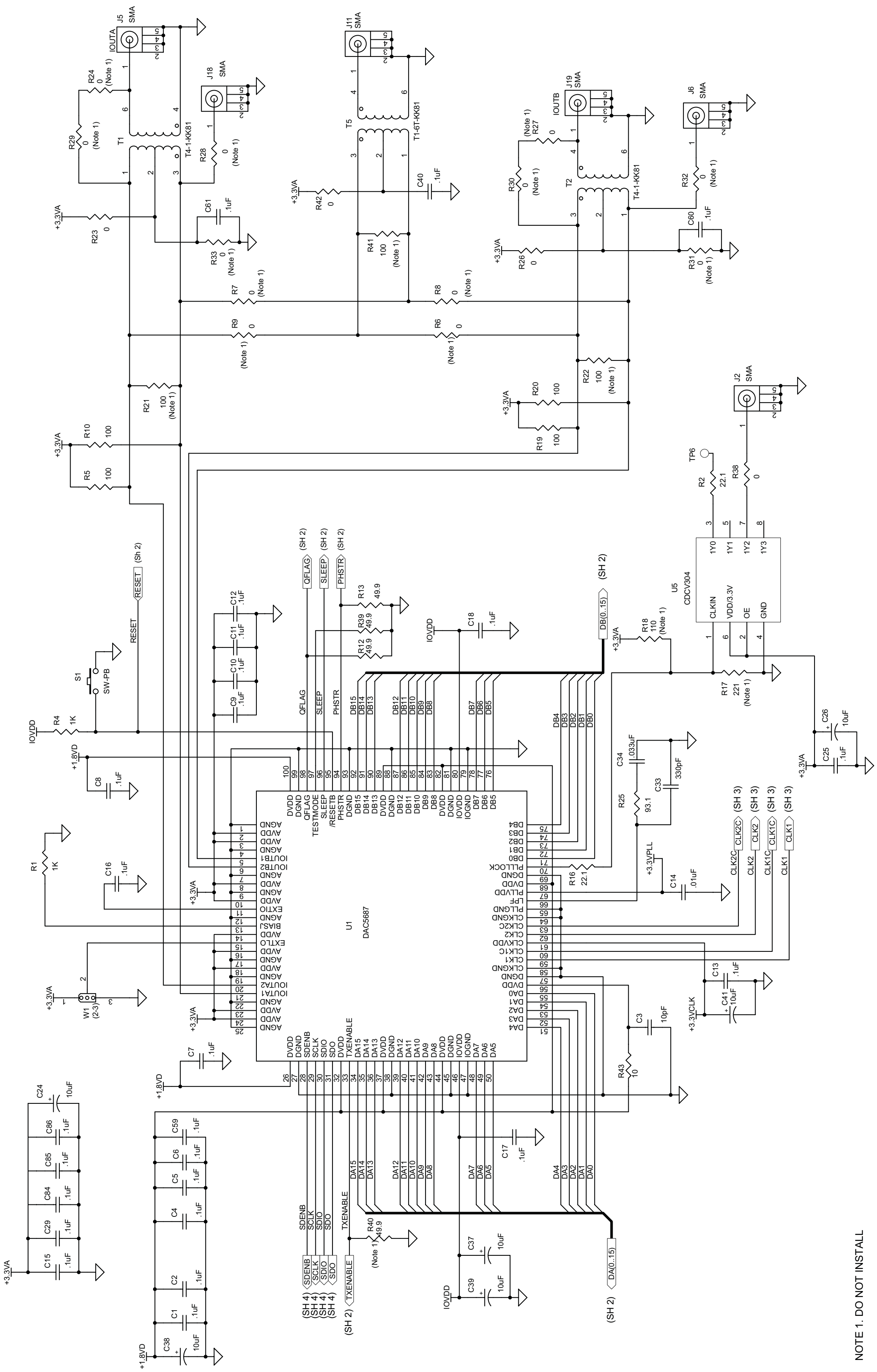

Figure 9. Schematic - Page 1

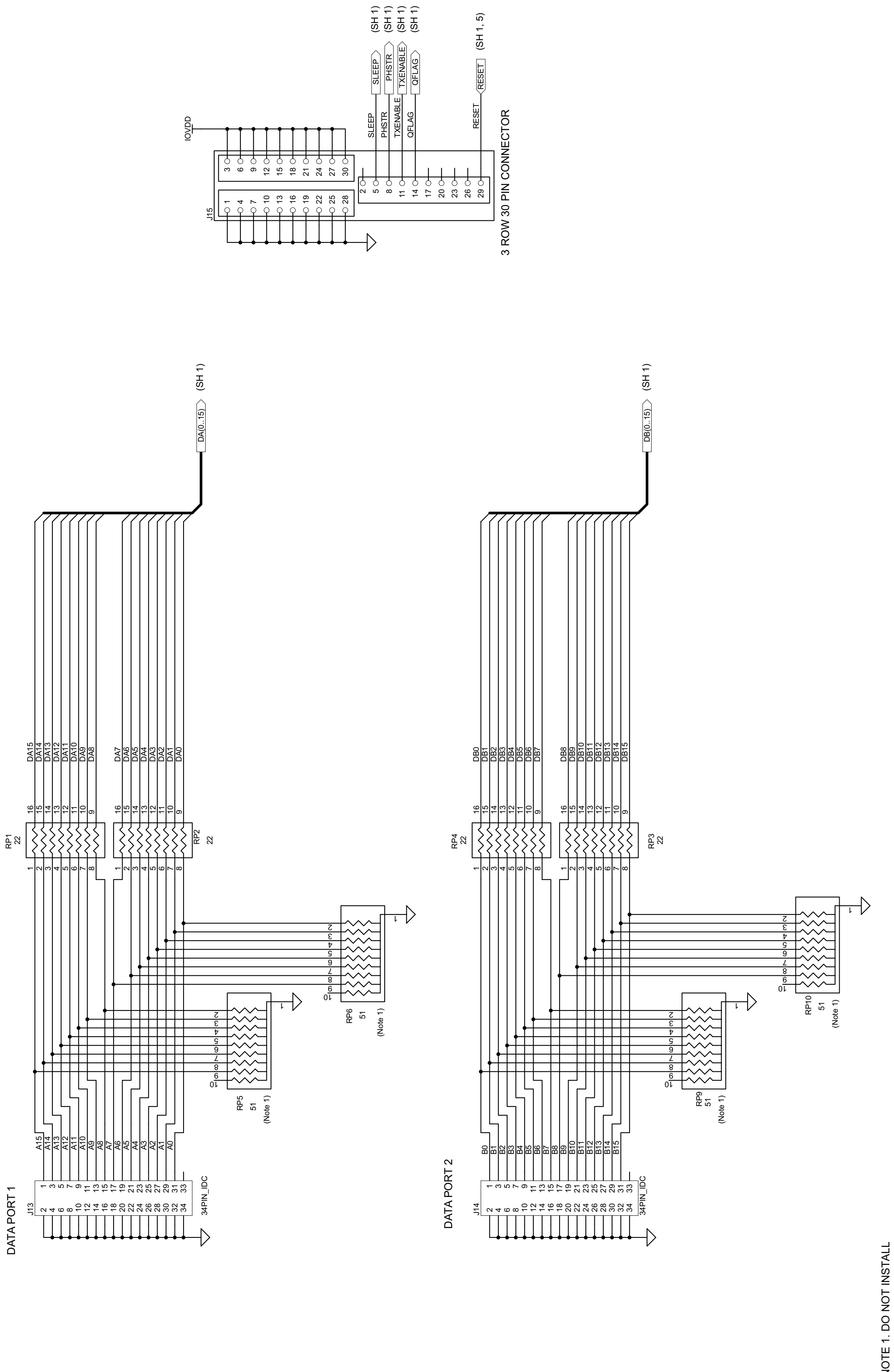

Figure 10. Schematic - Page 2

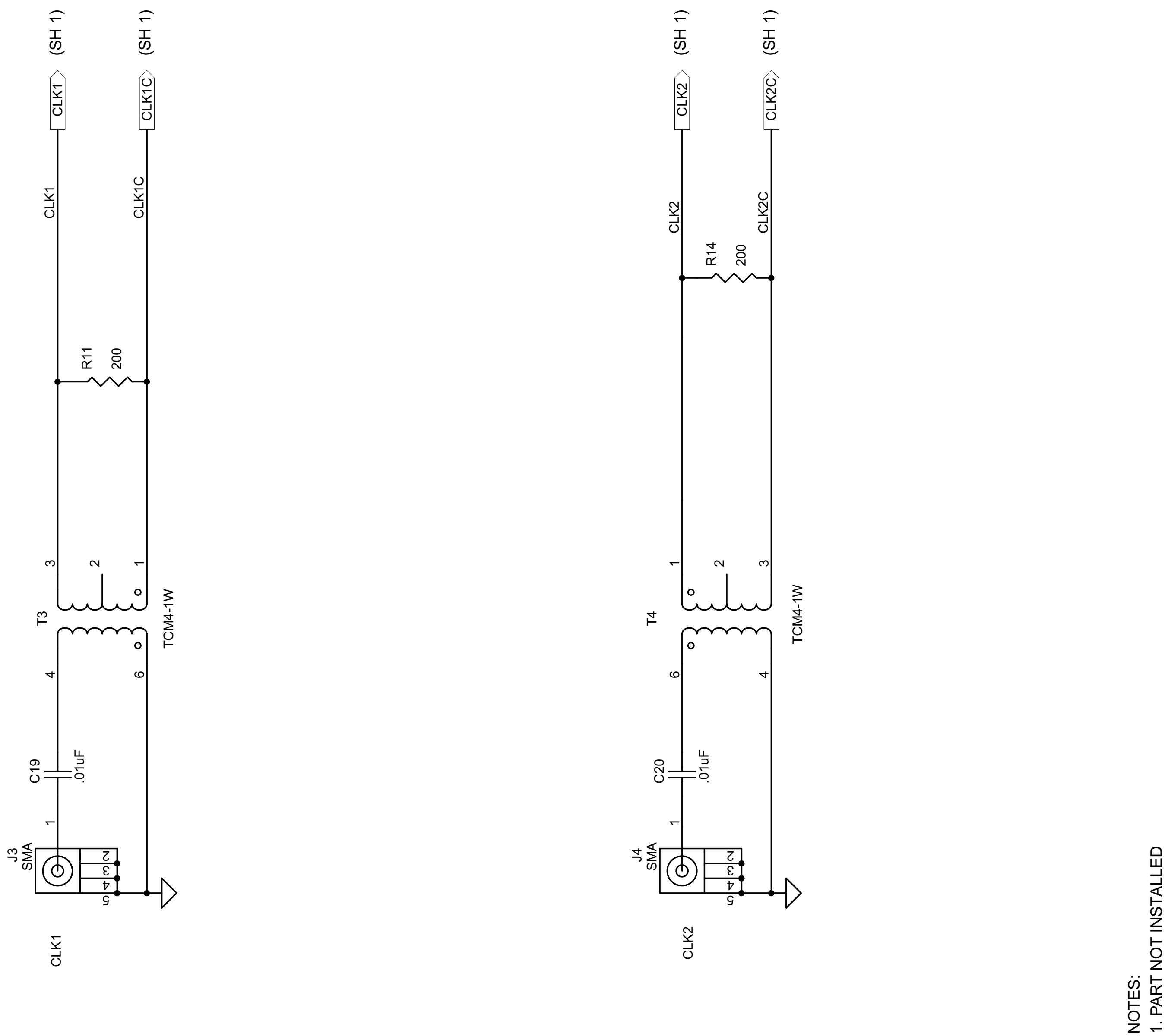

Figure 11. Schematic - Page 3

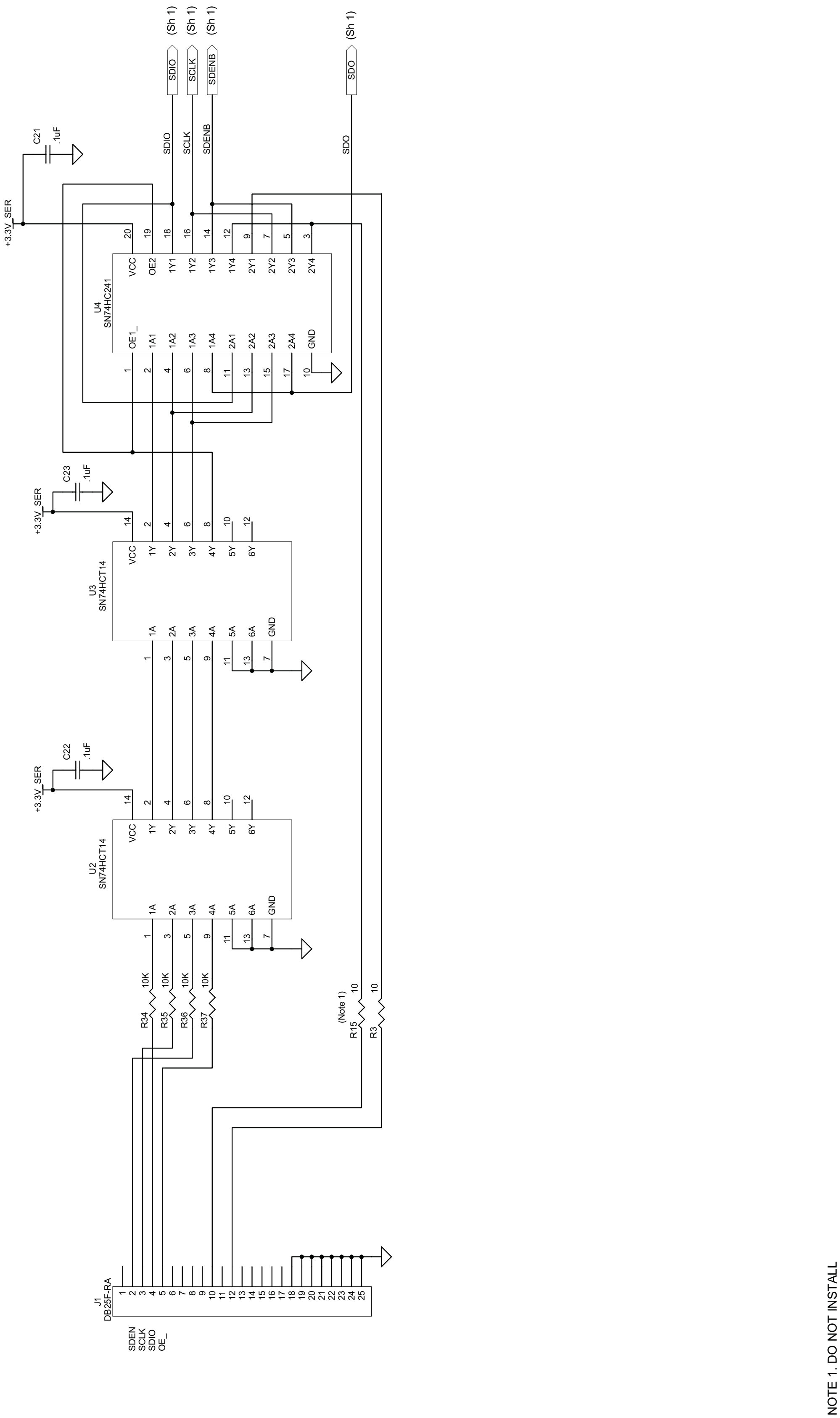

Figure 12. Schematic - Page 4

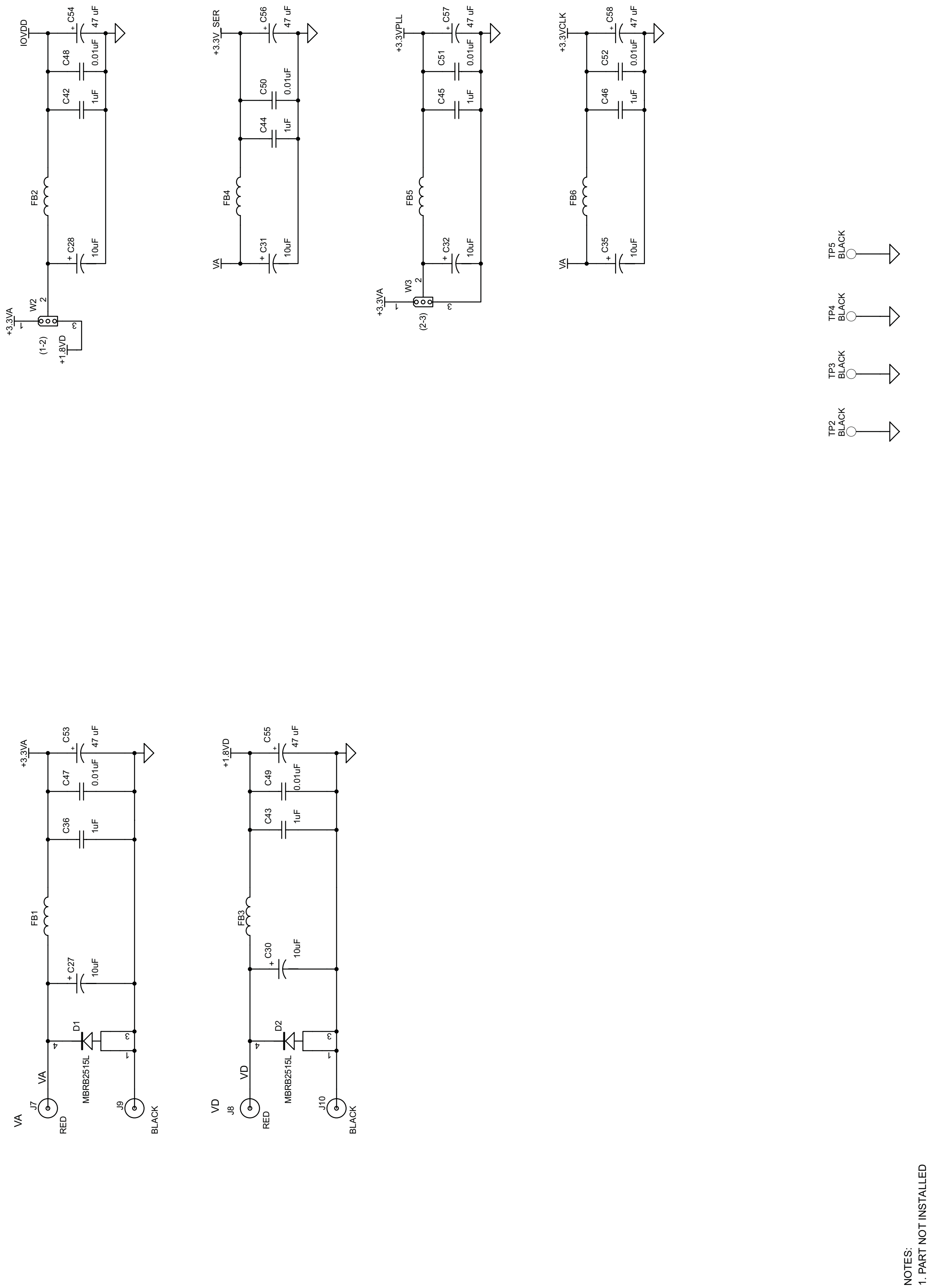

Figure 13. Schematic - Page 5

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.8 V to 3.3 V and the output voltage range of 3.3 V max.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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