High Voltage Very low current consumption Io=100mA Regulator

■GENERAL DESCRIPTION

The NJW4181 is a high input voltage and low current consumption 100mA series regulator low current consumption Iq=9μA and small package.

It has two package lineup. SOT-89 is able to direct replace to 3-terminal 78L series. ESON6, tiny DFN package, corresponds to a demand on miniaturization of sensor application and so on.

Due to the low current consumption of 9μA, the NJW4181 is suitable for light load and continuously running applications such as power management microprocessor, RTC, protection circuit, security system and so on.

■ PACKAGE OUTLINE

NJW4181KG1

NJW4181U3

■FEATURES

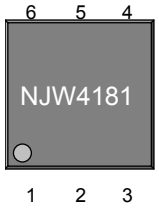
- Wide Operating Voltage Range — 35V (max.)
- Low Current Consumption — 9μA (typ.)
- Correspond to Low ESR capacitor (MLCC)
- Output Current — I_O(min.)=100mA
- High Precision Output — V_O ±1.0%
- Internal Thermal Overload Protection
- Internal Over Current Protection
- Internal Reverse Current Protection
- Package Outline — DFN6-G1(ESON6-G1), SOT-89-3

■ PRODUCT CLASSIFICATION

Device Name	Version	ON/OFF Function	Package	Status
NJW4181KG1-xxA	A	Yes	DFN6-G1(ESON6-G1)	PLAN
NJW4181U2-xxA	A	Yes	SOT-89-5	PLAN
NJW4181KG1-xxB	B	-	DFN6-G1(ESON6-G1)	
NJW4181U3-xxB	B	-	SOT-89-3	

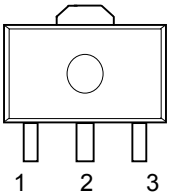
xx=Output Voltage ex) 33=3.3V 05=5.0V

■PIN CONFIGURATION



1. N.C.
2. GND
3. N.C.
4. V_{IN}
5. N.C.
6. V_{OUT}

NJW4181KG1



1. V_{OUT}
2. GND
3. V_{IN}

NJW4181U3

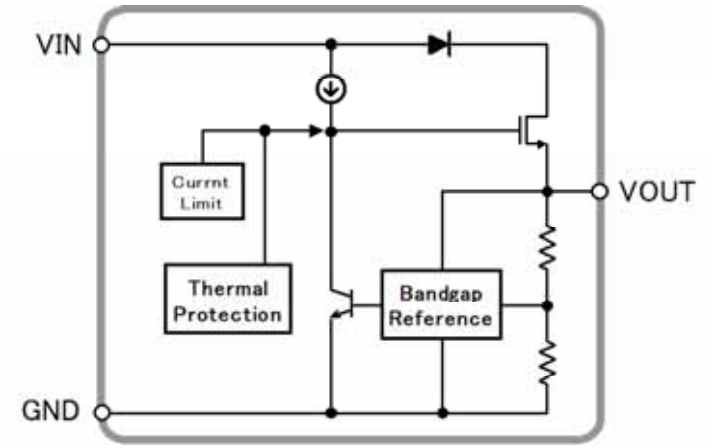
■ INPUT VOLTAGE RANGE

$V_O \leq 3V$: V_{IN} = +4.7V to +35V

$3V < V_O \leq 5V$: $V_{IN} = V_O$+1.7V to +35V

$V_O > 5V$: $V_{IN} = V_O$+2.0V to +35V

■BLOCK DIAGRAM



■OUTPUT VOLTAGE RANK LIST

DFN6-G1(ESON6-G1) SOT-89-3

Device Name	V_{OUT}	Device Name	V_{OUT}
NJW4181KG1-25B	2.5V	NJW4181U3-25B	2.5V
NJW4181KG1-33B	3.3V	NJW4181U3-33B	3.3V
NJW4181KG1-05B	5.0V	NJW4181U3-05B	5.0V
NJW4181KG1-08B	8.0V	NJW4181U3-08B	8.0V
NJW4181KG1-15B	15.0V	NJW4181U3-12B	12.0V
		NJW4181U3-15B	15.0V

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	RATINGS		UNIT
Input Voltage	V_{IN}	-0.3 to +40		V
Output Voltage	V_{OUT}	-0.3 ~ V_{IN}+7 ≤ 17 (Vo≤5.0V) -0.3 ~ +17 (Vo>5.0V)		V
Power Dissipation	P_D	DFN6-G1 (ESON6-G1)	420 (*1)	mW
			1200 (*2)	
		SOT-89-3	625 (*3)	
			2400 (*4)	
Junction Temperature	Tj	-40 to +150		°C
Operating Temperature	Topr	-40 to +85		°C
Storage Temperature	Tstg	-40 to +150		°C

(*1): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(*2): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm^2)

(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)
(4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ ELECTRICAL CHARACTERISTICS

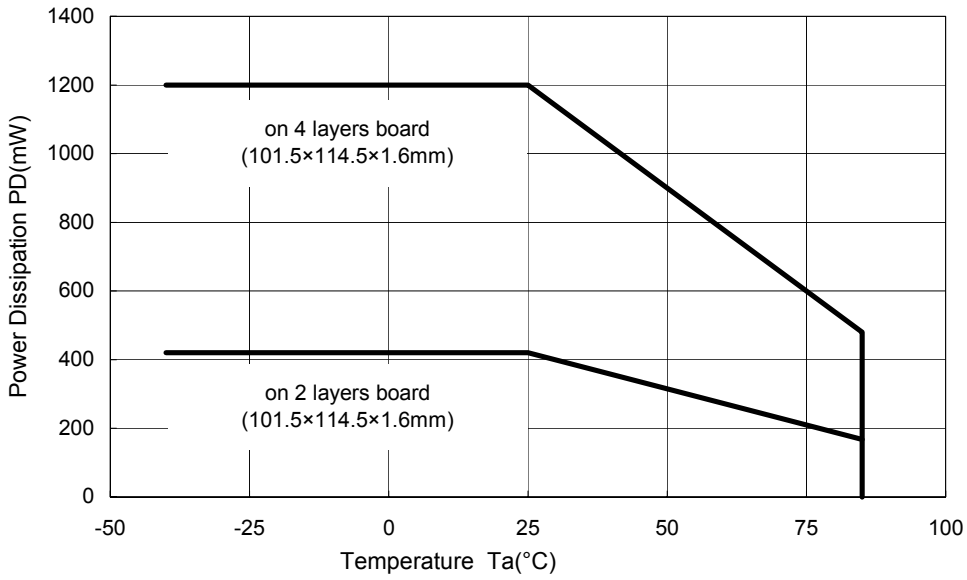
(Unless otherwise specified, V_{IN}=Vo+2.3V(3V<V_O≤5V: V_{IN} = Vo+2.0V, V_O≤3V: V_{IN} = 5.0V)
C_{IN} = 0.1 µF, C_O = 2.2µF, Ta= 25°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	I_O=30mA	-1.0%	-	+1.0%	V
Quiescent Current	I_Q	I_O=0mA	-	9	20	µA
Output Current	Io	$V_O \times 0.9$	100	-	-	mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_O≤3V: V_{IN} = +5.0V to +35V 3V<V_O≤5V: V_{IN} = V_O+2.0V to +35V V_O>5V: V_{IN} = V_O+2.3V to +35V, Io=30mA	-	-	0.05	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_O=0mA to 100mA	-	-	0.005	%/mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta Ta$	Ta=0 to 85°C, I_O=10mA	-	± 100	-	ppm/°C
Sink Current under Reverse Current Protection operating	$I_{REVERSE}$	V_{IN} =0V,Vo=5V(V_O≦5.0V)	-	0	1	µA
		V_{IN} =0V,Vo=15V(V_O>5.0V)		100	200	
Input Voltage	V_{IN}	V_O≤3V	4.7	-	35	V
		3V<V_O≤5V	V_O+1.7	-	35	
		V_O>5V	V_O+2.0	-	35	

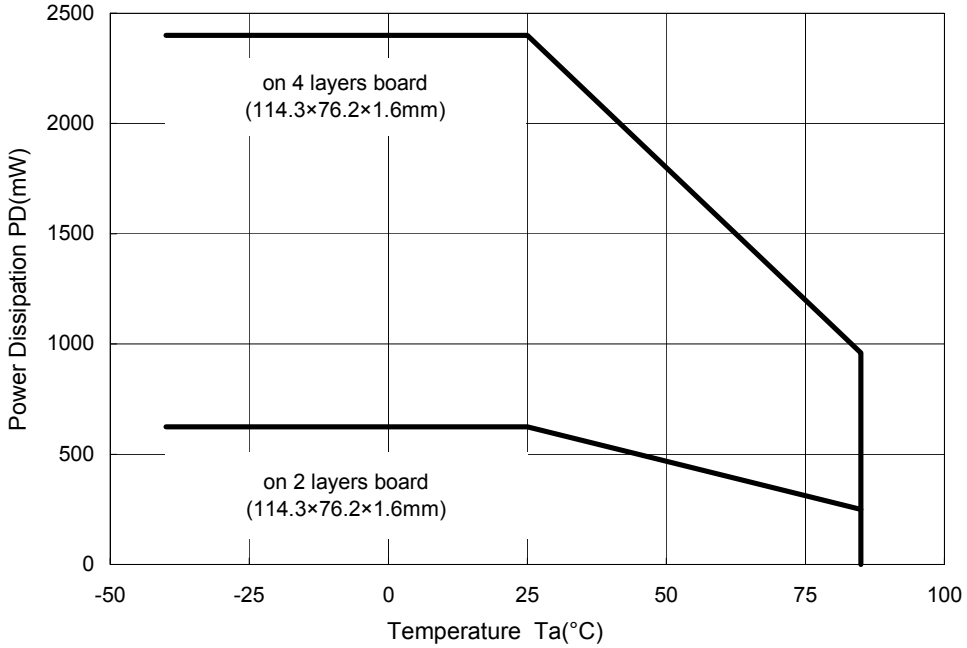
The above specification is a common specification for all output voltages.
Therefore, it may be different from the individual specification for a specific output voltage.

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

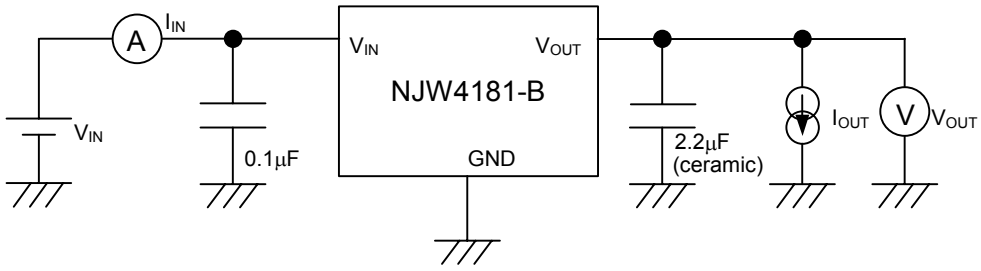
NJW4181KG1 Power Dissipation
(Topr=-40~+85°C,Tj=150°C)



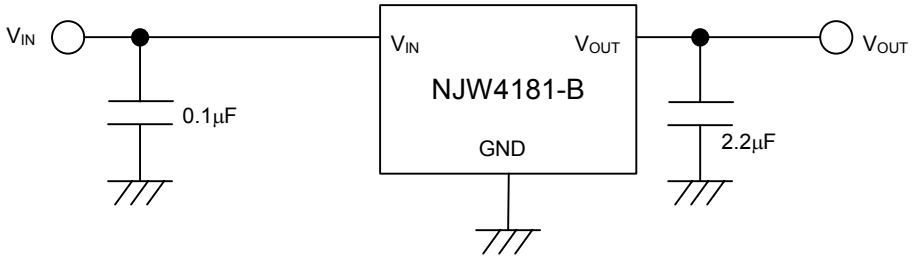
NJW4181U3 Power Dissipation
(Topr=-40~+85°C,Tj=150°C)



■ TEST CIRCUIT



■ TYPICAL APPLICATION



*Input Capacitor C_{IN}

Input Capacitor C_{IN} is required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and the V_{IN} pin as shortest path as possible to avoid the problem.

*Output Capacitor C_O

Output capacitor (C_O) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

On the other hand, Use of a larger C_O reduces output noise and ripple output, and also improves output transient response when rapid load change.

Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and the V_{OUT} pin as shortest path as possible for stable operation

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O, recommend that have withstand voltage margin against output voltage and superior temperature characteristic.

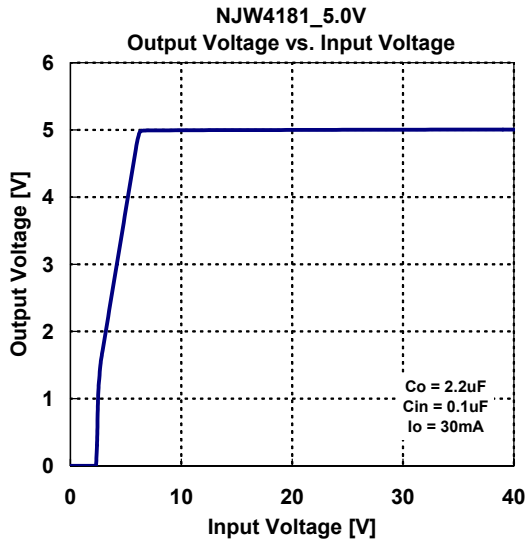
*Reverse Current Protection

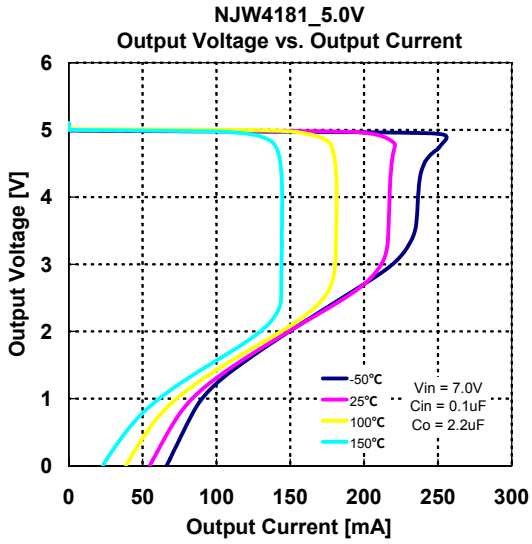
NJW4181 is built-in a Reverse Current Protection. This circuit restrains reverse current from the V_O pin to the V_{IN} pin when the input voltage is less than the output voltage.

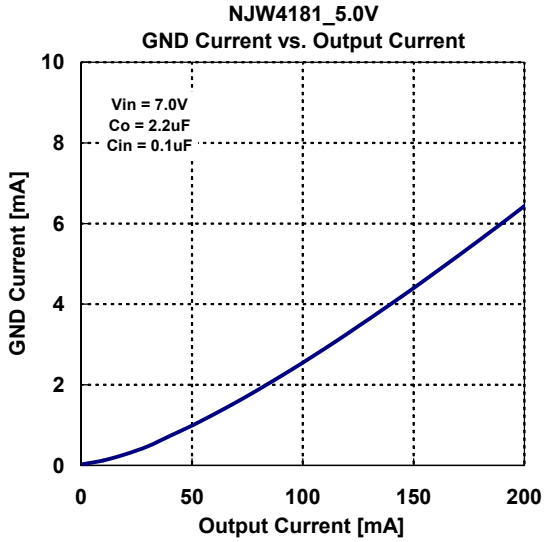
In case of the voltage rank 5.0V or below, reverse voltage differential between output and input should keep V_{IN}+7V or less, to prevent IC breaking due to huge reverse current.

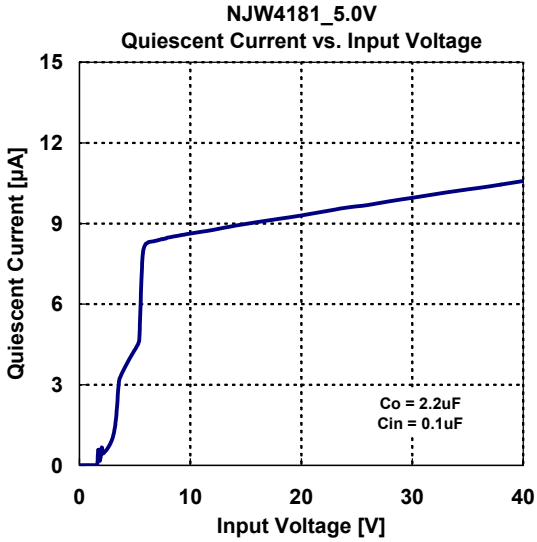
And also, the absolute maximum ratings of the Vo pin (17V) should not be exceeded.

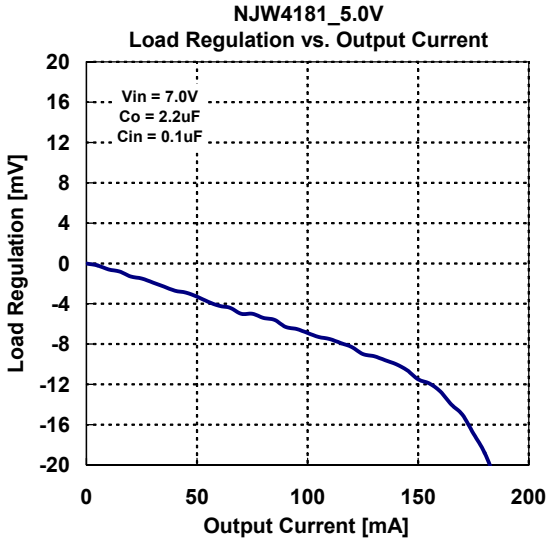
■ NJW4181-05 TYPICAL CHARACTERISTICS

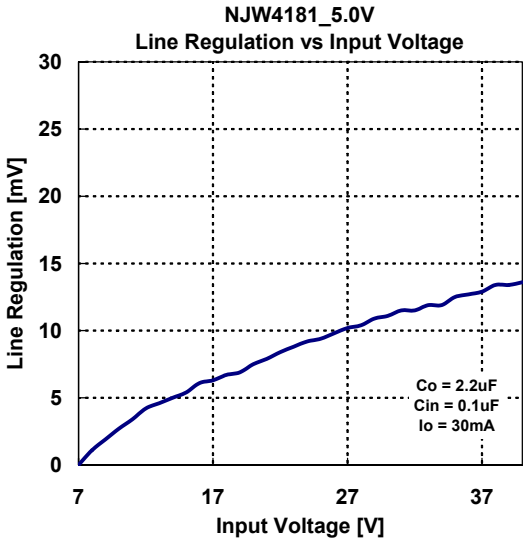




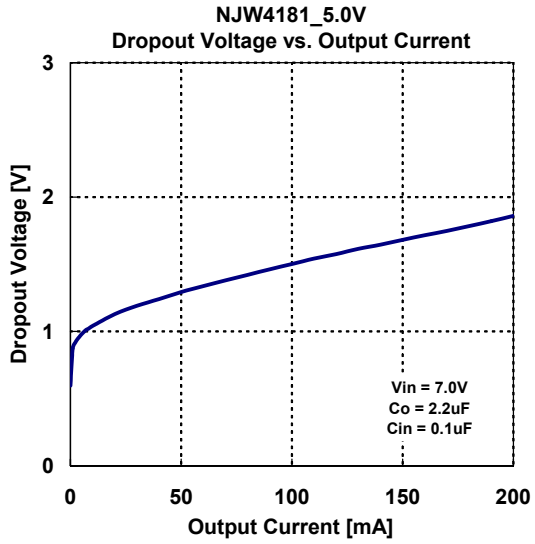


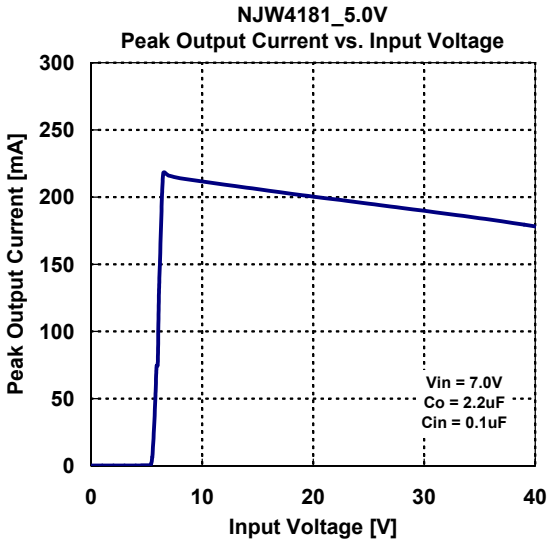


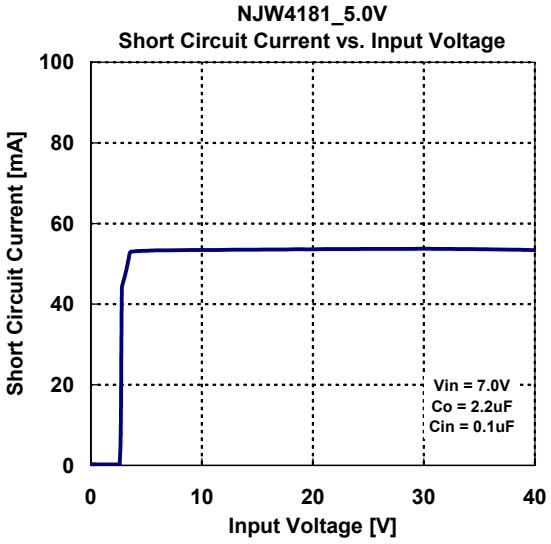


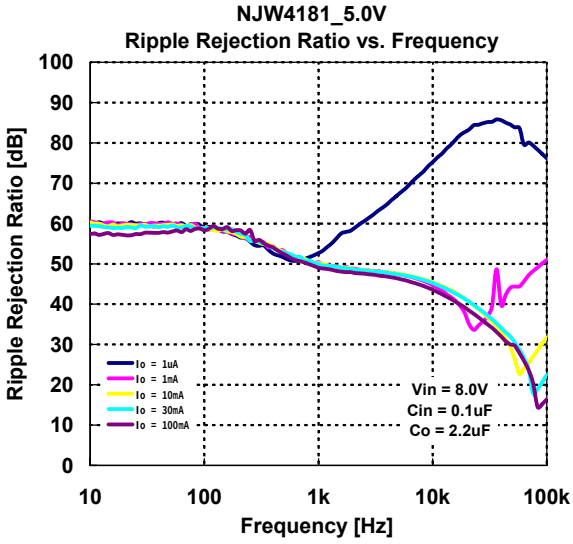


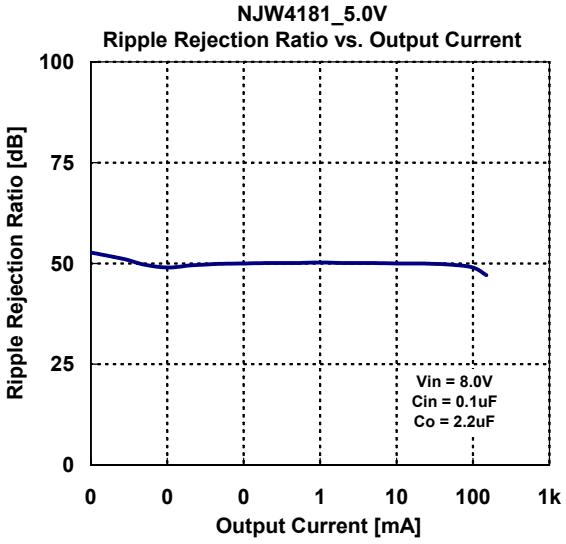
■ NJW4181-05 TYPICAL CHARACTERISTICS

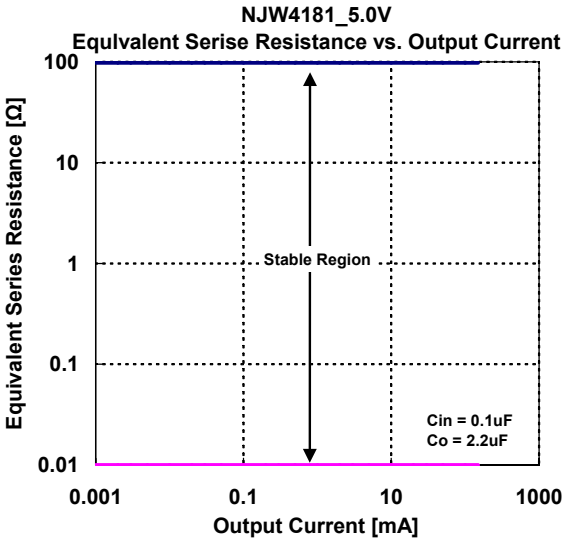




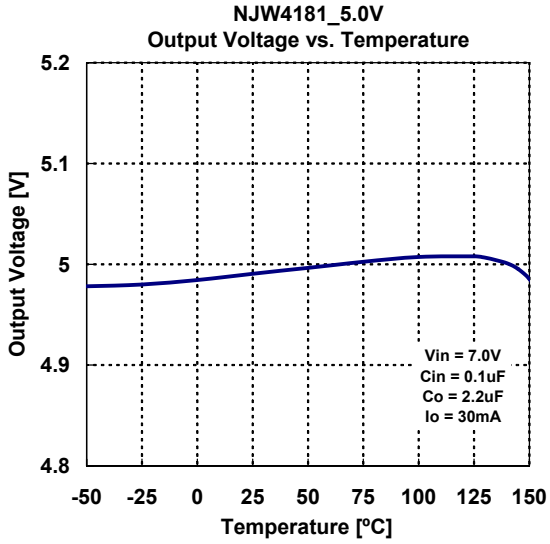


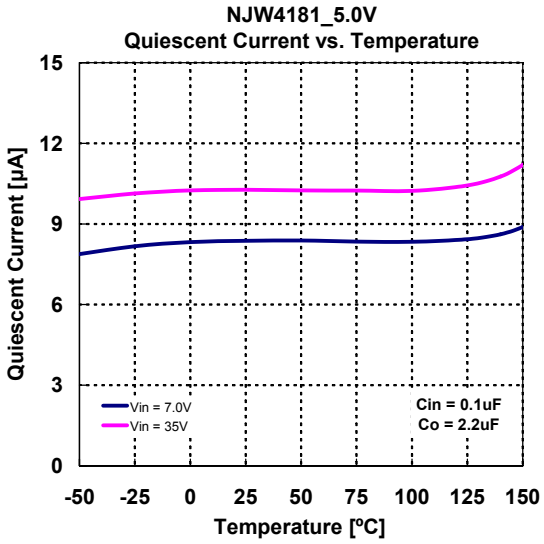


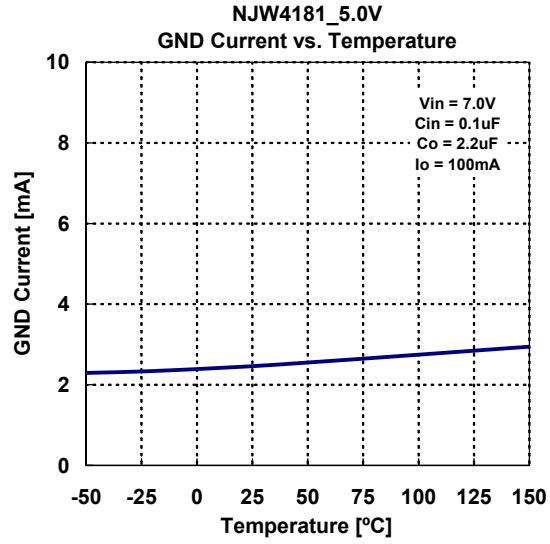


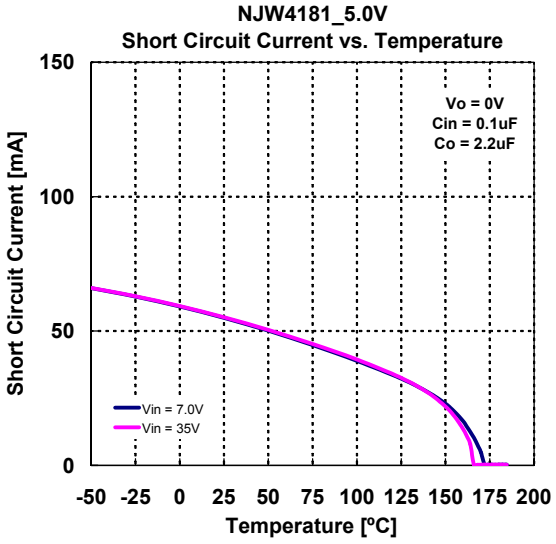


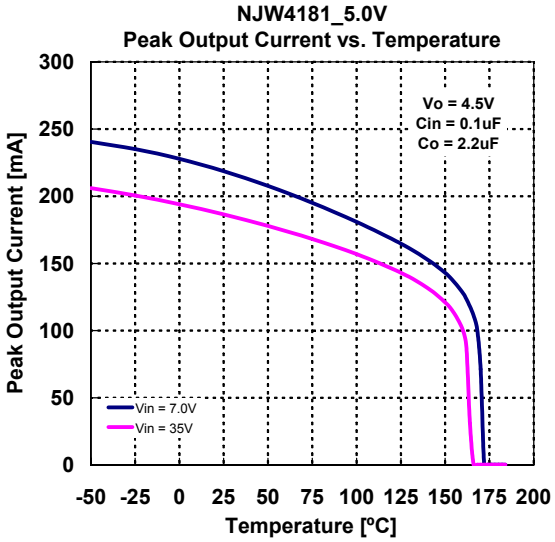
■ NJW4181-05 TYPICAL CHARACTERISTICS

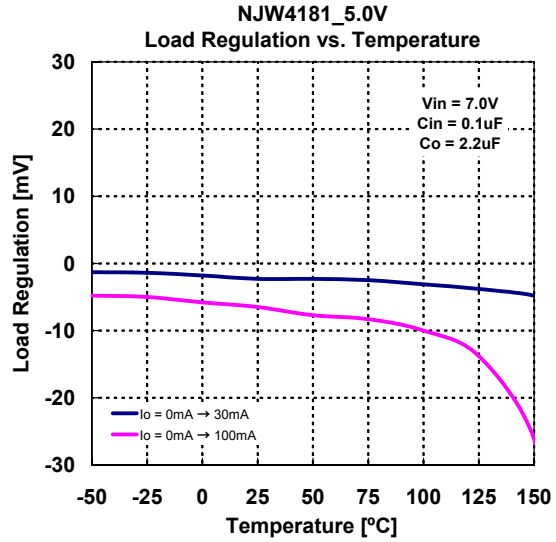






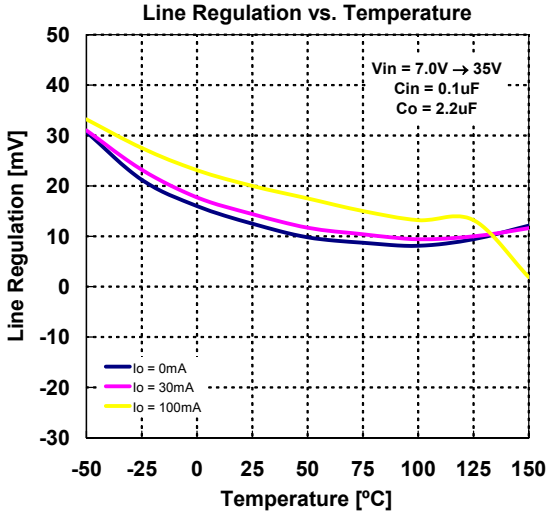




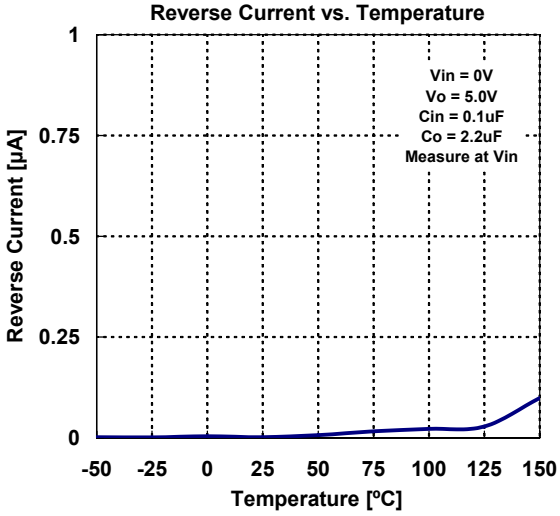


■ NJW4181-05 TYPICAL CHARACTERISTICS

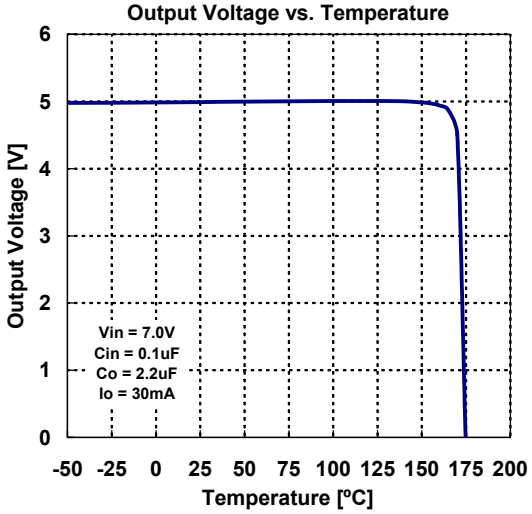
NJW4181_5.0V
Line Regulation vs. Temperature



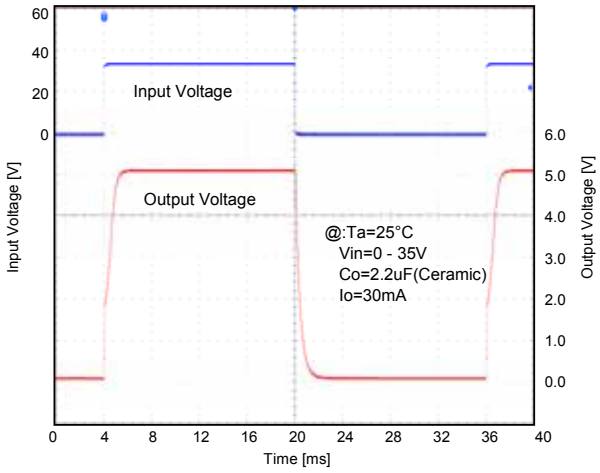
NJW4181_5.0V
Reverse Current vs. Temperature



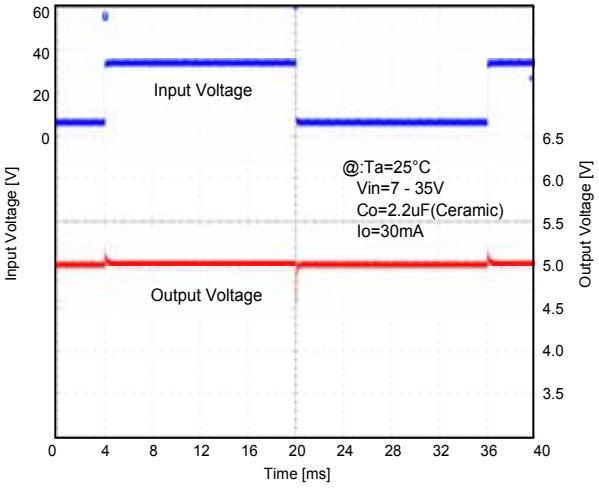
NJW4181_5.0V
Output Voltage vs. Temperature



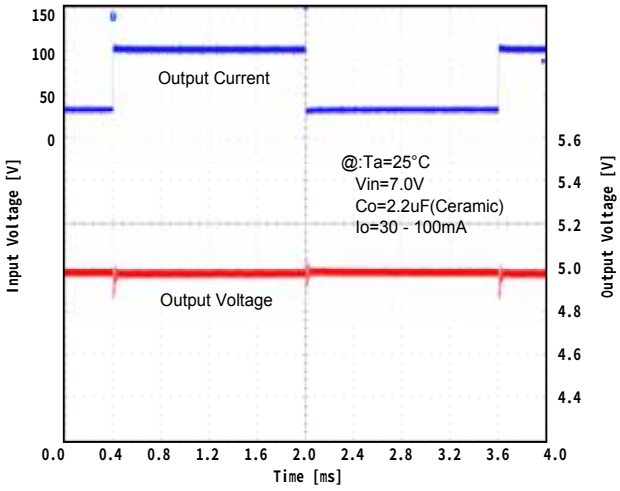
NJW4181_5.0V
Input Transient Response



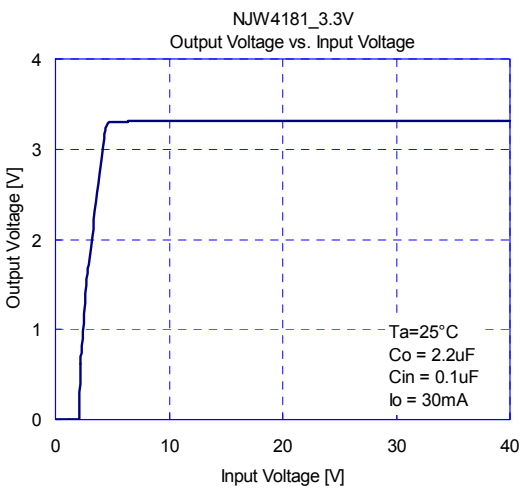
NJW4181_5.0V
Input Transient Response

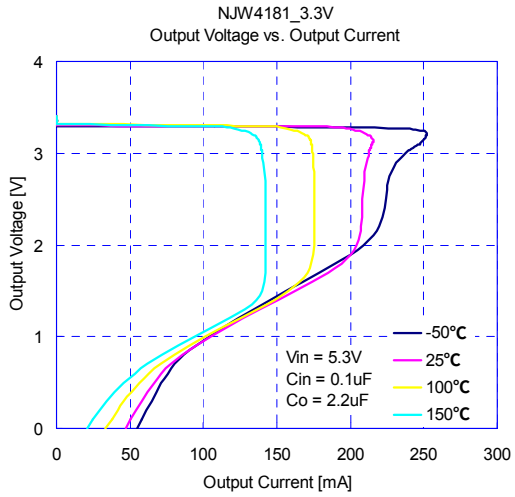


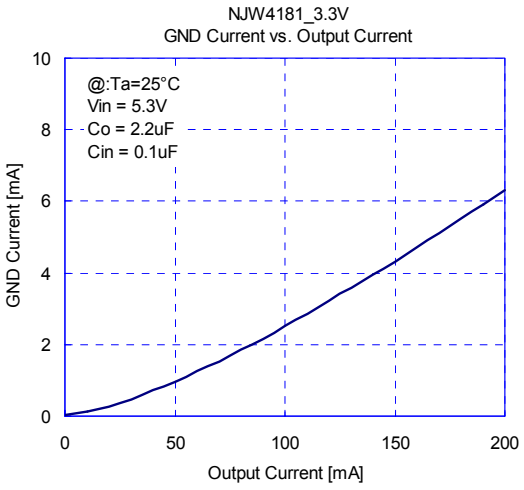
NJW4181_5.0V
Load Transient Response

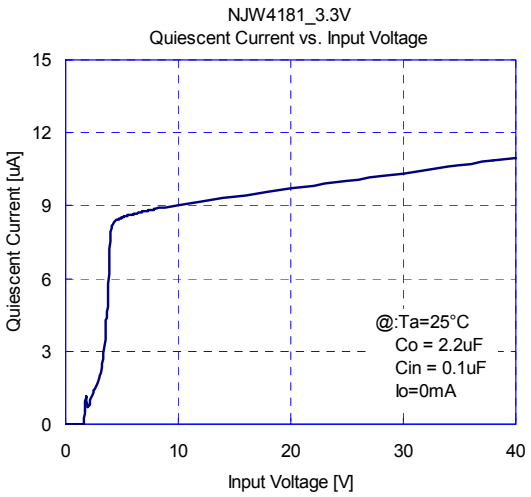


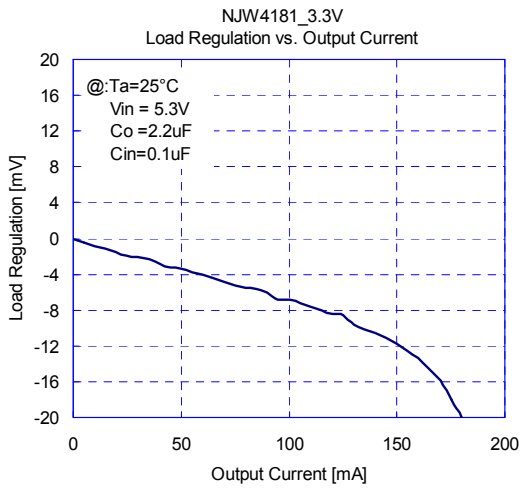
■NJW4181-33 TYPICAL CHARACTERISTICS

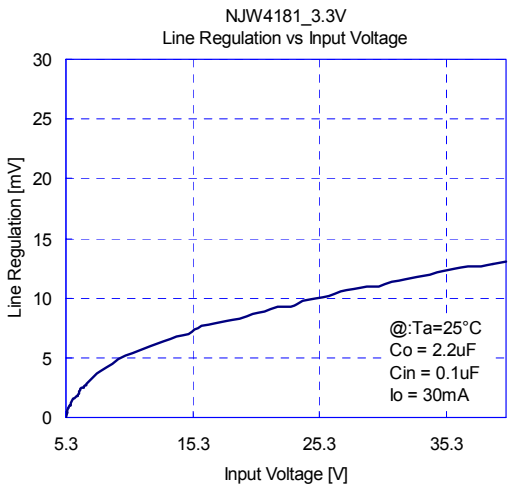






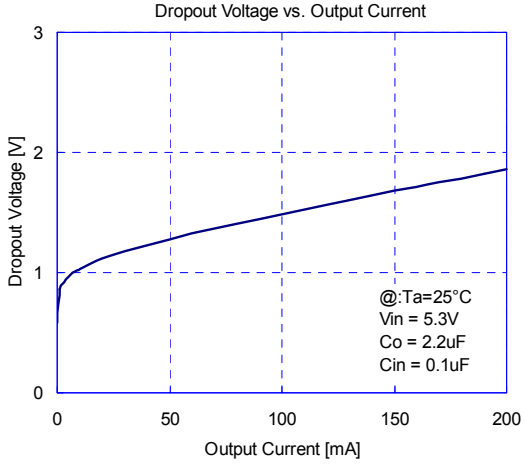




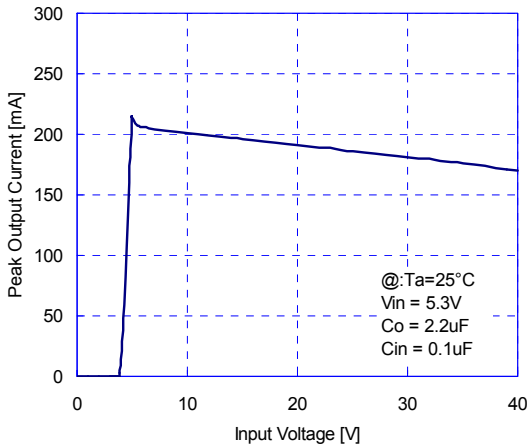


■NJW4181-33 TYPICAL CHARACTERISTICS

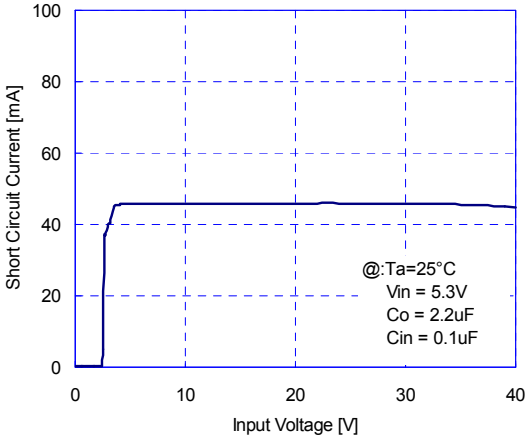
NJW4181_3.3V
Dropout Voltage vs. Output Current



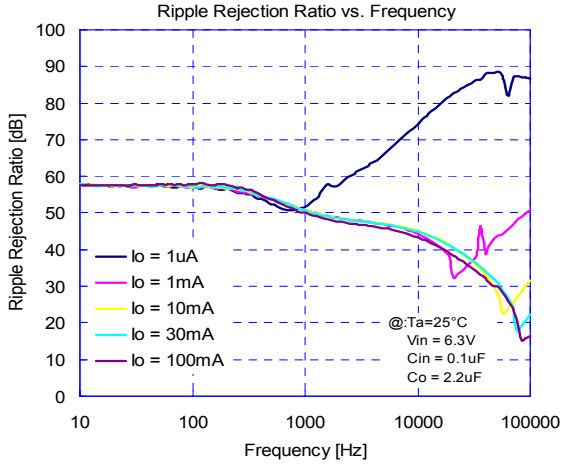
NJW4181_3.3V
Peak Output Current vs. Input Voltage



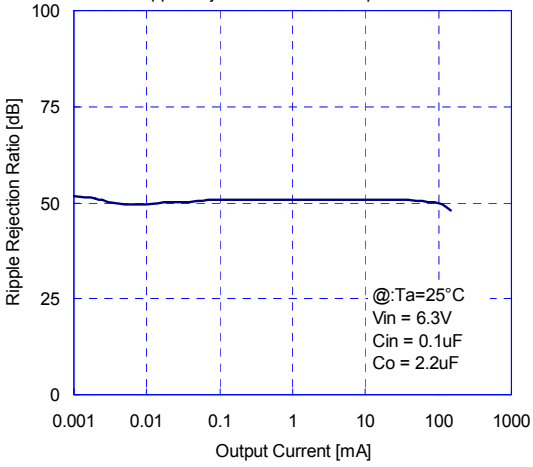
NJW4181_3.3V
Short Circuit Current vs. Input Voltage



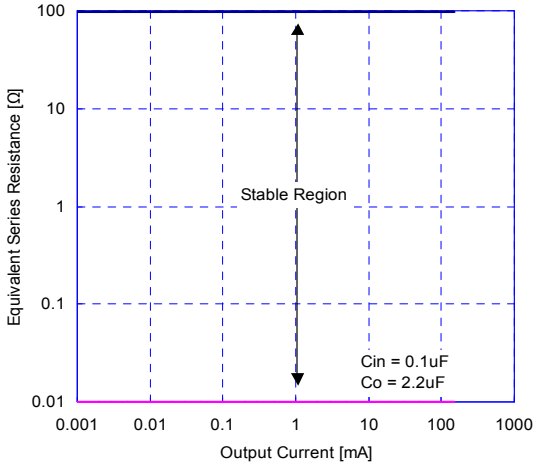
NJW4181_3.3V
Ripple Rejection Ratio vs. Frequency



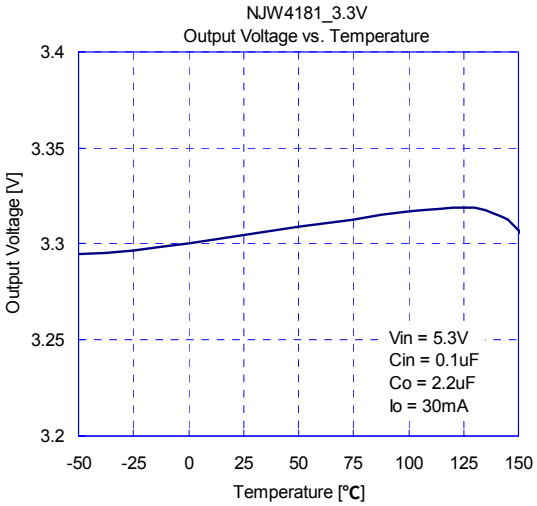
NJW4181_3.3V
Ripple Rejection Ratio vs. Output Current

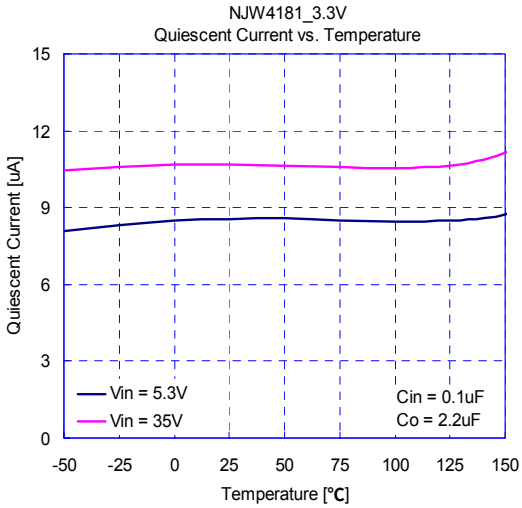


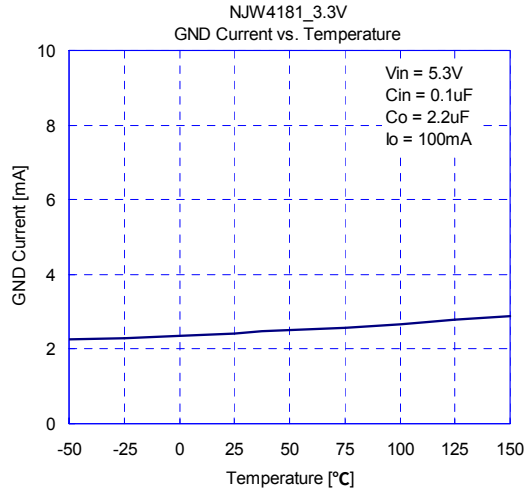
NJW4181_3.3V
Equlvalent Serise Resistance vs. Output Current

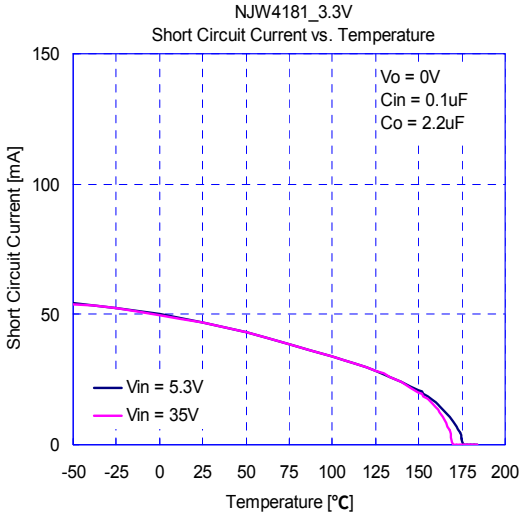


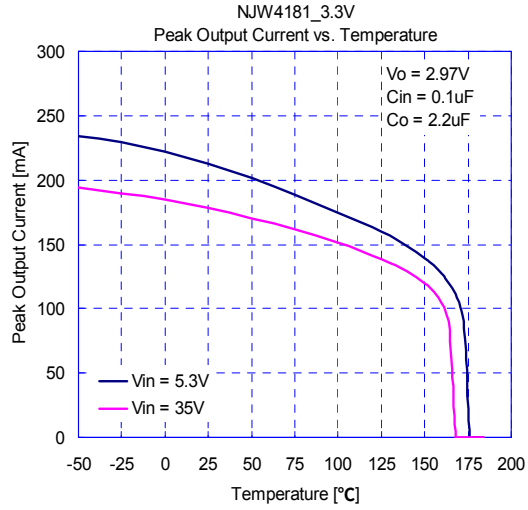
■NJW4181-33 TYPICAL CHARACTERISTICS

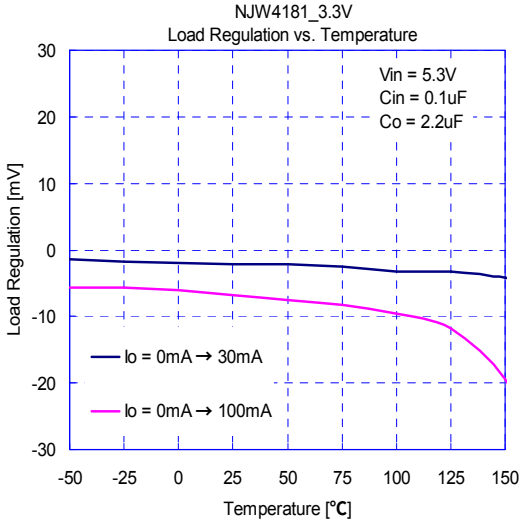












■NJW4181-33 TYPICAL CHARACTERISTICS