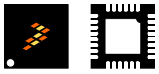
Freescale Semiconductor, Inc.
Data Sheet: Technical Data

Document Number: WPR1516
Rev 2, 1/2015

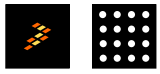
MWPR1516 16 KB Flash

24 MHz Cortex-M0+ Based Microcontroller

MWPR1516CFM(R)
MWPR1516CALR



32-pin QFN (FM)
5 x 5 x 0.58 Pitch 0.5 mm



36-pin WLCSP (AL)
3.1 x 3.0 x 0.6 Pitch 0.4 mm

Higher integration receiver controller MCU for wireless power transfer application. Targeting battery powered products are smart phone, tablet, portable medical devices, power tools etc.

This product offers:

- AC/DC conversion and modulation/demodulation circuit for bi-directional communication to support industrial standards with foreign object detection (FOD)
- USB/adapter power switcher to charge products with wire and wireless with priority.
- Up to 15 W with proper external transistors
- QFN package for industrial application and WLCSP package for space constrained consumer applications

Performance

- 24 MHz ARM® Cortex®-M0+ core
- Single cycle 32-bit x 32-bit multiplier

Memories and memory interfaces

- 16 KB program flash memory
- 4 KB SRAM

System peripherals

- LDO provides 5 V and 3 A output to down system
- CNC controls the communication and provides AC protection
- High voltage input PMC module with three power modes: Run, Wait, Stop
- LVR with reset or interrupt, selectable trip points
- WDOG with independent clock source
- Serial wire debug interface

Clocks

- 32.768 kHz or 4 MHz to 24 MHz crystal oscillator
- Internal 20 kHz low-power oscillator (LPO)
- Internal clock source (ICS)
- Internal FLL with internal or external reference, precision trimming

Operating Characteristics

- Input from rectifier voltage range: 3.5 to 20 V
- Temperature range (ambient): -40 to 85°C

Human-machine interface

- One interrupt module (IRQ)
- Up to 13 general-purpose input/output (GPIO)

Communication interfaces

- One UART module
- One I2C module

Analog Modules

- One 12-bit analog-to-digital converters (ADC) with up to 4 external channels
- One programmable gain amplifier (PGA) with differential input and output
- One analog comparator (ACMP) containing a 6-bit DAC and programmable reference input

Timers

- Two 2-channel FTMs with basic TPM function
- One periodic interrupt timers (PIT)
- One FSK demodulation timer (FSKDT)
- System tick timer (SysTick)
- One real time clock (RTC)

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information

Part Number[1]	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MWPR1516CFM(R)	16	4	13
MWPR1516CALR	16	4	13

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	WPR1516PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	WPR1516RM[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	WPR1516_0N49M[1]
Package drawing	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00615D[1] WLCSP 36-pin: 98ASA00789D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

Figure 1 shows the functional modules in the chip.

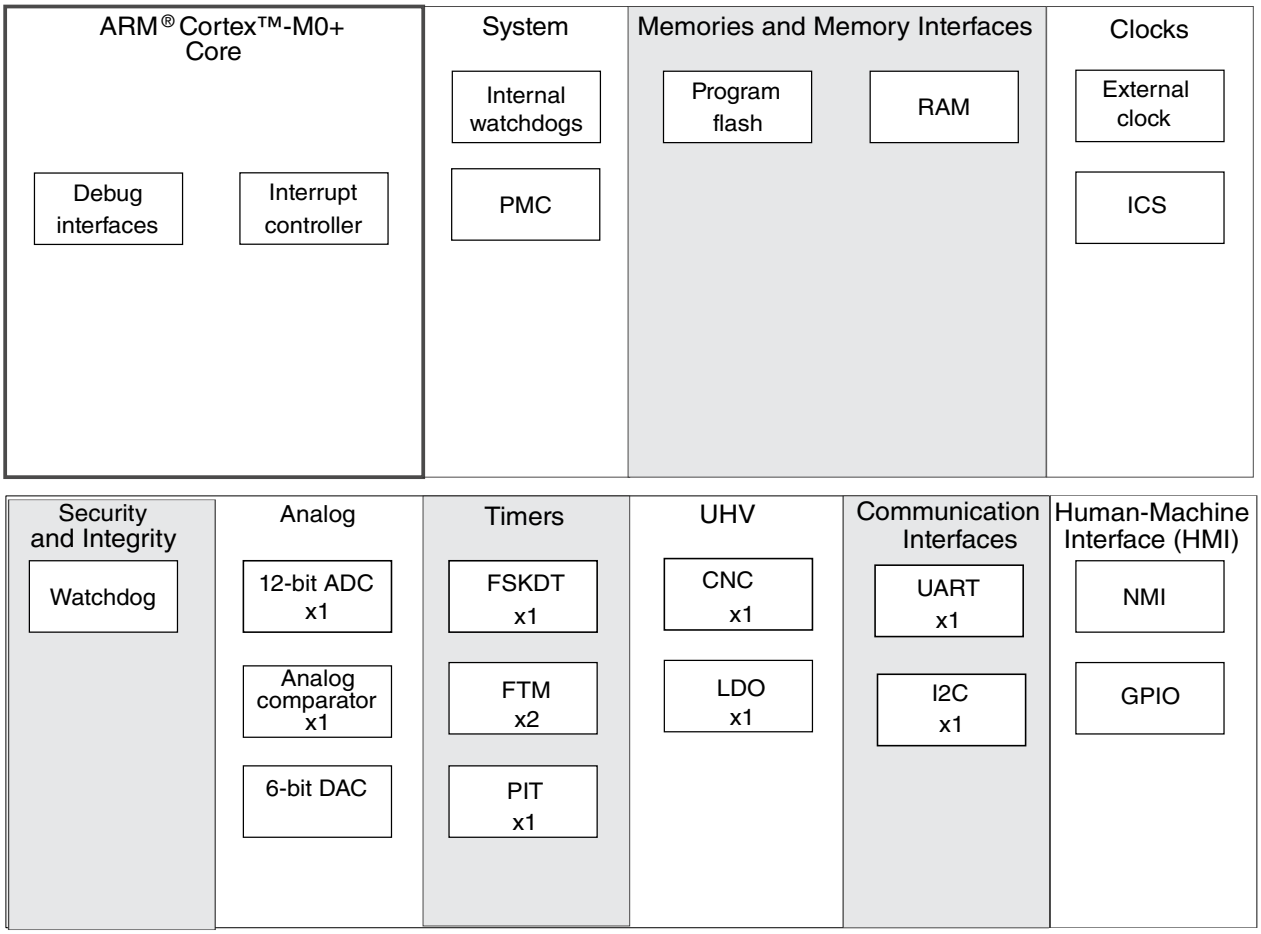


Figure 1. Functional block diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description[1]	Min	Typ.	Max	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	—	+2000	V	2
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	—	+500	V	3
I_{LAT}	Latch-up current at ambient temperature of 85 °C	-100	—	+100	mA	4

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions, unless otherwise noted.
2. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
3. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
4. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 1. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{REC}	Supply voltage from wireless receiver rectifier	0	20	V
$V_{AC1/AC2}$	AC voltage input from wireless receiver coil	-0.3	21	V
I_{VREC}	Maximum current into V_{REC}	0	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET\_b}}$, EXTAL, and XTAL)	-0.3	V_{DD}+0.3	V
V_{AD_IN}	Wired power input voltage	0	12	
V_{AIO}	• Analog[1], $\overline{\text{RESET}}$, VOUT_FB, EXTAL, and XTAL input voltage • VOUT and ISENS input voltage	-0.3 -0.3	V_{DD}+0.3 5.5	
I_D	Instantaneous maximum current single pin limit • for GPIO pins • for other pins except power pins	-25 -10	25 10	mA

1. Analog pins are defined as pins that do not have an associated general-purpose I/O port function.

2 General

2.1 Nonswitching electrical specifications

2.1.1 DC electrical characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	Descriptions			Min.	Typical[1]	Max.	Unit
—	Operating voltage		—	3.13	—	5.5	V
V_{OH}	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} – 0.8	—	—	V
I_{OHT}	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
V_{OL}	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
I_{OLT}	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
V_{IH}	Input high voltage	All digital inputs	V_{DD} > 4.5 V	0.70 × V_{DD}	—	—	V
V_{IH}	Input high voltage	All digital inputs	3.13 V <V_{DD} ≤ 4.5 V	0.75 × V_{DD}	—	—	V
V_{IL}	Input low voltage	All digital inputs	3.13 V <V_{DD} ≤ 4.5 V	—	—	0.30 × V_{DD}	V
V_{IL}	Input low voltage	All digital inputs	V_{DD} > 3.3 V	—	—	0.35 × V_{DD}	V
V_{hys}	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In}\rvert$	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ}\rvert$	Hi-Z (off-state) leakage current	All input / output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT}\rvert$	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	Descriptions			Min.	Typical[1]	Max.	Unit
R_{PU}	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA6 or PTA7	—	30.0	—	50.0	kΩ
R_{PU}[2]	Pullup resistors	PTA6 and PTA7	—	30.0	—	60.0	kΩ
I_{IC}	DC injection current[3, 4, 5, 6]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
		Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
3. This item applies to the GPIO share pads only.
4. All functional non-supply pins, except for PTA6 and PTA7, are internally clamped to V_{DD}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. Power supply electrical characteristics

Symbol	Description		Min.	Typical [1]	Max.	Unit
$V_{DD1.8}$	Output voltage core	Full performance mode	1.72	1.83	1.98	V
		Reduced power mode[2]	—	1.6	—	V
V_{DDF}	Output Voltage Flash	Full performance mode	2.6	2.81	2.9	V
		Reduced power mode[2]	—	1.69	—	V
V_{DD}[3]	Output voltage V_{DD}	Full performance mode 3.5 V≤V_{REC}<4.5 V	3.13	—	4.5	V
		Full performance mode 4.5 V≤ V_{REC}<5.3 V	4.19	—	5.25	V
		Full performance mode V_{REC}≥5.3 V	4.75	4.99	5.25	V
		Reduced power mode[2]	2.5	—	5.75	V
I_{DD}	Load current V_{DD}	Full performance mode 3.5 V ≤ V_{REC}<4.5 V	0	—	28	mA
		Full performance mode 4.5V ≤ V_{REC}<5.3 V	0	—	28	mA
		Full performance mode V_{REC}≥5.3 V	0	—	50	mA
		Reduced power mode[2]	0	—	5	mA
V_{REFH}	Output voltage V_{REFH}	4.1 V≤V_{REC}<4.5 V	3.781	3.8	3.819	V
		4.5 V≤V_{REC}<4.9 V	3.781/ 4.179	3.8/ 4.2[4]	3.819/ 4.221	V

Table continues on the next page...

Table 3. Power supply electrical characteristics (continued)

Symbol	Description		Min.	Typical [1]	Max.	Unit
		V_{REC} ≥ 4.9 V	3.781/ 4.179/ 4.577	3.8/ 4.2/ 4.6[4]	3.819/ 4.221/ 4.623	V
—	V_{REFH} accuracy	V_{REC}≥V_{REFH} + 0.3, 0—70 °C	—	—	0.5	%
		V_{REC}≥V_{REFH} + 0.3, -40—85 °C	—	—	0.8	%
I_{REFH}	Output current V_{REFH}	V_{REC}≥V_{REFH} + 0.3	0	—	5	mA
V_{LVWA}	V_{DD} Low voltage warning assert level	PMC_LVCTLSTAT1[SLVWSEL] = 0b	3.43	3.63	3.83	V
		PMC_LVCTLSTAT1[SLVWSEL] = 1b	3.94	4.14	4.34	
V_{LVWD}	V_{DD} Low voltage warning deassert level	PMC_LVCTLSTAT1[SLVWSEL] = 0b	3.54	3.74	3.94	V
		PMC_LVCTLSTAT1[SLVWSEL] = 1b	4.08	4.28	4.48	
V_{LVRA}	V_{DD} low voltage reset assert		2.97	3.02	—	V
V_{LVRD}	V_{DD} low voltage reset deassertl		—	—	3.13	V
$V_{LVWREFHA}$	Low voltage warning for V_{REFH} assert level	PMC_VREFHLVW[LVWCFG]=00b	3.34	3.54	3.74	V
		PMC_VREFHLVW[LVWCFG]=01b	3.43	3.63	3.83	V
		PMC_VREFHLVW[LVWCFG]=10b	3.86	4.06	4.26	V
		PMC_VREFHLVW[LVWCFG]=11b	4.11	4.31	4.51	V
$V_{LVWREFHA}$	Low voltage warning for V_{REFH} deassert level	PMC_VREFHLVW[LVWCFG]=00b	3.45	3.65	3.85	V
		PMC_VREFHLVW[LVWCFG]=01b	3.55	3.75	3.95	V
		PMC_VREFHLVW[LVWCFG]=10b	4.00	4.20	4.40	V
		PMC_VREFHLVW[LVWCFG]=11b	4.27	4.47	4.67	V
$V_{LVR1.8A}$	Low voltage reset for $V_{DD1.8}$ assert level		1.49	1.69	1.89	V
$V_{LVR1.8D}$	Low voltage reset for $V_{DD1.8}$ deassert level		1.56	1.76	1.96	V
$V_{LVRDDFA}$	Low voltage reset for V_{DDF} assert level		2.44	2.64	2.84	V
$V_{LVRDDFD}$	Low voltage reset for V_{DDF} deassert level		2.52	2.72	2.92	V
f_{LPOCLK}	Trimmed LPOCLK output frequency		—	20	—	kHz
df_{LPOCLK}	Trimmed LPOCLK internal clock Δf / $f_{NOMINAL}$[5]		-5	—	5	%
t_{SDEL}	LPOCLK start up delay		—	25	50	µs
dV_{HT}	Temperature sensor slope		—	5.07	—	mV/°C
V_{HT}	Temperature sensor output voltage		—	1.57	—	V
T_{HTIA}	High temperature interrupt assert[6]		95	110	125	°C
T_{HTID}	High temperature interrupt deassert[6]		85	100	115	°C
V_{BG}	Bandgap output voltage		1.13	1.2	1.32	V
V_{HCBG}	HC Bandgap output voltage		1.14	1.15	1.16	V
t_{STP_REC}	Recovery time from Stop	not including V_{REFH}	—	15	—	µs
		including V_{REFH}	—	1	—	ms

1. Typical values are measured at 25 °C.

2. Power supply enters reduced power mode when MCU is in Stop mode.
3. V_{DD} is from V_{DD1}.
4. This typical value is configurable based on V_{REC}.
5. User need to trim the LPOCLK in order to get ±5% LPOCLK
6. This is junction temperature.

NOTE

Unless noted, VDD1 and VDD2 must be shorted on the application board.

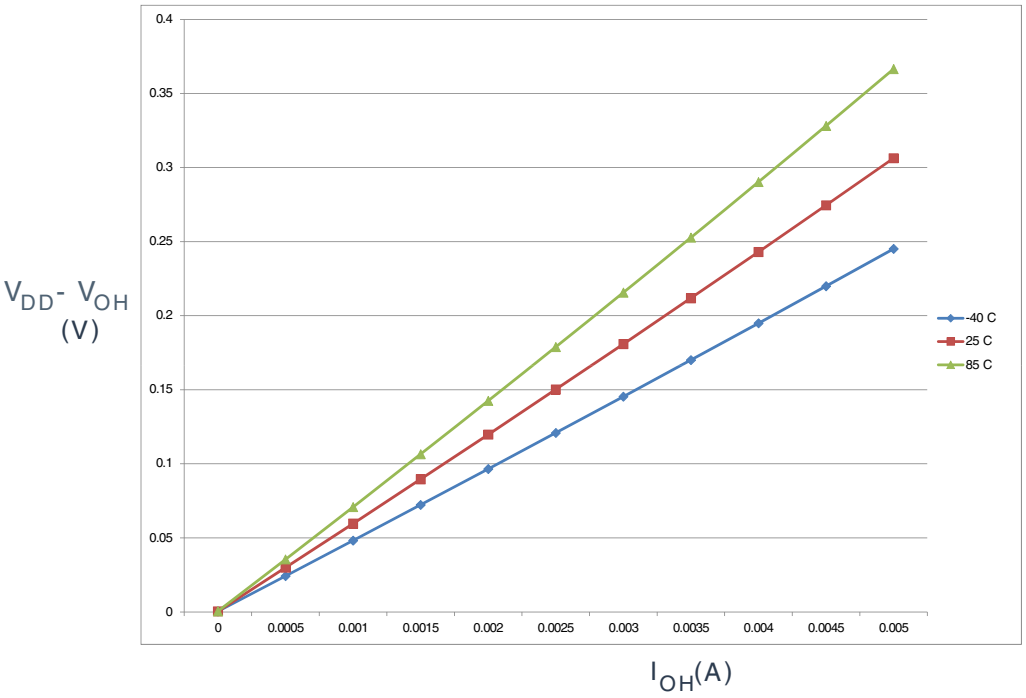


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

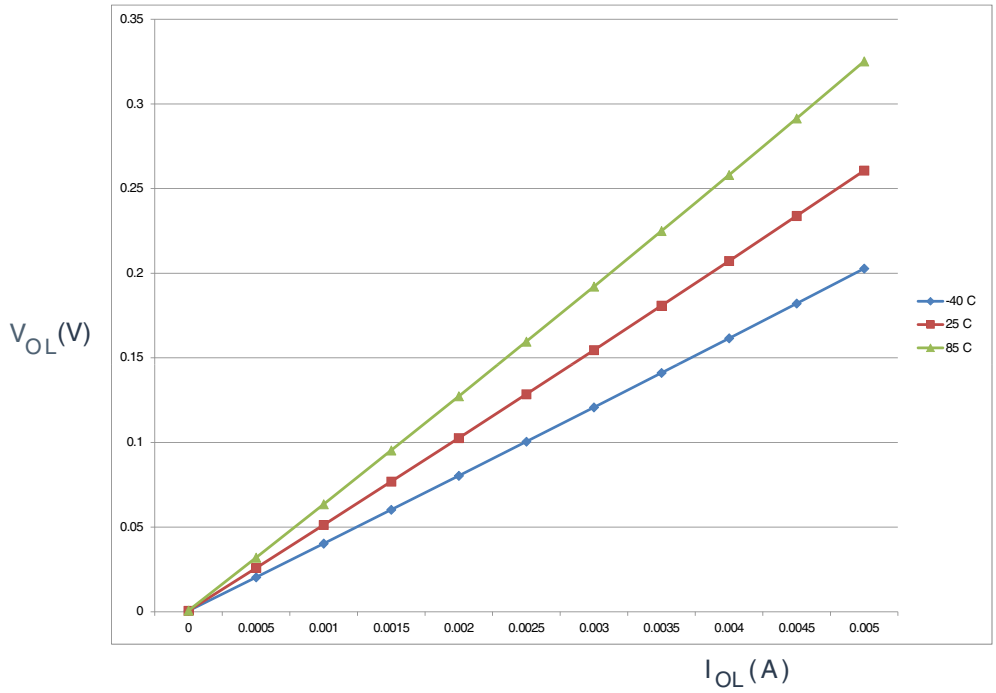


Figure 3. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

2.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics (at 5.5 V)

Parameter	Symbol	Bus Freq.	Typical[1]	Max.	Unit	Temp.
Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	24 MHz	13.17	—	mA	-40–85 °C
		12 MHz	9.37	—		
		6 MHz	7.49	—		
Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	24 MHz	11.17	—	mA	-40–85 °C
		12 MHz	8.37	—		
		6 MHz	6.99	—		
Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	24 MHz	14.01	17	mA	-40–85 °C
		12 MHz	8.65	—		
		6 MHz	6.60	—		
Run supply current FBE mode, all modules clocks disabled; run from RAM	RI_{DD}	24 MHz	10.61	13	mA	-40–85 °C
		12 MHz	7.65	—		
		6 MHz	6.09	—		
Wait mode current FBE mode, all modules clocks enabled	WI_{DD}	24 MHz	8.23	10	mA	-40–85 °C

Table continues on the next page...

Table 4. Supply current characteristics (at 5.5 V) (continued)

Parameter	Symbol	Bus Freq.	Typical[1]	Max.	Unit	Temp.
		12 MHz	6.52	—		
		6 MHz	5.53	—		
Stop mode supply current no clocks active (except CNC clock)	SI_{DD}	—	700	—	µA	-40–85 °C

1. Data in Typical column was characterized at 25 °C or is typical recommended value.

2.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

2.1.3.1 Radiated Emissions

Table 5. EMC radiated emissions operating behaviors for 32-pin QFN package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	4	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	6	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	16	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{RECT} = 5.0 V, T_A = 25 °C, f_{OSC} = 32.768 kHz (crystal), f_{SYS} = 24 MHz, f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2 Switching specifications

2.2.1 Control timing

Table 6. Control Timing

Rating		Symbol	Min.	Typical[1]	Max.	Unit
Bus frequency (t_{CYC} = 1 / f_{Bus})		f_{Bus}	DC	—	24	MHz
Internal low power oscillator frequency[2]		f_{LPO}	16	20	26	KHz
External reset pulse width		t_{EXTRST}	1.5 × t_{CYC}	—	—	ns
Reset low drive		t_{RSTDRV}	34 × t_{CYC}	—	—	ns
External NMI pin interrupt pulse width - Asynchronous path		t_{NMI}	100	—	—	ns
IRQ pulse width	Asynchronous path[3]	t_{ILIH}	100	—	—	ns
	Synchronous path	t_{IHIL}	1.5 × t_{CYC}	—	—	ns
Port rise and fall time - Normal drive strength (load = 50 pF)	—	t_{Rise}	—	10.2	—	ns
		t_{Fall}	—	9.5	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. It can be configured by PMC_RC20KTRM[OSCOT].
3. This is the shortest pulse that is guaranteed to be recognized as a IRQ pin request.

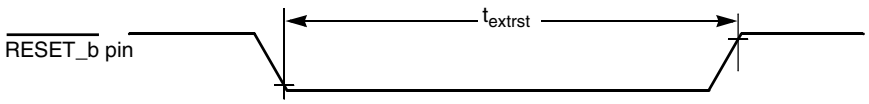


Figure 4. Reset Timing

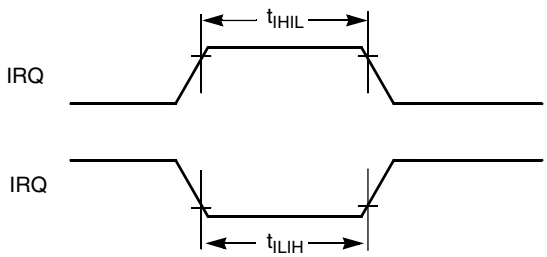


Figure 5. IRQ Timing

2.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized. These synchronizers operate from the timer clock.

Table 7. FTM Input Timing

Function	Symbol	Min.	Max.	Unit
Input capture pulse width	t_{ICPW}	1.5	—	t_{Timer} [1]

1. $t_{Timer} = 1/f_{Timer}$

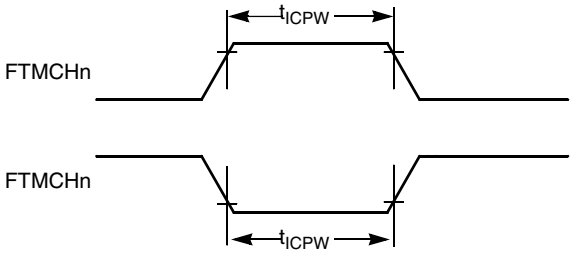


Figure 6. Timer Input Capture Pulse

2.3 Thermal specifications

2.3.1 Thermal operating requirements

Table 8. Thermal operating requirements of WLCSP package

Symbol	Description	Min.	Max	Unit	Notes
T_J	Die junction temperature	-40	95	°C	
T_A	Ambient temperature	-40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA} \times$ chip power dissipation.

Table 9. Thermal operating requirements of QFN package

Symbol	Description	Min.	Max	Unit	Notes
T_J	Die junction temperature	-40	105	°C	
T_A	Ambient temperature	-40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA} \times$ chip power dissipation.

2.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal Attributes

Board type	Symbol	Description	32 QFN	36 WLCSP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	97	129.8	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	33	71.4	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	81	116.5	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	27	68.0	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	48.6	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.3	8.1	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	—	14.3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C)$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$$

Where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

3 Peripheral operating requirements and behaviors

3.1 UHV modules

3.1.1 LDO electrical characteristics

This section provides data about the LDO module electrical characteristics.

Table 11. LDO electrical characteristics

Symbol	Description		Min.	Typical	Max.	Unit
V_{OUT} [1]	Regulated output voltage		4.2	5	5.2	V
V_{OUTA}	Output voltage accuracy		—	2[2]	—	%
V_{TH1}	Over voltage protection de-assert	LDO_CR[OVTHLD]=00b	—	4.27	—	V
		LDO_CR[OVTHLD]=01b		4.62		
		LDO_CR[OVTHLD]=10b		5.33		
		LDO_CR[OVTHLD]=11b		5.78		
V_{TH2}	Over voltage protection assert	LDO_CR[OVTHLD]=00b	—	4.8	—	V
		LDO_CR[OVTHLD]=01b		5.2		
		LDO_CR[OVTHLD]=10b		6.0		
		LDO_CR[OVTHLD]=11b		6.5		
I_{LIM}	Current limit threshold, with sample resistor:	33 mΩ	0.3	N x 1.4/(511 x 10 x Rsense)[3]	—	A
		100 mΩ	0.1			
I_{TH1}	Over current protection threshold	LDO_CR[OCTHLD]=000b	—	1.05/(10 x Rsense)	—	A
		LDO_CR[OCTHLD]=001b		1.10/(10 x Rsense)		
		LDO_CR[OCTHLD]=010b		1.15/(10 x Rsense)		
		LDO_CR[OCTHLD]=011b		1.20/(10 x Rsense)		
		LDO_CR[OCTHLD]=100b		1.25/(10 x Rsense)		
		LDO_CR[OCTHLD]=101b		1.30/(10 x Rsense)		
		LDO_CR[OCTHLD]=110b		1.35/(10 x Rsense)		
		LDO_CR[OCTHLD]=111b		1.40/(10 x Rsense)		

1. V_{OUT} is configurable by LDO_VTRM[VTRM], it must be lower than 5.2 V. User can check the voltage dropout of MOSFET to avoid over power consumption.
2. This value is affected by the precision of the output voltage divider resistor.
3. N is configured by LDO_VTRM[VTRM].

3.1.2 Programmable gain amplifier (PGA) electronic characterizations

This section includes information about PGA.

Table 12. PGA electrical characteristics (4.5 V ≤ VDDA ≤ 5.5 V)

Symbol	Description		Min.	Typical	Max.	Unit
Gain	Programmable gain	PGA_CTRL[GAIN]=00b	—	8	—	
		PGA_CTRL[GAIN]=01b		10		
		PGA_CTRL[GAIN]=10b		15		
		PGA_CTRL[GAIN]=11b		20		
dGain/dT	Gain versus temperature		—	10	—	ppm/°C
V_{OS}	Input referred offset voltage[1]		-12	—	12	mV
dV_{OS}/dT	Input referred offset voltage versus temperature		—	20	—	µV/°C
I_{IN_BIAS}	Input BIAS current		—	—	250	µA
Bw(-3 dB)	PGA -3 dB bandwidth	PGA_CTRL[GAIN]=00b	—	—	2.0	MHz
		PGA_CTRL[GAIN]=01b			1.6	
		PGA_CTRL[GAIN]=10b			1.0	
		PGA_CTRL[GAIN]=11b			0.8	
PSRR	Power supply rejection ratio		—	-60	—	dB
CMRR	Common mode rejection ratio		—	-60	—	dB
VR_CM_IN	Input common mode voltage		4.5	5	5.5	V
VR_DM_IN	Input differential mode voltage	PGA_CTRL[GAIN]=00b	—	—	250	mV
		PGA_CTRL[GAIN]=01b			200	
		PGA_CTRL[GAIN]=10b			130	
		PGA_CTRL[GAIN]=11b			100	

1. The output referred offset of PGA is digitized by the on-chip ADC and stored in certain memory of each chip, customer can access the data to perform system level calibration.

3.1.3 Communication and clamp controller (CNC) electronic characterizations

This section includes information about FSK Zero-Crossing, VREC and VAD analog comparators.

Table 13. FSK analog comparator electrical specifications

Symbol	Characteristic		Min.	Typical	Max.	Unit
V_{DDA}	Supply voltage		3.5	—	5.5	V
I_{DDA}	Power consumption		—	270	—	µA
V_{AIN}	Analog input range		V_{SS}	—	V_{DD} - 1.4	V
V_{AIO}	Analog input offset voltage		—	—	20	mV
V_H	Analog comparator hysteresis	CNC_ANACFG1[ZCDHYST] = 00b	—	0	—	mV
		CNC_ANACFG1[ZCDHYST] = 01b		18		

Table 13. FSK analog comparator electrical specifications

Symbol	Characteristic		Min.	Typical	Max.	Unit
		CNC_ANACFG1[ZCDHYST] = 10b		40		
		CNC_ANACFG1[ZCDHYST] = 11b		60		

Table 14. CNC over-voltage protect (OVP) and low-voltage protect (LVP) electrical specifications

Symbol	Characteristic		Min.	Typical	Max.	Unit
$V_{REC-OVP}$	VREC OVP assert	CNC_ANACFG1[VRECOVLVL]=00b	—	25.7	—	V
		CNC_ANACFG1[VRECOVLVL]=01b	21.5	22.5	23.2	
		CNC_ANACFG1[VRECOVLVL]=10b	19.3	20.3	21.2	
		CNC_ANACFG1[VRECOVLVL]=11b	16.4	17.1	18	
$V_{REC-OVPR}$	VREC OVP de-assert	CNC_ANACFG1[VRECOVLVL]=00b	—	20.4	—	V
		CNC_ANACFG1[VRECOVLVL]=01b	17	17.8	18.4	
		CNC_ANACFG1[VRECOVLVL]=10b	15.2	16.2	16.8	
		CNC_ANACFG1[VRECOVLVL]=11b	12.8	13.5	14	
$V_{REC-LVP}$	VREC LVP assert		4.3	4.5	4.7	V
$V_{REC-LVPR}$	VREC LVP de-assert		4.9	5.1	5.3	V
V_{AD-OVP}	VAD OVP assert		5.5	5.7	5.9	V
$V_{AD-OVPR}$	VAD OVP de-assert		5.15	5.3	5.5	V
V_{AD-OK}	VAD LVP assert		4.15	4.3	4.55	V
V_{AD-OK}	VAD LVP de-assert		3.95	4.0	4.25	V

3.2 Core modules

3.2.1 SWD electricals

Table 15. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation • Serial wire debug	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns

Table continues on the next page...

Table 15. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	0	—	ns

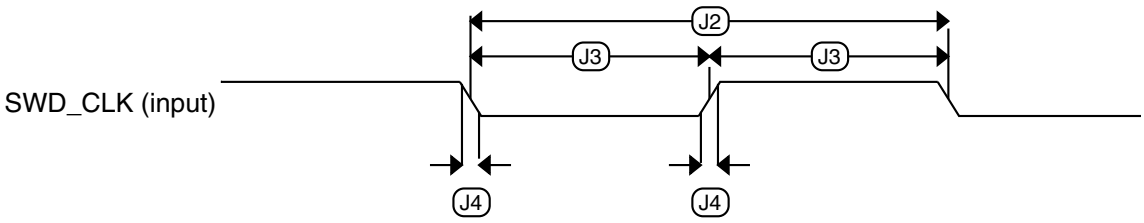


Figure 7. Serial wire clock input timing

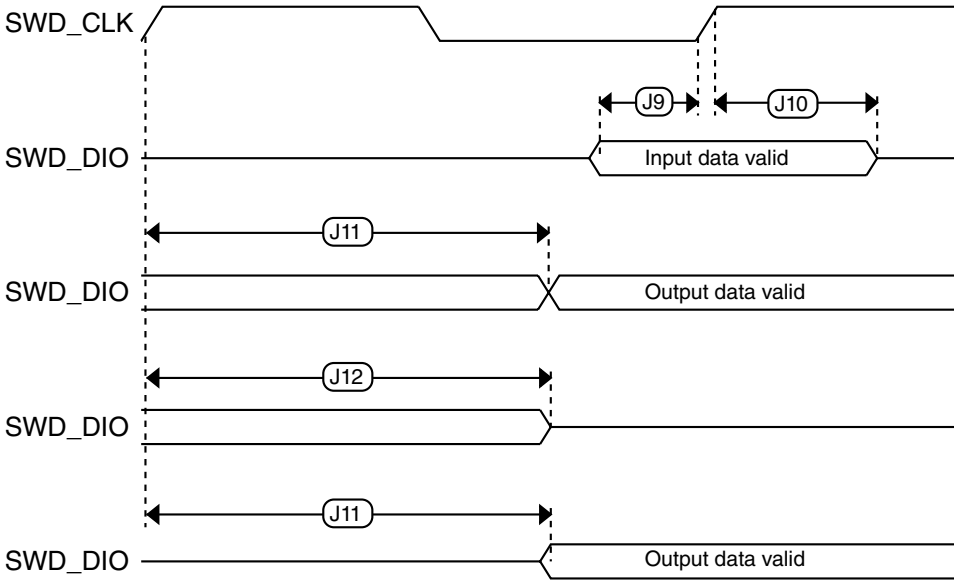


Figure 8. Serial wire data timing

3.3 Clock modules

3.3.1 External oscillator (OSC) and ICS characteristics

Table 16. OSC and ICS specifications (temperature range = -40 to 85 °C ambient)

Characteristic		Symbol	Min	Typical[1]	Max	Unit
Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	High range (RANGE = 1)	f_{hi}	4	—	24	MHz
Load capacitors		C1, C2	See Note[2]			
Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
	Low Frequency, High-Gain Mode		—	10	—	MΩ
	High Frequency, Low-Power Mode		—	1	—	MΩ
	High Frequency, High-Gain Mode		—	1	—	MΩ
Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
	High-Gain Mode		—	200	—	kΩ
Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	8 MHz		—	0	—	kΩ
	16 MHz		—	0	—	kΩ
	24 MHz		—	0	—	kΩ
Crystal start-up time low range = 32.768 kHz crystal; High range = 24 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	Low range, high gain		—	800	—	ms
	High range, low power	t_{CSTH}	—	3	—	ms
	High range, high gain		—	1.5	—	ms
Internal reference start-up time		t_{IRST}	—	20	50	µs
Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	37.5	—	kHz
DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	40	—	50	MHz
Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 85°C	Δf_{int_t}	-1	—	0.5	%
	Over temperature range from 0 °C to 85°C	Δf_{int_t}	-0.5	—	0.5	
Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 85°C	Δf_{dco_ft}	-2	—	1.5	%
	Over temperature range from 0 °C to 85°C	Δf_{dco_ft}	-1	—	1.5	

Table continues on the next page...

Table 16. OSC and ICS specifications (temperature range = -40 to 85 °C ambient) (continued)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
FLL acquisition time[4,6]	$t_{Acquire}$	—	—	2	ms
Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

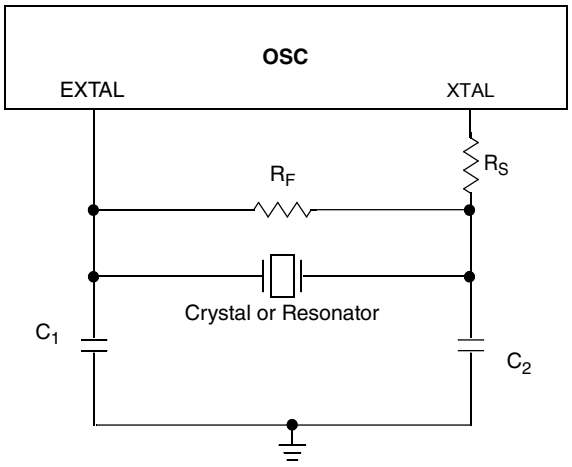


Figure 9. Typical crystal or resonator circuit

3.4 Memories and memory interfaces

3.4.1 NVM specifications

This section provides details about program / erase times, program / erase endurance for the flash memory.

Table 17. Flash characteristics

Characteristic	Symbol	Min.[1]	Typical[2]	Max.[3]	Unit[4]
NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
Erase Verify All Blocks	t_{VFYALL}	—	—	4653	t_{CYC}
Erase Verify Flash Block	t_{RD1BLK}	—	—	4626	t_{CYC}
Erase Verify Flash Section	t_{RD1SEC}	—	—	482	t_{CYC}
Read Once	t_{RDONCE}	—	—	464	t_{CYC}
Program Flash (2 words)	t_{PGM2}	0.14	0.14	0.35	ms
Program Flash (4 words)	t_{PGM4}	0.23	0.23	0.56	ms
Program Once	$t_{PGMONCE}$	0.22	0.23	0.23	ms
Erase All Blocks	t_{ERSALL}	95.54	100.31	100.56	ms
Erase Flash Block	t_{ERSBLK}	95.54	100.31	100.56	ms
Erase Flash Sector	t_{ERSPG}	19.11	20.06	20.10	ms
Unsecure Flash	t_{UNSECU}	95.55	100.31	100.57	ms
Configure NVM	$t_{CONFNVM}$	—	—	381	t_{CYC}
Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{CYC}
Set User Margin Level	t_{MLOADU}	—	—	420	t_{CYC}
FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
Data retention at an average junction temperature of T_{JAVG} = 85 °C after up to 10,000 program / erase cycles	t_{D_RET}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{CYC} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program and erase operations, see the Memory section.

3.5 Analog

3.5.1 IFR measurement conditions

The value stored in the IFR is measured under the conditions of the following table.

Table 18. IFR measurement conditions

Symbol	Descriptions	Value	Unit
V_{REFH}	ADC reference voltage	5	V
V_{REC}	Supply voltage from wireless receiver rectifier	5	V
V_{DDX}	I/O supply voltage	5	V
f_{BUS}	Bus frequency	24	MHz
T_A	Ambient temperature	25	°C
—	Code execution	From RAM	—
—	NVM activity	—	—

3.5.2 ADC characteristics

This section describes the ADC characteristics.

Table 19. ADC Operating Conditions

Characteristic		Symbol	Min	Typ	Max	Unit
Reference potential	Low	V_{RL}	V_{SSA}	—	V_{DDA} / 2	V
	High	V_{RH}	V_{DDA} / 2	—	V_{DDA}	V
Differential reference voltage[1]		V_{RH} - V_{RL}	3.13	5.0	5.5	V
ADC Clock Frequency (derived from bus clock via the prescaler bus)		f_{ATDCLK}	0.25	—	8.33	MHz
Buffer amplifier turn on time (delay after module start / recovery from Stop mode)		t_{REC}	—	—	1	µs
ADC disable time		$t_{DISABLE}$	—	—	3	bus clock cycles
ADC Conversion Period[2]	12-bit resolution	N_{CONV12}	19	—	39	ADC clock cycles
	10-bit resolution	N_{CONV10}	18	—	38	
	8-bit resolution	N_{CONV8}	16	—	36	

1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V.
2. The minimum time assumes a sample time of four ATD clock cycles. The maximum time assumes a sample time of 24 ATD clock cycles.

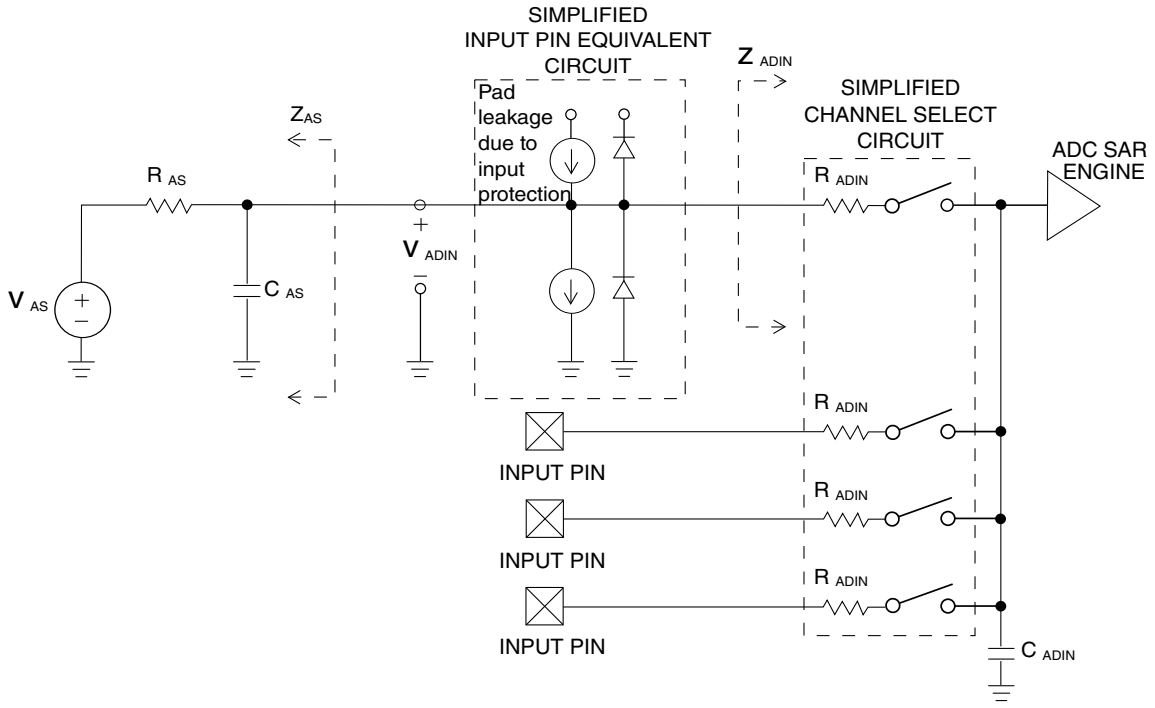


Figure 10. ADC Input Impedance Equivalency Diagram

Table 20. ADC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Max input source resistance	R_S	—	—	1	KΩ
Total input capacitance Non sampling	C_{INN}	—	—	10	pF
Total input capacitance sampling	C_{INS}	—	—	16	
Input internal Resistance	R_{INA}	—	5	15	KΩ
Disruptive analog input current	I_{NA}	0.25	—	2.5	mA
Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

Table 21. ADC Conversion Performance

Characteristic[1]		Symbol	Min	Typical	Max	Unit
Resolution	12-Bit	LSB	—	1.25	—	mV
Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
Resolution	10-Bit	LSB	—	5	—	mV
Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
Integral Nonlinearity	10-Bit	INL	-2.5	±1	2.5	counts
Absolute Error[2]	10-Bit	AE	-3	±2	3	counts

Table continues on the next page...

Table 21. ADC Conversion Performance (continued)

Characteristic[1]		Symbol	Min	Typical	Max	Unit
Resolution	8-Bit	LSB	—	20	—	mV
Differential Non-linearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
Integral Non-linearity	8-Bit	INL	-1	±0.5	1	counts
Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.
2. These values include the quantization error which is inherently 1/2 count for any ADC.

NOTE

Supply voltage V_{DDA} = 5.12 V. External $V_{REF} = V_{RH} - V_{RL}$ = 5.12 V. f_{ADCCLK} = 8.0 MHz The values are tested to be valid with no IO PORT output drivers switching simultaneous with conversions.

3.5.3 Analog comparator (ACMP) electricals

Table 22. Comparator electrical specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply current (Operation mode)	I_{DDA}	—	10	20	µA
Supply current, low-speed mode (EN = 1, PMODE = 0)	I_{DDLS}	—	18	20	µA
Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
Analog input offset voltage	V_{AIO}	—	—	40	mV
Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
Analog comparator initialization delay[1]		—	—	40	µs
Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
6-bit DAC current adder (enabled)	I_{DAC6b}	—	7	—	µA
Propagation Delay	t_D	—	0.4	1	µs
6-bit DAC integral non-linearity	INL	–0.5	—	0.5	LSB[2]
6-bit DAC differential non-linearity	DNL	–0.3	—	0.3	LSB[2]

1. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
2. 1 LSB = $V_{reference}/64$

3.6 Communication interfaces

3.6.1 Inter-Integrated Circuit Interface (I2C) timing

Table 23. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode[1]		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[2]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	μs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[3]	3.45[4]	0[5]	0.9[3]	μs
Data set-up time	t_{SU}; DAT	250[6]	—	100[4, 7]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[8]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[7]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. Fast mode is fully supported on all pins at VDD > 2.7 V. If VDD < 2.7 V, only pins that support high drive strength can support fast mode with maximum bus loading.
2. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V
3. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
4. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
5. Input signal Slew = 10 ns and Output Load = 50 pF
6. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
7. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
8. C_b = total capacitance of the one bus line in pF.

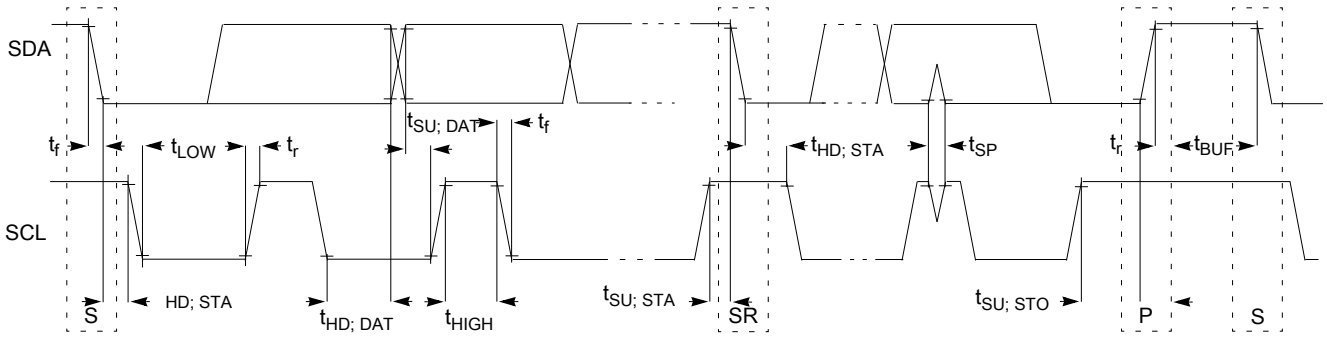


Figure 11. Timing definition for fast and standard mode devices on the I²C bus

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00615D
36-pin WLCSP	98ASA00789D

5 Pinout

5.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document.

NOTE

VDD1 and VDD2 must be short on PCB.

PTA6 and PTA7 are true open drain pins. The external pullup resistor must be added to make them output correct values in using I2C0, GPIO, and UART0.

The NC pin must be floating, and do not tie it to the any of the VDD or VSS.

32 QFN	36 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
—	C3	VSS1	VSS1	VSS1			
—	C4	VSS1	VSS1	VSS1			
—	D3	VDD1	VDD1	VDD1			
—	D4	VDD1	VDD1	VDD1			
1	A1	VREC	VREC	VREC			
2	A2	VDD1	VDD1	VDD1			
3	A3	VSS1	VSS1	VSS1			
4	B3	PTA0	DISABLED	PTA0	SBAR_IN1	EXTAL	
5	B4	PTA1	DISABLED	PTA1	SBAR_OUT0	XTAL	
6	A4	PTA2	DISABLED	PTA2	BUSOUT	SBAR_OUT1	FTM0_CH0
7	A5	PTA3	DISABLED	PTA3	CLAMP	ACMP0_OUT	FTM0_CH1
8	A6	PTA4	SWDIO	PTA4	SWDIO		FTM1_CH0
9	B6	PTA5	SWCLK	PTA5	SWCLK		FTM1_CH1
10	B5	PTA6	DISABLED	PTA6	I2C0_SDA	UART0_RX	
11	C5	PTA7	DISABLED	PTA7	I2C0_SCL	UART0_TX	
12	C6	VSS2/ VSSA	VSS2/ VSSA	VSS2/ VSSA			
13	D6	VDD2/ VDDA	VDD2/ VDDA	VDD2/ VDDA			
14	E6	PTB0/ RESET_b/ NMI_b	RESET_b	PTB0	IRQ	NMI_b	RESET_b
15	D5	PTB1	DISABLED	PTB1	ADCAD0	SBAR_IN0	
16	E5	PTB2	DISABLED	PTB2	ADCAD1	ACMP0_IN0	
17	F6	PTB3	DISABLED	PTB3	ADCAD2	ACMP0_IN1	
18	E4	PTB4	DISABLED	PTB4	ADCAD3		
19	F5	VSS3	VSS3	VSS3			
20	F4	VREFH	VREFH	VREFH			
21	F3	VOUT_FB	VOUT_FB	VOUT_FB			
23	F2	VOUT	VOUT	VOUT			
24	F1	ISENS	ISENS	ISENS			
25	E2	CLC1	CLC1	CLC1			
26	D2	VLC	VLC	VLC			
27	E1	GD	GD	GD			
28	D1	VBOOT	VBOOT	VBOOT			
29	C2	AD_IN	AD_IN	AD_IN			
30	B2	AD_EN	AD_EN	AD_EN			

32 QFN	36 WLC SP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
31	C1	AC1	AC1	AC1			
32	B1	AC2	AC2	AC2			

5.2 Device pin assignment

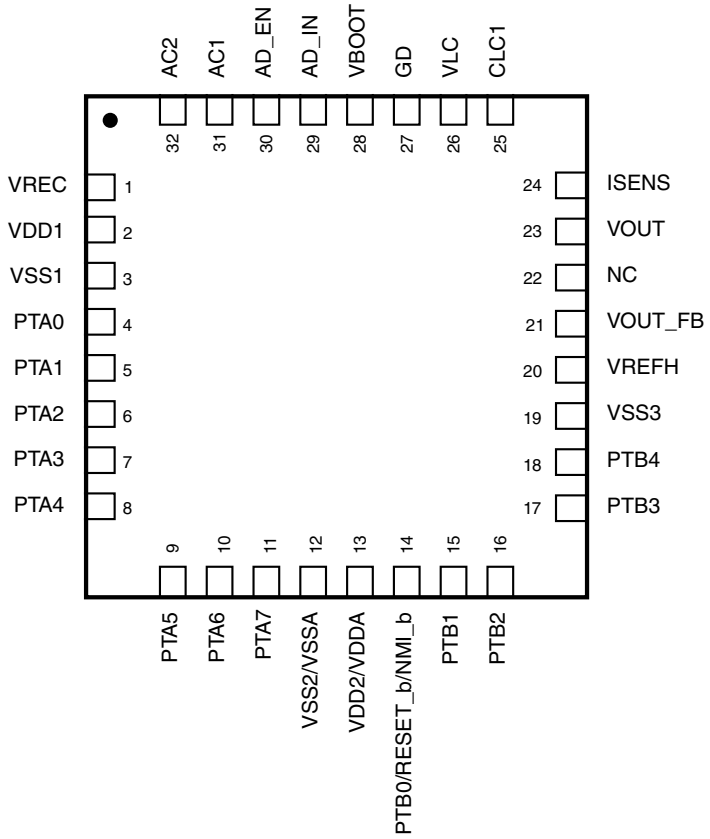


Figure 12. 32-pin QFN package

NOTE

The NC pin must be floating, and do not tie it to the VDD or VSS.

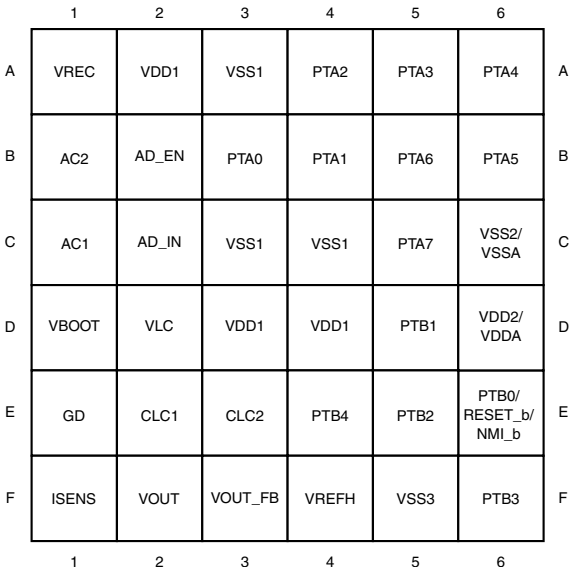


Figure 13. 36-pin WLCSP package

6 Ordering Parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: WPR1516.

7 Part Identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q WPR## FFF R T PP N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
WPR##	WPR family	• WPR15
FFF	Program flash memory size	• 16 = 16 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• C = -40 to 85 °C
PP	Package identifier	• FM=32 QFN (5 mm x 5 mm) • AL=36 WLCSP (3.1 mm x 3.0 mm)
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MWPR1516CFM

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

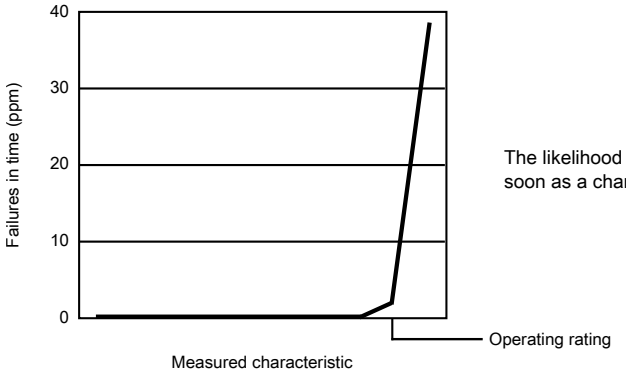
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

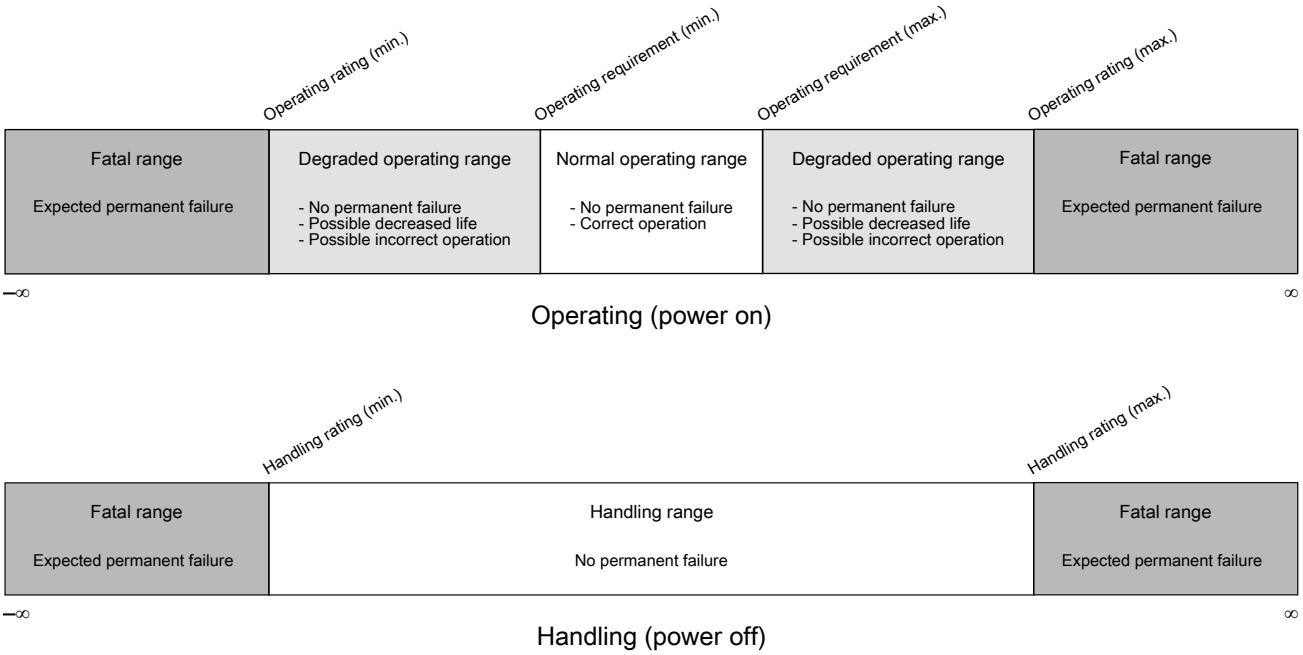
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

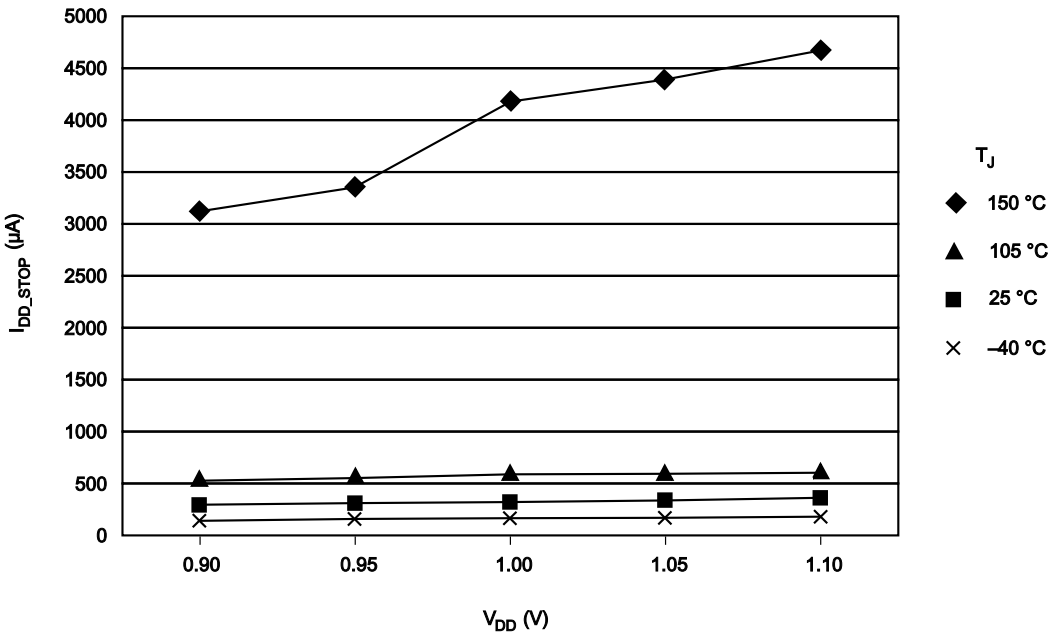
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 24. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 25. Revision history

Rev. No.	Date	Substantial Changes
2	1/2015	Initial public release.

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