

# W-LAN+Bluetooth® Combo Module Data Sheet

Infineon CYW4373 Chipset  
for 802.11a/b/g/n/ac + Bluetooth® 5.2

Design Name: Type2BC  
Tentative P/N : LBEE5PK2BC-771  
Sample P/N : LBEE5PK2BC-SMP

***This Datasheet is preliminary version, and subject to change without notice***

## Revision History

| Revision Code | Date                       | Description                                                                                                                                                                                                     | Comments |
|---------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| -             | July 17 <sup>th</sup> 2020 | First Issue                                                                                                                                                                                                     |          |
| A             | Apr 30 <sup>th</sup> 2021  | <ul style="list-style-type: none"> <li>• Scope</li> <li>• Part Number</li> <li>• Dimensions, Marking and Terminal Configurations</li> <li>• DC / RF Characteristics</li> <li>• Tape and Reel Packing</li> </ul> | Update   |
| B             | Dec 29 <sup>th</sup> 2021  | <ul style="list-style-type: none"> <li>• DC / RF Characteristics</li> <li>• Module height</li> <li>• Bandgap reference resistor to 4.75K ohm +/-1%.</li> </ul>                                                  | Update   |
| C             | Feb 16 <sup>th</sup> 2022  | <ul style="list-style-type: none"> <li>• Scope BT 5.2</li> <li>• Bluetooth® QDID</li> </ul>                                                                                                                     | Update   |
| D             | May 5 <sup>th</sup> 2022   | <ul style="list-style-type: none"> <li>• terminal configuration</li> <li>• DC / RF Characteristics</li> </ul>                                                                                                   | Update   |
| E             | June 14 <sup>th</sup> 2022 | <ul style="list-style-type: none"> <li>• Scope IC P/N</li> </ul>                                                                                                                                                | Update   |

## TABLE OF CONTENTS

|                                                                    |    |
|--------------------------------------------------------------------|----|
| Revision History.....                                              | 1  |
| 1. Scope .....                                                     | 4  |
| 2. Part Number .....                                               | 4  |
| 3. Block Diagram .....                                             | 4  |
| 4. Certification Information .....                                 | 5  |
| 4.1. Radio Certification .....                                     | 5  |
| 4.2. Bluetooth® Qualification .....                                | 5  |
| 5. Dimensions, Marking and Terminal Configurations .....           | 6  |
| 6. Rating .....                                                    | 12 |
| 7. Operating Condition .....                                       | 12 |
| 7.1. Operating condition .....                                     | 12 |
| 7.2. External LPO signal Requirement .....                         | 12 |
| 8. Power Up Sequence .....                                         | 13 |
| 8.1. Power Up Sequence for WLAN ON, and BT ON .....                | 13 |
| 8.2. Power Up Sequence for WLAN ON, and BT OFF .....               | 13 |
| 8.3. Power Up Sequence for WLAN OFF, and BT ON .....               | 14 |
| 8.4. Power Up Sequence for WLAN OFF, and BT OFF .....              | 14 |
| 9. Digital I/O Requirements .....                                  | 15 |
| 9.1. Digital I/O Pins.....                                         | 15 |
| 9.2. RF Switch Control Output Pins .....                           | 15 |
| 10. Interface Timing.....                                          | 16 |
| 10.1. SDIO Timing (Default Mode) .....                             | 16 |
| 10.2. SDIO Timing (High Speed Mode) .....                          | 17 |
| 10.3. SDIO BUS Timing Specifications in SDR Modes .....            | 18 |
| 10.4. SDIO Timing Specifications in DDR50 Mode .....               | 21 |
| 10.5. UART Timing (Default Mode) .....                             | 22 |
| 10.6. Bluetooth® PCM Timing .....                                  | 23 |
| 10.6.1. Short Frame Sync, Master Mode .....                        | 23 |
| 10.7. Short Frame Sync, Slave Mode .....                           | 24 |
| 10.8. Long Frame Sync, Master Mode .....                           | 24 |
| 10.9. Long Frame Sync, Slave Mode .....                            | 25 |
| 10.9.1. Short Frame Sync, Burst Mode .....                         | 25 |
| 10.9.2. Long Frame Sync, Burst Mode .....                          | 26 |
| 11. DC / RF Characteristics.....                                   | 27 |
| 11.1. DC/RF Characteristics for IEEE802.11b - 2.4GHz .....         | 27 |
| 11.1.1. High Rate Condition for IEEE802.11b – 2.4GHz .....         | 27 |
| 11.1.2. Low Rate Condition for IEEE802.11b – 2.4GHz .....          | 28 |
| 11.2. DC/RF Characteristics for IEEE802.11g - 2.4GHz .....         | 29 |
| 11.2.1. High Rate Condition for IEEE802.11g – 2.4GHz .....         | 29 |
| 11.2.2. Low Rate Condition for IEEE802.11g – 2.4GHz .....          | 30 |
| 11.3. DC/RF Characteristics for IEEE802.11n – 2.4GHz .....         | 31 |
| 11.3.1. High Rate Condition for IEEE802.11n – 2.4GHz .....         | 31 |
| 11.3.2. Low Rate Condition for IEEE802.11n – 2.4GHz .....          | 32 |
| 11.4. DC/RF Characteristics for IEEE802.11a - 5GHz .....           | 33 |
| 11.4.1. High Rate Condition for IEEE802.11a – 5GHz .....           | 33 |
| 11.4.2. Low Rate Condition for IEEE802.11a – 5GHz .....            | 34 |
| 11.5. DC/RF Characteristics for IEEE802.11n(HT20) - 5GHz .....     | 34 |
| 11.5.1. High Rate Condition for IEEE802.11n(HT20) – 5GHz .....     | 34 |
| 11.5.2. Low Rate Condition for IEEE802.11n(HT20) – 5GHz .....      | 35 |
| 11.6. DC/RF Characteristics for IEEE802.11ac(HT20) - 5GHz .....    | 35 |
| 11.6.1. High Rate Condition for IEEE802.11ac(VHT20) – 5GHz .....   | 35 |
| 11.6.2. Low Rate Condition for IEEE802.11ac(VHT20) – 5GHz .....    | 36 |
| 11.7. DC/RF Characteristics for IEEE802.11n(HT 40MHz) - 5GHz ..... | 36 |
| 11.7.1. High Rate Condition for IEEE802.11n(HT40) – 5GHz .....     | 36 |
| 11.7.2. Low Rate Condition for IEEE802.11n(HT40) – 5GHz .....      | 37 |

Preliminary

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|                                                                     |    |
|---------------------------------------------------------------------|----|
| 11.8. DC/RF Characteristics for IEEE802.11ac(VHT 40MHz) - 5GHz..... | 37 |
| 11.8.1. High Rate Condition for IEEE802.11ac(VHT40) – 5GHz.....     | 37 |
| 11.8.2. Low Rate Condition for IEEE802.11ac(VHT40) – 5GHz.....      | 38 |
| 11.9. DC/RF Characteristics for IEEE802.11ac(VHT 80MHz) - 5GHz..... | 38 |
| 11.9.1. High Rate Condition for IEEE802.11ac(VHT80) – 5GHz.....     | 38 |
| 11.9.2. Low Rate Condition for IEEE802.11ac(VHT80) – 5GHz.....      | 39 |
| 11.10. DC/RF Characteristics for Bluetooth®.....                    | 40 |
| 11.11. DC/RF Characteristics for Bluetooth® (LE).....               | 41 |
| 12. Land Patterns.....                                              | 42 |
| 13. Reference Circuit.....                                          | 43 |
| 14. Tape and Reel Packing.....                                      | 45 |
| 15. Notice.....                                                     | 48 |
| 15.1. Storage Conditions.....                                       | 48 |
| 15.2. Handling Conditions.....                                      | 48 |
| 15.3. Standard PCB Design (Land Pattern and Dimensions).....        | 48 |
| 15.4. Notice for Chip Placer :.....                                 | 48 |
| 15.5. Soldering Conditions :.....                                   | 48 |
| 15.6. Cleaning :.....                                               | 49 |
| 15.7. Operational Environment Conditions :.....                     | 49 |
| 15.8. Input Power Capacity :.....                                   | 49 |
| 16. Regulatory Statements.....                                      | 50 |
| 16.1. FCC Statements.....                                           | 50 |
| 16.2. IC Statements.....                                            | 50 |
| 17. PRECONDITION TO USE OUR PRODUCTS.....                           | 51 |

 Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

## 1. Scope

This specification is applied to the IEEE802.11a/b/g/n/ac W-LAN + Bluetooth® 5.2 combo module.

- Host Interface
  - WLAN :SDIO or USB(shared)
  - BT/BLE :UART or USB(shared)
- IC P/N : Infineon / CYW4373
- Reference Clock : Reference clock embedded
- Weight : 0.2g
- RoHS : This component can meet with RoHS compliance.
- MSL\* : Level 3

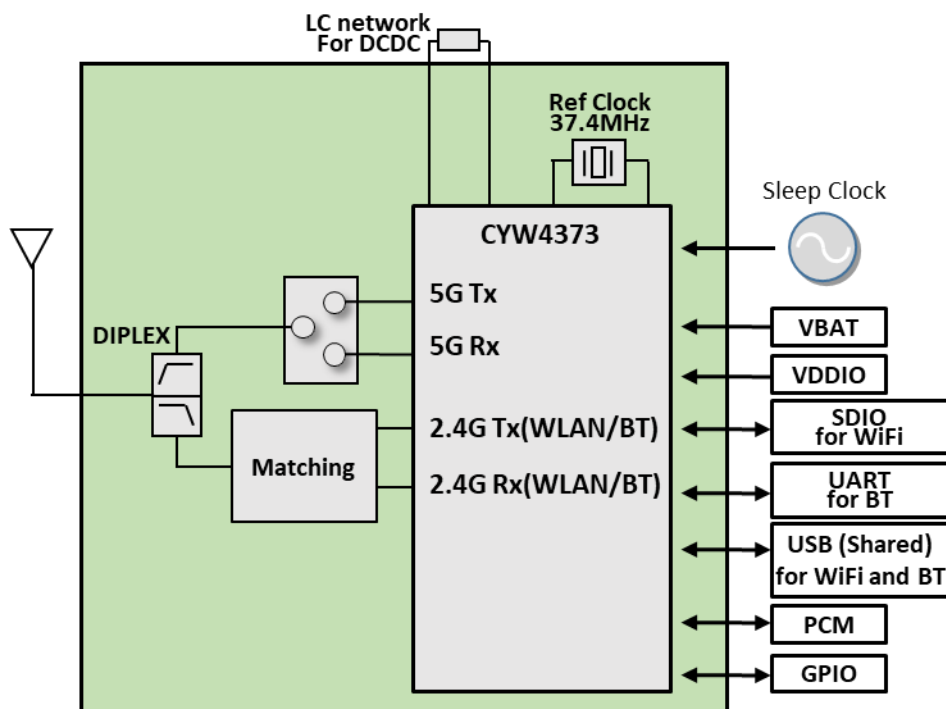
\*This product is moisture sensitive. Please check the detail in 15.1 Storage Condition section.

## 2. Part Number

| Ordering Part Number | Description             |
|----------------------|-------------------------|
| LBEE5PK2BC-EVB       | In case of EVB order    |
| LBEE5PK2BC-SMP       | In case of sample order |
| LBEE5PK2BC-771       | Mass Produced Product   |

“Type2BC” is design name of this module. Design name may be used in certification test report.

## 3. Block Diagram



## **4. Certification Information**

### **4.1. Radio Certification**

#### **USA/Canada**

FCC ID : T.B.D.

IC : T.B.D

\*Please follow installation manual of Appendix

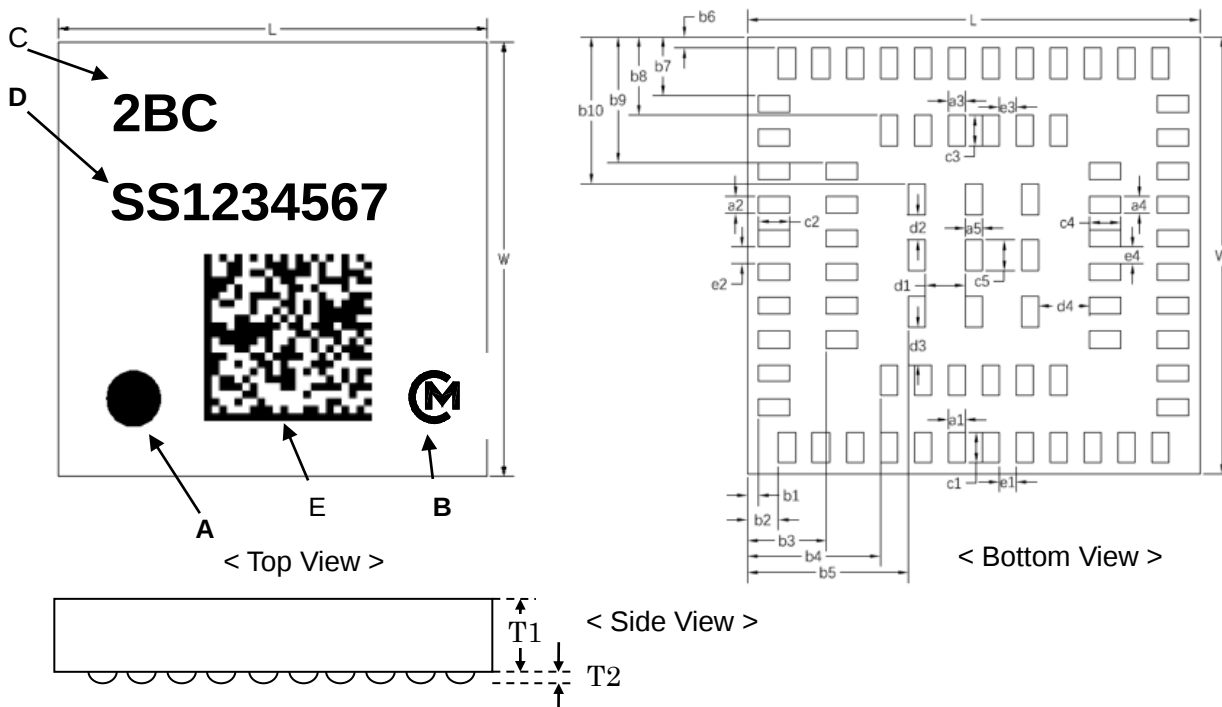
#### **Europe**

T.B.D.

### **4.2. Bluetooth® Qualification**

QDID: 173411

## 5. Dimensions, Marking and Terminal Configurations

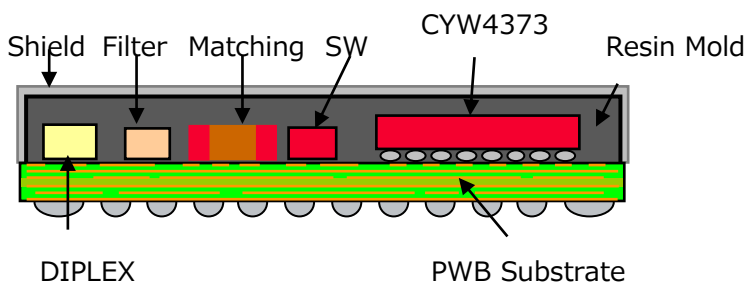


| Marking | Meaning                |
|---------|------------------------|
| A       | Pin 1 Marking          |
| B       | Murata Logo            |
| C       | Module Type            |
| D       | Inspection Number      |
| E       | 2D Code (Internal use) |

| Mark | Dimension | Mark | Dimension  | Mark | Dimension   |
|------|-----------|------|------------|------|-------------|
| L    | 8.00±0.20 | W    | 7.80±0.20  | T1   | 1.15 max    |
| a1   | 0.30±0.10 | a2   | 0.30±0.10  | a3   | 0.30±0.10   |
| a4   | 0.30±0.10 | a5   | 0.30±0.10  | b1   | 0.30±0.15   |
| b2   | 0.55±0.15 | b3   | 1.50±0.15  | b4   | 2.35±0.15   |
| b5   | 2.85±0.15 | b6   | 0.30±0.15  | b7   | 1.05±0.15   |
| b8   | 1.50±0.15 | b9   | 2.25±0.15  | b10  | 2.675±0.15  |
| c1   | 0.45±0.10 | c2   | 0.45±0.10  | c3   | 0.45±0.10   |
| c4   | 0.45±0.10 | c5   | 0.45±0.10  | d1   | 0.70±0.10   |
| d2   | 0.55±0.10 | d3   | 0.725±0.10 | d4   | 0.90±0.10   |
| e1   | 0.30±0.10 | e2   | 0.30±0.10  | e3   | 0.30±0.10   |
| e4   | 0.30±0.10 |      |            | T2   | 0.045±0.025 |

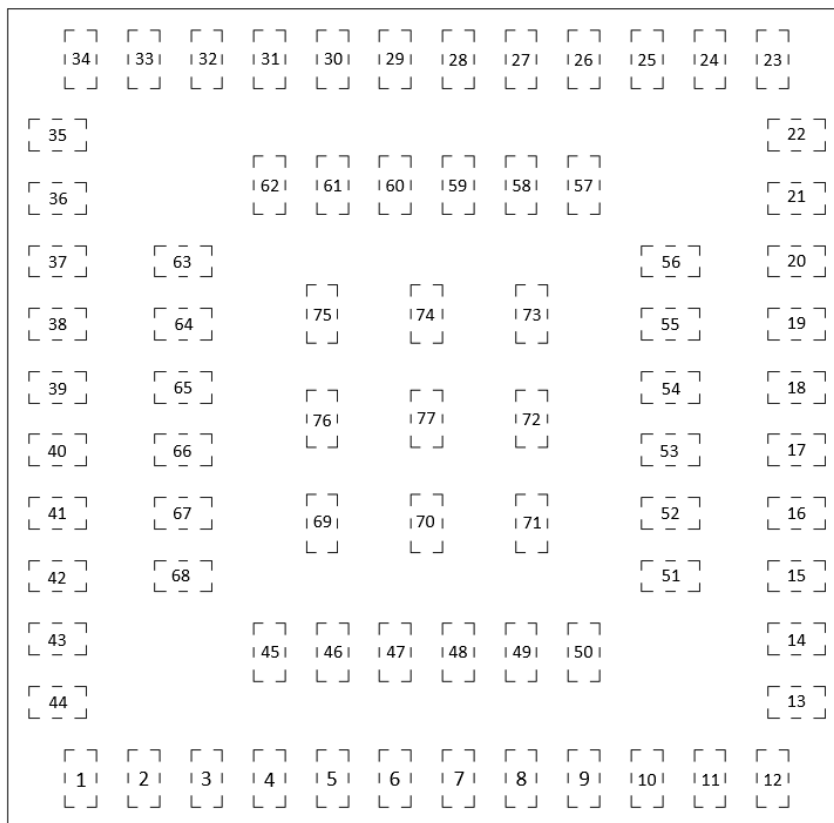
(unit : mm)

### Structure



# Pin Layout

<TOP View>



| No. | Terminal Name | No. | Terminal Name | No. | Terminal Name | No. | Terminal Name  |
|-----|---------------|-----|---------------|-----|---------------|-----|----------------|
| 1   | GND           | 21  | GND           | 41  | GND           | 61  | GND            |
| 2   | SR_VLX        | 22  | WL_ANT        | 42  | VDDIO         | 62  | GND            |
| 3   | VBAT          | 23  | GND           | 43  | VIN_LDO       | 63  | TRST_L         |
| 4   | WL_REG_EN     | 24  | GND           | 44  | VOUT_BBPLL    | 64  | JTAG_TDI       |
| 5   | LPO_IN        | 25  | RF_SW_CTRL_5  | 45  | GPIO_1        | 65  | JTAG_TDO       |
| 6   | BT_PCM_IN     | 26  | RF_SW_CTRL_0  | 46  | USB2_DM       | 66  | JTAG_TCK/SWCLK |
| 7   | BT_PCM_CLK    | 27  | GND           | 47  | USB2_DP       | 67  | JTAG_TMS/SWDIO |
| 8   | BT_PCM_SYNC   | 28  | SDIO_CMD      | 48  | USB2_MONCDR   | 68  | BT_REG_EN      |
| 9   | BT_PCM_OUT    | 29  | SDIO_DATA_1   | 49  | USB2_AVDD33   | 69  | GND            |
| 10  | BT_UART_TXD   | 30  | SDIO_DATA_0   | 50  | USB2_RREF     | 70  | GND            |
| 11  | BT_UART_CTS_N | 31  | SDIO_DATA_3   | 51  | BT_DEV_WAKE   | 71  | GND            |
| 12  | BT_UART_RXD   | 32  | SDIO_DATA_2   | 52  | WL_HOST_WAKE  | 72  | GND            |
| 13  | BT_UART_RTS_N | 33  | SDIO_CLK      | 53  | JTAG_SEL      | 73  | GND            |
| 14  | GND           | 34  | GND           | 54  | STRAP_1       | 74  | GND            |
| 15  | NC            | 35  | NC            | 55  | STRAP_2       | 75  | GND            |
| 16  | GND           | 36  | NC            | 56  | STRAP_0       | 76  | GND            |
| 17  | BT_HOST_WAKE  | 37  | NC            | 57  | GND           | 77  | GND            |
| 18  | BT_GPIO_2     | 38  | NC            | 58  | GND           |     |                |
| 19  | BT_GPIO_3     | 39  | NC            | 59  | NC            |     |                |
| 20  | BT_GPIO_5     | 40  | NC            | 60  | NC            |     |                |

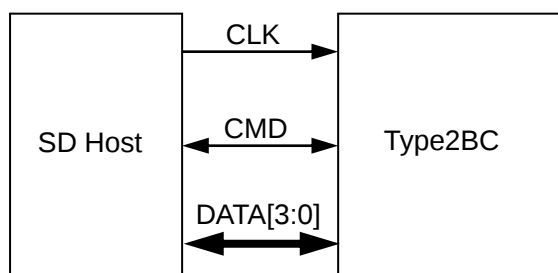
| No. | Terminal Name | Type | Connection to IC Terminal | Description                                                                                                                                                                                                                                                                              |
|-----|---------------|------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 2   | SR_VLX        | PO   | SR_VLX                    | CBUCK switching regulator output. Refer to Reference circuit for details of the inductor and capacitor required in this output.                                                                                                                                                          |
| 3   | VBAT          | PI   | SR_VDDBAT5V/LDO_VD DBAT5V | Supply to internal Power source of VBAT                                                                                                                                                                                                                                                  |
| 4   | WL_REG_EN     | I    | WL_REG_ON                 | Used by PMU to power-up or power down the internal CYW8x373 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 5   | LPO_IN        | I    | LPO_IN                    | External Sleep clock input(32.768kHz)                                                                                                                                                                                                                                                    |
| 6   | BT_PCM_IN     | I    | BT_PCM_IN                 | PCM data input.                                                                                                                                                                                                                                                                          |
| 7   | BT_PCM_CLK    | I/O  | BT_PCM_CLK                | PCM clock; can be master(output) or slave(input).                                                                                                                                                                                                                                        |
| 8   | BT_PCM_SYNC   | I/O  | BT_PCM_SYNC               | PCM sync; can be master(output) or slave(input).                                                                                                                                                                                                                                         |
| 9   | BT_PCM_OUT    | O    | BT_PCM_OUT                | PCM data output                                                                                                                                                                                                                                                                          |
| 10  | BT_UART_TXD   | O    | BT_UART_TXD               | UART serial output. Serial data output for the HCI UART interface.                                                                                                                                                                                                                       |
| 11  | BT_UART_CTS_N | I    | BT_UART_CTS_N             | UART clear – to - send. Active - low clear – to - send signal for the HCI UART interface.                                                                                                                                                                                                |
| 12  | BT_UART_RXD   | I    | BT_UART_RXD               | UART serial input. Serial data input for the HCI UART interface.                                                                                                                                                                                                                         |
| 13  | BT_UART_RTS_N | O    | BT_UART_RTS_N             | UART request – to - send. Active - low request - to-send signal for the HCI UART interface.                                                                                                                                                                                              |
| 14  | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 15  | NC            | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 16  | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 17  | BT HOST WAKE  | I/O  | BT HOST WAKE              | Host wake-up. Signal from the CYW4373 to the host indicating that the CYW4373 requires attention. The polarity of this signal is software configurable and can be asserted high or low.                                                                                                  |
| 18  | BT_GPIO_2     | I/O  | BT_GPIO_2                 | Bluetooth® general-purpose I/O.                                                                                                                                                                                                                                                          |
| 19  | BT_GPIO_3     | I/O  | BT_GPIO_3                 | Bluetooth® general-purpose I/O.                                                                                                                                                                                                                                                          |
| 20  | BT_GPIO_5     | I/O  | BT_GPIO_5                 | Bluetooth® general-purpose I/O.                                                                                                                                                                                                                                                          |
| 21  | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 22  | WL_ANT        | RF   | -                         | RF output for WLAN/BT                                                                                                                                                                                                                                                                    |
| 23  | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 24  | GND           | -    | -                         | -                                                                                                                                                                                                                                                                                        |
| 25  | RF_SW_CTRL_5  | O    | RF_SW_CTRL_5              | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.                                                                                                                                                                                  |

| No. | Terminal Name | Type | Connection to IC Terminal                                       | Description                                                                                                                                                                                                                                                                                                             |
|-----|---------------|------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26  | RF_SW_CTRL_0  | O    | RF_SW_CTRL_0                                                    | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.                                                                                                                                                                                                                 |
| 27  | GND           | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 28  | SDIO_CMD      | I/O  | SDIO_CMD                                                        | SDIO command line                                                                                                                                                                                                                                                                                                       |
| 29  | SDIO_DATA_1   | I/O  | SDIO_DATA_1                                                     | SDIO data line 1                                                                                                                                                                                                                                                                                                        |
| 30  | SDIO_DATA_0   | I/O  | SDIO_DATA_0                                                     | SDIO data line 0                                                                                                                                                                                                                                                                                                        |
| 31  | SDIO_DATA_3   | I/O  | SDIO_DATA_3                                                     | SDIO data line 3                                                                                                                                                                                                                                                                                                        |
| 32  | SDIO_DATA_2   | I/O  | SDIO_DATA_2                                                     | SDIO data line 2                                                                                                                                                                                                                                                                                                        |
| 33  | SDIO_CLK      | I    | SDIO_CLK                                                        | SDIO clock input                                                                                                                                                                                                                                                                                                        |
| 34  | GND           | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 35  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 36  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 37  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 38  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 39  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 40  | NC            | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 41  | GND           | -    | -                                                               | -                                                                                                                                                                                                                                                                                                                       |
| 42  | VDDIO         | PI   | VDDIO/BT_VDDO                                                   | Supply for PMU, BT, WLAN, SDIO.                                                                                                                                                                                                                                                                                         |
| 43  | VIN_LDO       | PI   | LDO_VDD1P5/WRF_AFE_VDD1P35/<br>WRF_XTAL_VDD1P35/WRF_PMU_VDD1P35 | Input for LDO_VDD1P5/WRF_AFE_VDD1P35/<br>WRF_XTAL_VDD1P35/WRF_PMU_VDD1P35                                                                                                                                                                                                                                               |
| 44  | VOUT_BBPLL    | PO   | VOUT_HLDO                                                       | 1.2V supply for the PCIe.                                                                                                                                                                                                                                                                                               |
| 45  | GPIO_1        | I/O  | GPIO_1                                                          | Programmable GPIO Pin                                                                                                                                                                                                                                                                                                   |
| 46  | USB2_DM       | I/O  | USB2_DM                                                         | Data minus of shared USB2.0 port.                                                                                                                                                                                                                                                                                       |
| 47  | USB2_DP       | I/O  | USB2_DP                                                         | Data plus of shared USB2.0 port.                                                                                                                                                                                                                                                                                        |
| 48  | USB2_MONCDR   | O    | USB2_MONCDR                                                     | CDR monitor for debug.                                                                                                                                                                                                                                                                                                  |
| 49  | USB2_AVDD33   | PI   | USB2_AVDD33                                                     | Power Supply for shared USB2.0. When VBAT is between 3.6V to 4.8V connect to VOUT_3P3 i.e. 3.3V output of LDO3P3. When VBAT is 3.3V connect directly to VBAT.                                                                                                                                                           |
| 50  | USB2_RREF     | I/O  | USB2_RREF                                                       | Bandgap reference resistor;<br>4.75K ohm +/-1% for USB.<br>DNI for SDIO.                                                                                                                                                                                                                                                |
| 51  | BT_DEV_WAKE   | I    | BT_DEV_WAKE                                                     | Bluetooth® device wake-up: Signal from the host to the CYW4373 indicating that the host requires attention. The polarity of this signal is software configurable and can be asserted high or low                                                                                                                        |
| 52  | WL_HOST_WAKE  | O    | GPIO_0                                                          | Programmable GPIO Pin                                                                                                                                                                                                                                                                                                   |
| 53  | JTAG_SEL      | I    | JTAG_SEL                                                        | JTAG select. This pin must be kept NO CONNECT if the JTAG interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL = 1:<br><ul style="list-style-type: none"> <li>■ GPIO_2 is TCK</li> <li>■ GPIO_3 is TMS</li> <li>■ GPIO_4 is TDIO</li> <li>■ GPIO_5 is TDO</li> <li>■ GPIO_6 is TRST_L</li> </ul> |

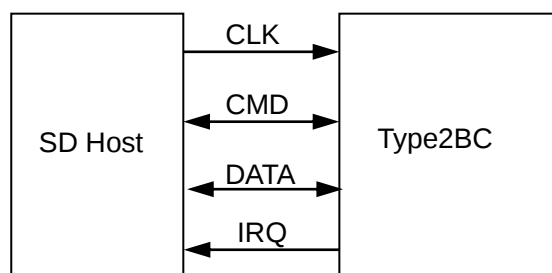
| No. | Terminal Name  | Type | Connection to IC Terminal | Description                                                                                                                                                                                                                                                                                          |
|-----|----------------|------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 54  | STRAP_1        | I    | STRAP_1                   | USBHUB_BYPASS                                                                                                                                                                                                                                                                                        |
| 55  | STRAP_2        | I    | STRAP_2                   | USB_DISABLE<br>1: USB disable<br>0: USB enable                                                                                                                                                                                                                                                       |
| 56  | STRAP_0        | I    | STRAP_0                   | SDIO_PADVDDIO sel<br>1: SDIO is 1.8V<br>0: SDIO is 3.3V or USB mode                                                                                                                                                                                                                                  |
| 57  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 58  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 59  | NC             | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 60  | NC             | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 61  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 62  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 63  | TRST_L         | I/O  | GPIO_6                    | GPIO_6 is TRST_L                                                                                                                                                                                                                                                                                     |
| 64  | JTAG_TDI       | I/O  | GPIO_4                    | GPIO_4 is TDI                                                                                                                                                                                                                                                                                        |
| 65  | JTAG_TDO       | I/O  | GPIO_5                    | GPIO_5 is TDO                                                                                                                                                                                                                                                                                        |
| 66  | JTAG_TCK/SWCLK | I/O  | GPIO_2                    | GPIO_2 is TCK/SWCLK                                                                                                                                                                                                                                                                                  |
| 67  | JTAG_TMS/SWDIO | I/O  | GPIO_3                    | GPIO_3 is TMS/SWDIO                                                                                                                                                                                                                                                                                  |
| 68  | BT_REG_EN      | I    | BT_REG_ON                 | Used by PMU to power-up or power down the internal CYW8x373 regulators used by the Bluetooth® section. Also, when deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 69  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 70  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 71  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 72  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 73  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 74  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 75  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 76  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |
| 77  | GND            | -    | -                         | -                                                                                                                                                                                                                                                                                                    |

## SDIO Pin Description

| No. | Pin Name | (i) SD 4-bit Mode |                        | (ii) SD 1-bit Mode |              |
|-----|----------|-------------------|------------------------|--------------------|--------------|
| 20  | SDIO_CLK | CLK               | Clock                  | CLK                | Clock        |
| 17  | SDIO_D0  | DATA0             | Data line 0            | DATA               | Data line    |
| 15  | SDIO_D1  | DATA1             | Data line 1 /Interrupt | IRQ                | Interrupt    |
| 16  | SDIO_D2  | DATA2             | Data line 2            | NC                 | Not used     |
| 14  | SDIO_D3  | DATA3             | Data line 3            | NC                 | Not used     |
| 18  | SDIO_CMD | CMD               | Command line           | CMD                | Command line |



(i) SD 4-bit Mode



(ii) SD 1-bit Mode

## Strapping Options

| Mode Select | STRAP_2 | STRAP_1 | STRAP_0                              |
|-------------|---------|---------|--------------------------------------|
| USB         | 0       | 0       | 0                                    |
| SDIO        | 1       | 0       | 0 = SDIO is 3.3V<br>1 = SDIO is 1.8V |

## 6. Rating

| Parameter           |       | Min  | Max  | Unit  |
|---------------------|-------|------|------|-------|
| Storage Temperature |       | -40  | +125 | deg.C |
| Supply Voltage      | VBAT  | -0.5 | 5.5  | V     |
|                     | VDDIO | -0.5 | 3.9  | V     |

\* Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

## 7. Operating Condition

### 7.1. Operating condition

| Parameter                                |       | Min               | Typ | Max               | Unit  |
|------------------------------------------|-------|-------------------|-----|-------------------|-------|
| Operating Temperature Range <sup>1</sup> |       | -20               | +25 | +70               | deg.C |
| Supply Voltage                           | VBAT  | 3.2 <sup>*1</sup> | 3.6 | 4.8 <sup>*2</sup> | V     |
|                                          | VDDIO | 1.62              | 1.8 | 1.98              | V     |
|                                          |       | 2.97              | 3.3 | 3.63              | V     |

\*1 CYW4373 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.6V<VBAT<4.8V.

\*2 The maximum continuous voltage is 4.8V.

### 7.2. External LPO signal Requirement

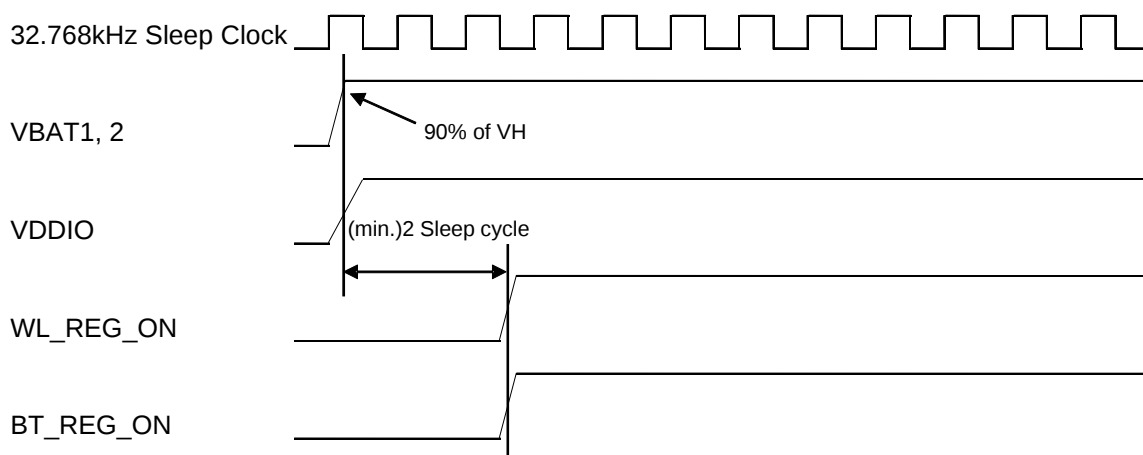
| Parameter                              | External LPO Clock       | Unit      |
|----------------------------------------|--------------------------|-----------|
| Nominal input frequency                | 32.768                   | kHz       |
| Frequency accuracy                     | +/-200                   | ppm       |
| Duty cycle                             | 30-70                    | %         |
| Input signal amplitude                 | 200 - 3300               | mV, p-p   |
| Signal type                            | Square-wave or sine-wave | -         |
| Input impedance <sup>*a</sup>          | > 100k<br>< 5            | ohm<br>pF |
| Clock jitter (during initial start-up) | <10,000                  | ppm       |

a) When power is applied or switch off.

<sup>1</sup> Functionality is guaranteed but specifications require derating at extreme temperatures

## 8. Power Up Sequence

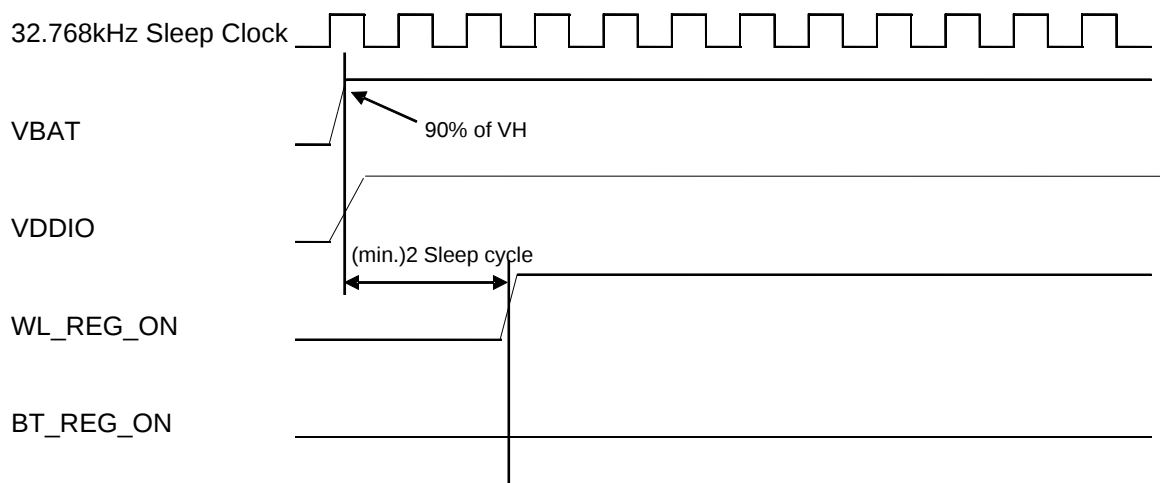
### 8.1. Power Up Sequence for WLAN ON, and BT ON



Notes:

1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

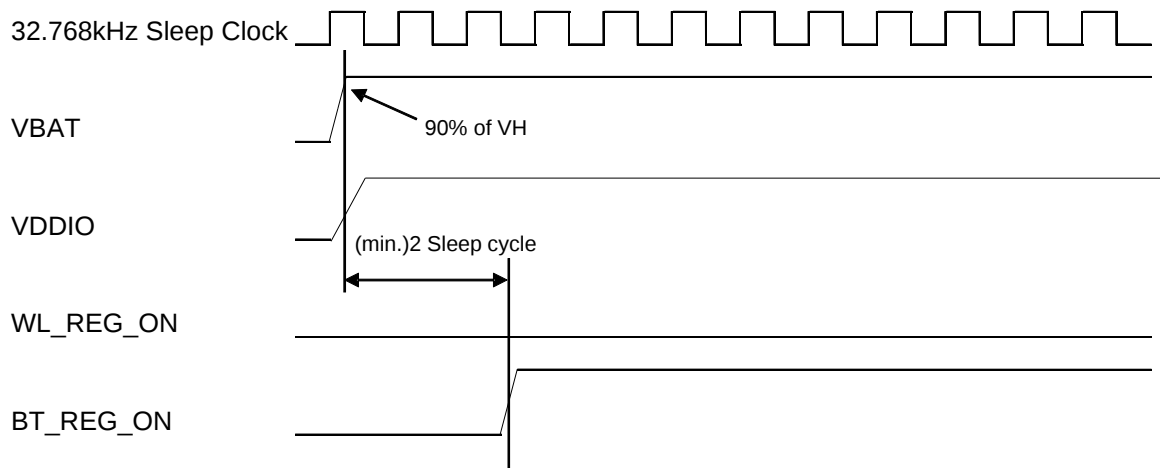
### 8.2. Power Up Sequence for WLAN ON, and BT OFF



Notes:

1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

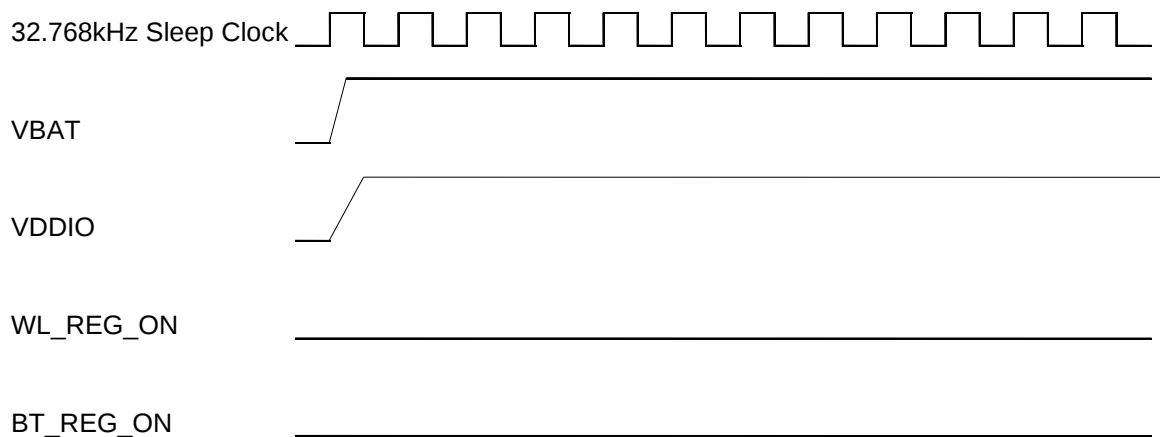
### 8.3. Power Up Sequence for WLAN OFF, and BT ON



Notes:

1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

### 8.4. Power Up Sequence for WLAN OFF, and BT OFF



Notes:

1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 9. Digital I/O Requirements

### 9.1. Digital I/O Pins

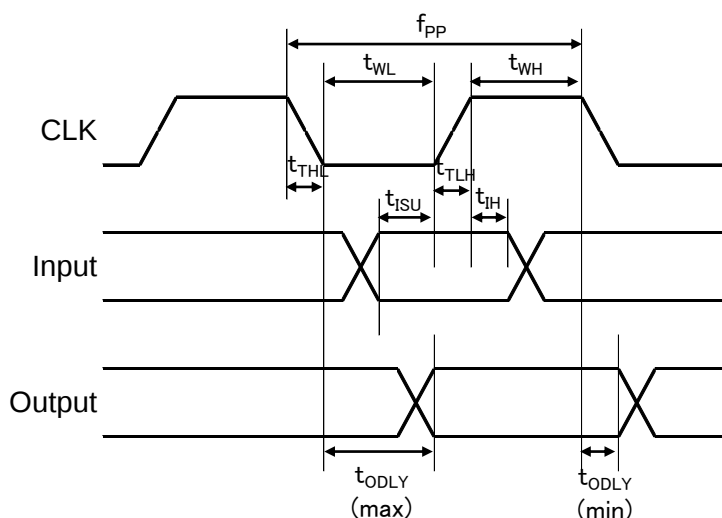
| Digital I/O Pins          | Sym.            | Min.       | Typ. | Max.       | Unit |
|---------------------------|-----------------|------------|------|------------|------|
| For VDDIO = 1.8V:         |                 |            |      |            |      |
| Input high voltage        | V <sub>IH</sub> | 0.65xVDDIO | -    | -          | V    |
| Input low voltage         | V <sub>IL</sub> | -          | -    | 0.35xVDDIO | V    |
| Output high voltage@2.0mA | V <sub>OH</sub> | VDDIO-0.45 | -    | -          | V    |
| Output low voltage@2.0mA  | V <sub>OL</sub> | -          | -    | 0.45       | V    |
| For VDDIO = 3.3V:         |                 |            |      |            |      |
| Input high voltage        | V <sub>IH</sub> | 2.00       | -    | -          | V    |
| Input low voltage         | V <sub>IL</sub> | -          | -    | 0.80       | V    |
| Output high voltage@2.0mA | V <sub>OH</sub> | VDDIO-0.40 | -    | -          | V    |
| Output low voltage@2.0mA  | V <sub>OL</sub> | -          | -    | 0.40       | V    |

### 9.2. RF Switch Control Output Pins

|                           | Sym.             | Min.       | Typ. | Max. | Unit |
|---------------------------|------------------|------------|------|------|------|
| For VDDIO_RF = 3.3V:      |                  |            |      |      |      |
| Output high voltage@2.0mA | V <sub>OH</sub>  | VDDIO-0.40 | -    | -    | V    |
| Output low voltage@2.0mA  | V <sub>OL</sub>  | -          | -    | 0.40 | V    |
| Output capacitance        | C <sub>out</sub> | -          | -    | 5    | pF   |

## 10. Interface Timing

### 10.1. SDIO Timing (Default Mode)



| Parameter                                                                    | Symbol            | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|------------------------------------------------------------------------------|-------------------|--------------------|--------------------|--------------------|------|
| Clock CLK (All values are referred to min. VIH and max. VIL <sup>(2)</sup> ) |                   |                    |                    |                    |      |
| Frequency-Data Transfer Mode                                                 | f <sub>PP</sub>   | 0                  | -                  | 25                 | MHz  |
| Frequency-Identification Mode                                                | f <sub>OD</sub>   | 0                  | -                  | 400                | kHz  |
| Clock Low Time                                                               | t <sub>WL</sub>   | 10                 | -                  | -                  | ns   |
| Clock High Time                                                              | t <sub>WH</sub>   | 10                 | -                  | -                  | ns   |
| Clock Rise Time                                                              | t <sub>TLH</sub>  | -                  | -                  | 10                 | ns   |
| Clock Falling Time                                                           | t <sub>THL</sub>  | -                  | -                  | 10                 | ns   |
| Inputs: CMD, DAT (referenced to CLK)                                         |                   |                    |                    |                    |      |
| Input Setup Time                                                             | t <sub>ISU</sub>  | 5                  | -                  | -                  | ns   |
| Input Hold Time                                                              | t <sub>IH</sub>   | 5                  | -                  | -                  | ns   |
| Outputs: CMD, DAT (referenced to CLK)                                        |                   |                    |                    |                    |      |
| Output Delay time-Data Transfer Mode                                         | t <sub>ODLY</sub> | 0                  | -                  | 14                 | ns   |
| Output Delay time-Identification Mode                                        | t <sub>ODLY</sub> | 0                  | -                  | 50                 | ns   |

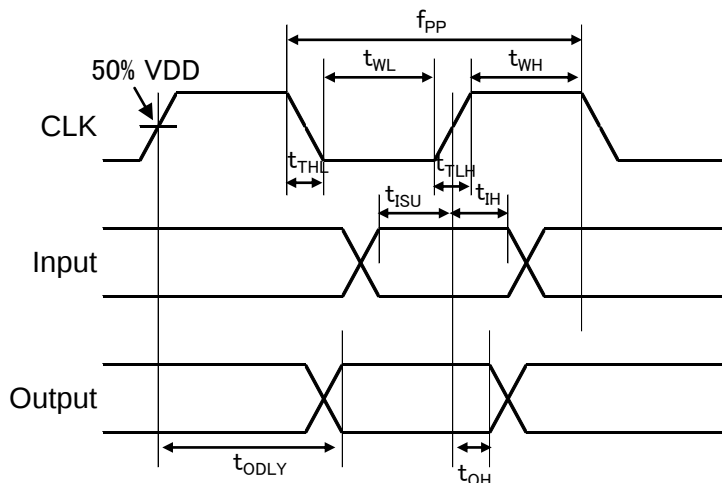
(1). Timing is based on  $CL \leq 40pF$  load on CMD and Data.

(2). Min (V<sub>ih</sub>) = 0.7\*VDDIO and max (V<sub>il</sub>) = 0.2\*VDDIO.

Preliminary

< Specification may be changed by Murata without notice >  
Murata(China) Investment Co., Ltd.

## 10.2. SDIO Timing (High Speed Mode)



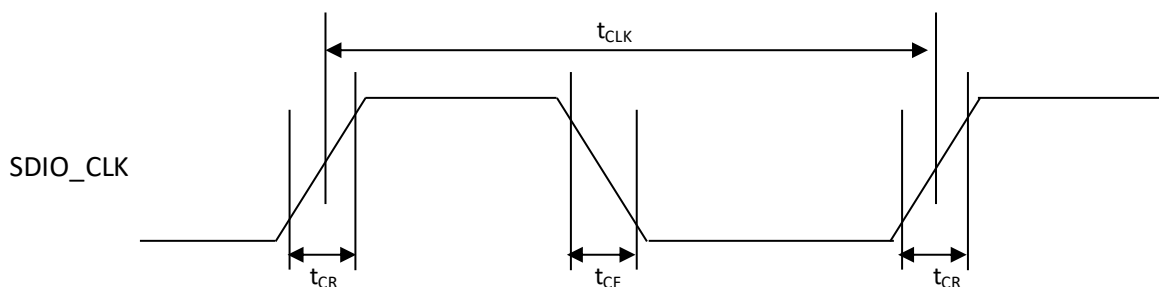
| Parameter                                                                    | Symbol | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|------------------------------------------------------------------------------|--------|--------------------|--------------------|--------------------|------|
| Clock CLK (All values are referred to min. VIH and max. VIL <sup>(2)</sup> ) |        |                    |                    |                    |      |
| Frequency-Data Transfer Mode                                                 | fPP    | 0                  | -                  | 50                 | MHz  |
| Frequency-Identification Mode                                                | fOD    | 0                  | -                  | 400                | kHz  |
| Clock Low Time                                                               | tWL    | 7                  | -                  | -                  | ns   |
| Clock High Time                                                              | tWH    | 7                  | -                  | -                  | ns   |
| Clock Rise Time                                                              | tTLH   | -                  | -                  | 3                  | ns   |
| Clock Falling Time                                                           | tTHL   | -                  | -                  | 3                  | ns   |
| Inputs: CMD, DAT (referenced to CLK)                                         |        |                    |                    |                    |      |
| Input Setup Time                                                             | tISU   | 6                  | -                  | -                  | ns   |
| Input Hold Time                                                              | tIH    | 2                  | -                  | -                  | ns   |
| Outputs: CMD, DAT (referenced to CLK)                                        |        |                    |                    |                    |      |
| Output Delay time-Data Transfer Mode                                         | tODLY  | -                  | -                  | 14                 | ns   |
| Output Hold time                                                             | tOH    | 2.5                | -                  | -                  | ns   |
| Total System Capacitance (each line)                                         | CL     | -                  | -                  | 40                 | pF   |

(1). Timing is based on  $CL \leq 40\text{pF}$  load on CMD and Data.

(2). Min (Vih) =  $0.7 \cdot VDDIO$  and max (Vil) =  $0.2 \cdot VDDIO$ .

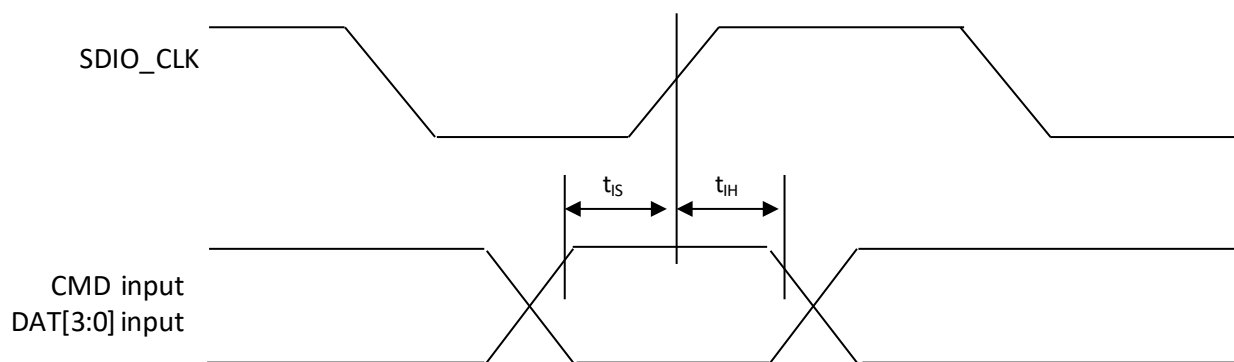
### 10.3. SDIO BUS Timing Specifications in SDR Modes

#### Clock Timing



| Parameter        | Symbol           | Min | Max                  | Unit | Comments                                                                                                                                                                     |
|------------------|------------------|-----|----------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| -                | $t_{CLK}$        | 40  | -                    | ns   | SDR12 mode                                                                                                                                                                   |
|                  |                  | 20  | -                    | ns   | SDR25 mode                                                                                                                                                                   |
|                  |                  | 10  | -                    | ns   | SDR50 mode                                                                                                                                                                   |
|                  |                  | 4.8 | -                    | ns   | SDR104 mode                                                                                                                                                                  |
| -                | $t_{CR}, t_{CF}$ | -   | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 2.00\text{ns}(\text{max})@100\text{MHz}, c\text{CARD}=10\text{pF}$<br>$t_{CR}, t_{CF} < 0.96\text{ns}(\text{max})@208\text{MHz}, c\text{CARD}=10\text{pF}$ |
| Clock duty Cycle | -                | 30  | 70                   | %    | -                                                                                                                                                                            |

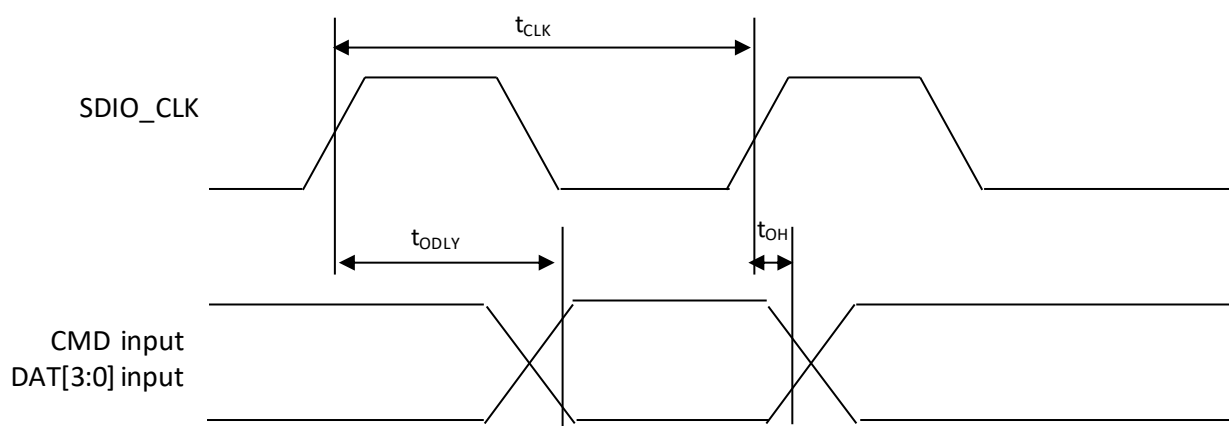
#### Card Input Timing



| Symbol      | Min | Max | Unit | Comments                                             |
|-------------|-----|-----|------|------------------------------------------------------|
| SDR104 Mode |     |     |      |                                                      |
| $t_{IS}$    | 1.4 | -   | ns   | $c\text{CARD} = 10\text{pF}, V_{CT} = 0.975\text{V}$ |
| $t_{IH}$    | 0.8 | -   | ns   | $c\text{CARD} = 5\text{pF}, V_{CT} = 0.975\text{V}$  |
| SDR50 Mode  |     |     |      |                                                      |
| $t_{IS}$    | 3.0 | -   | ns   | $c\text{CARD} = 10\text{pF}, V_{CT} = 0.975\text{V}$ |
| $t_{IH}$    | 0.8 | -   | ns   | $c\text{CARD} = 5\text{pF}, V_{CT} = 0.975\text{V}$  |

## Card Output Timing

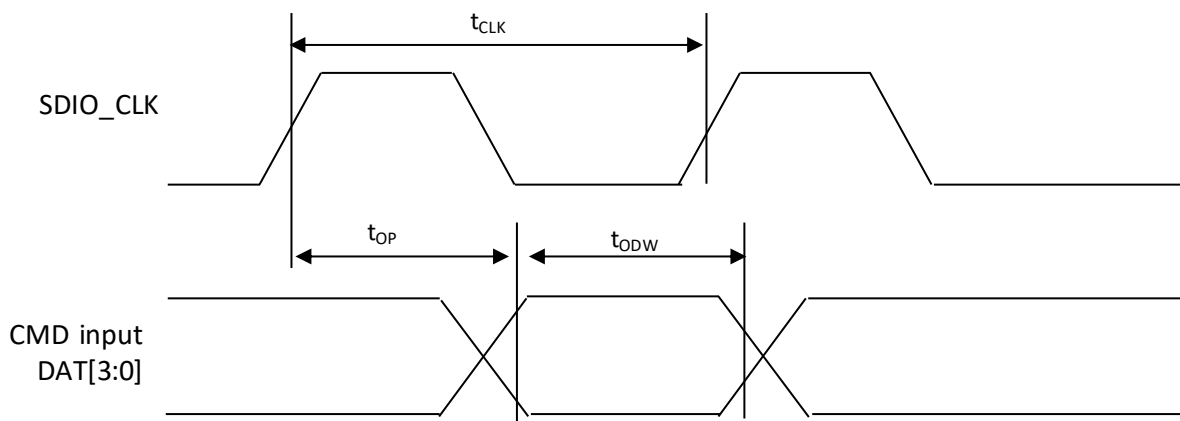
### SDIO Bus Output Timing ( SDR Modes up to 100MHz)



### SDIO Bus Output Timing Parameters ( SDR Modes up to 100MHz)

| Symbol     | Min | Max  | Unit | Comments                                                           |
|------------|-----|------|------|--------------------------------------------------------------------|
| $t_{ODLY}$ | -   | 7.5  | ns   | $t_{CLK} \geq 10\text{ns}$ CL = 30pF using driver type B for SDR50 |
| $t_{ODLY}$ | -   | 14.0 | ns   | $t_{CLK} \geq 20\text{ns}$ CL = 40pF using for SDR12,SDR25         |
| $t_{OH}$   | 1.5 | -    | ns   | Hold time at the $t_{ODLY}(\text{min})$ CL = 15pF                  |

### SDIO Bus Output Timing ( SDR Modes 100MHz to 208MHz)

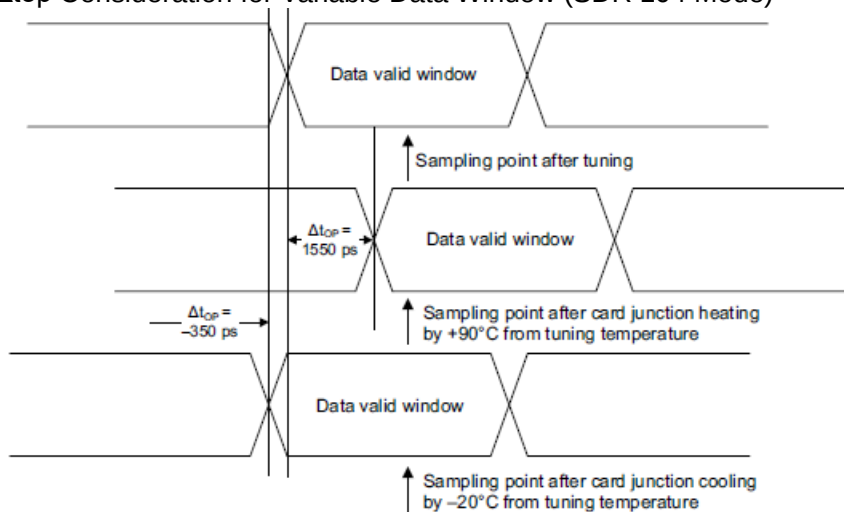


### SDIO Bus Output Timing Parameters ( SDR Modes 100MHz to 208MHz)

| Symbol       | Min  | Max   | Unit | Comments                                        |
|--------------|------|-------|------|-------------------------------------------------|
| tOP          | 0    | 2     | UI   | Card output phase                               |
| $\Delta tOP$ | -350 | +1550 | ps   | Delay variation due to temp change after tuning |
| tODW         | 0.60 | -     | UI   | tODW = 2.88ns @208MHz                           |

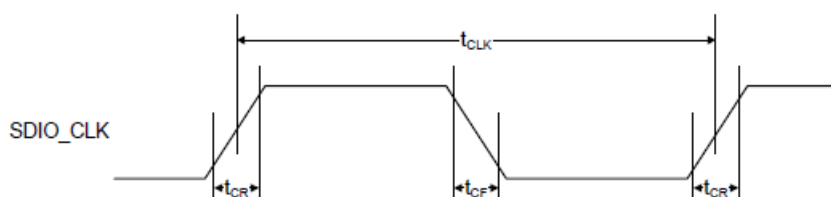
- $\Delta tOP = +1550ps$  for junction temperature of  $\Delta tOP = 90^{\circ}C$  during operation.
- $\Delta tOP = -350ps$  for junction temperature of  $\Delta tOP = -20^{\circ}C$  during operation.
- $\Delta tOP = +2600ps$  for junction temperature of  $\Delta tOP = -20^{\circ}C$  to  $+125^{\circ}C$  during operation

### $\Delta tOP$ Consideration for Variable Data Window (SDR 104 Mode)



#### 10.4. SDIO Timing Specifications in DDR50 Mode

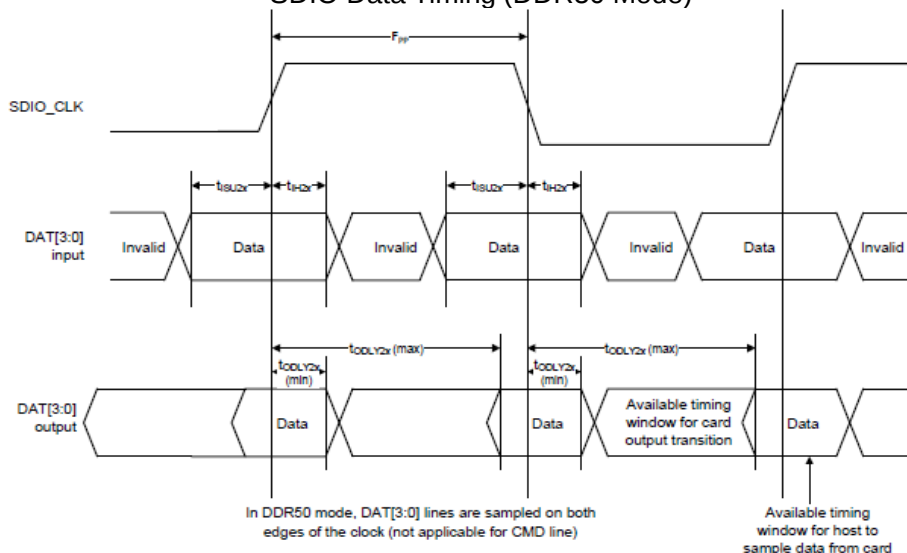
SDIO Clock Timing (DDR50 Mode)



SDIO Bus Clock Timing Parameters (DDR50 Mode)

| Parameter        | Symbol           | Min | Max                  | Unit | Comments                                                                              |
|------------------|------------------|-----|----------------------|------|---------------------------------------------------------------------------------------|
| -                | $t_{CLK}$        | 20  | -                    | ns   | DDr50 mode                                                                            |
| -                | $t_{CR}, t_{CF}$ | -   | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 4.00\text{ns}(\text{max})@50\text{MHz}$ ,<br>$c_{Card}=10\text{pF}$ |
| Clock duty cycle | -                | 45  | 55                   | %    | -                                                                                     |

SDIO Data Timing (DDR50 Mode)



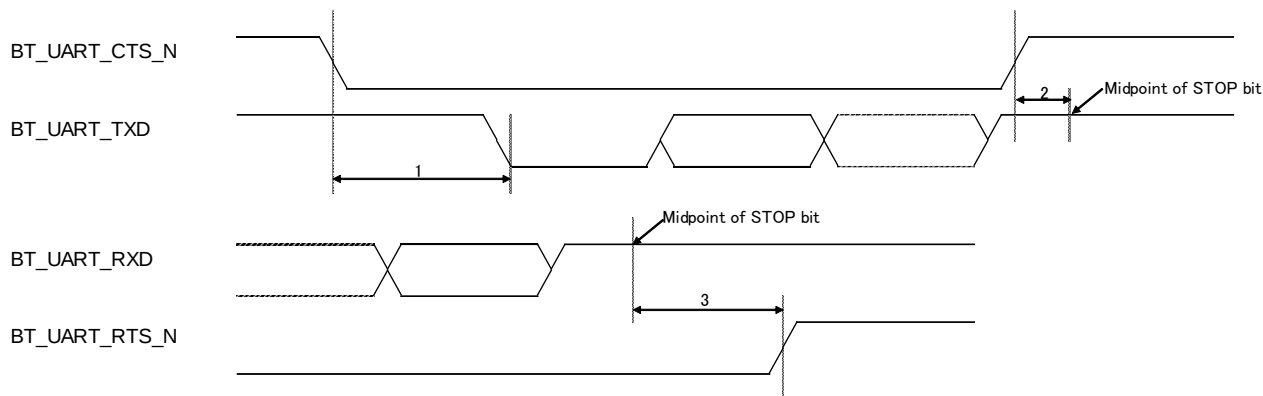
SDIO Bus Timing parameters (DDR50 Mode)

| Parameter         | Symbol       | Min | Max  | Unit | Comments                          |
|-------------------|--------------|-----|------|------|-----------------------------------|
| Input CMD         |              |     |      |      |                                   |
| Input setup time  | $t_{ISU}$    | 6   | -    | ns   | $C_{card} < 10\text{pF}$ (1 card) |
| Input hold time   | $t_{IH}$     | 0.8 | -    | ns   | $C_{card} < 10\text{pF}$ (1 card) |
| Output CMD        |              |     |      |      |                                   |
| Output delay time | $t_{ODLY}$   | -   | 13.7 | ns   | $C_{card} < 30\text{pF}$ (1 card) |
| Output hold time  | $t_{OH}$     | 1.5 | -    | ns   | $C_{card} < 15\text{pF}$ (1 card) |
| Input DAT         |              |     |      |      |                                   |
| Input setup time  | $t_{ISU2x}$  | 3   | -    | ns   | $C_{card} < 10\text{pF}$ (1 card) |
| Input hold time   | $t_{IH2x}$   | 0.8 | -    | ns   | $C_{card} < 10\text{pF}$ (1 card) |
| Output DAT        |              |     |      |      |                                   |
| Output delay time | $t_{ODLY2x}$ | -   | 7.5  | ns   | $C_{card} < 25\text{pF}$ (1 card) |
| Output hold time  | $t_{OH2x}$   | 1.5 | -    | ns   | $C_{card} < 15\text{pF}$ (1 card) |

## 10.5. UART Timing (Default Mode)

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The UART supports the Bluetooth® 4.2 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .



| Reference | Description                                             | Min | Typ | Max | Unit        |
|-----------|---------------------------------------------------------|-----|-----|-----|-------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid            | -   | -   | 1.5 | Bit periods |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit | -   | -   | 0.5 | Bit periods |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high     | -   | -   | 0.5 | Bit periods |

Example of Common Baud Rates

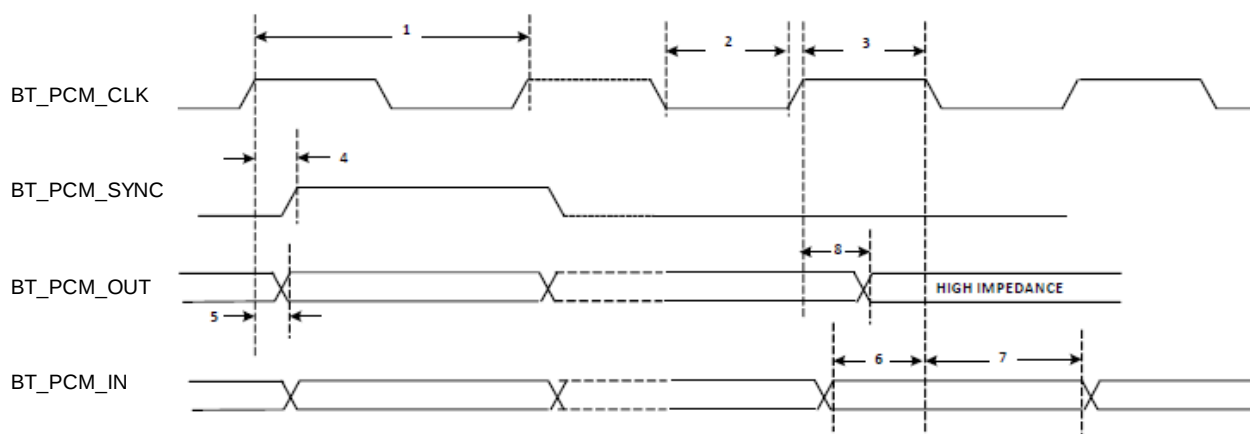
| Desired Rate | Actual Rate set in the module | Error (%) |
|--------------|-------------------------------|-----------|
| 4000000      | 4000000                       | 0.00      |
| 3000000      | 3000000                       | 0.00      |
| 921600       | 923077                        | 0.16      |
| 115200       | 115385                        | 0.16      |
| 57600        | 57692                         | 0.16      |
| 9600         | 9600                          | 0.00      |

## 10.6. Bluetooth® PCM Timing

The PCM Interface can connect to linear PCM Codec devices. In master or slave mode. In master mode, the module generates the PCM\_CLK and PCM\_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the modules.

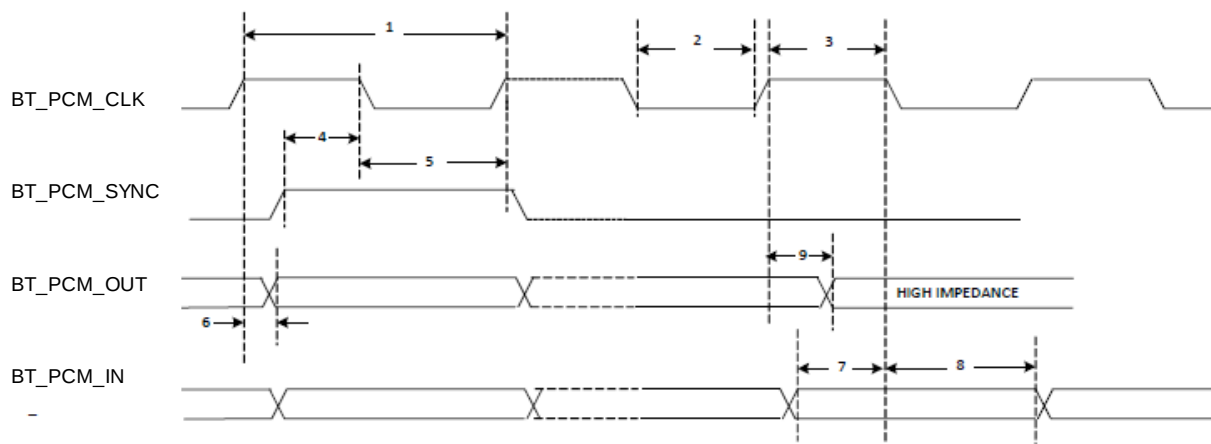
The PCM interface supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

### 10.6.1. Short Frame Sync, Master Mode



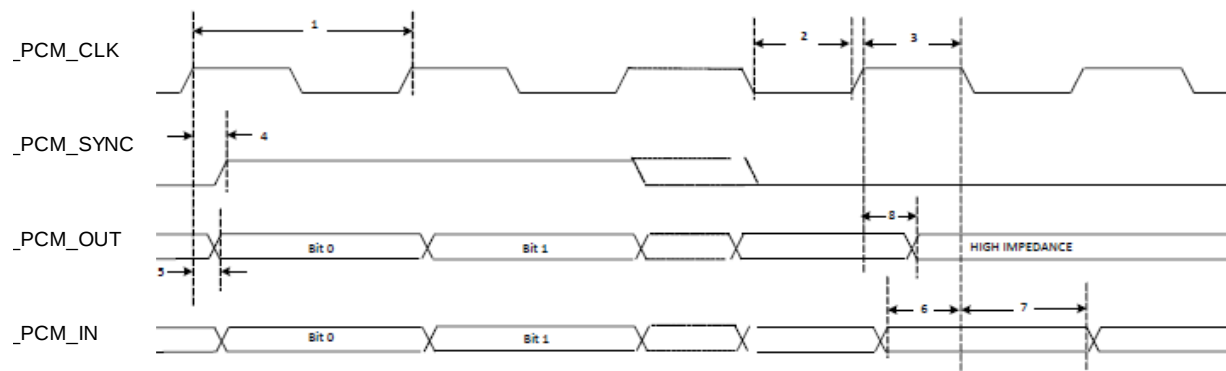
| Reference | Description                                                                                  | Min | Typ | Max | Unit |
|-----------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                      | -   | -   | 12  | MHz  |
| 2         | PCM bit clock High                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock Low                                                                            | 41  | -   | -   | ns   |
| 4         | PCM_SYNC delay                                                                               | 0   | -   | 25  | ns   |
| 5         | PCM_OUT delay                                                                                | 0   | -   | 25  | ns   |
| 6         | PCM_IN setup                                                                                 | 8   | -   | -   | ns   |
| 7         | PCM_IN hold                                                                                  | 8   | -   | -   | ns   |
| 8         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 10.7. Short Frame Sync, Slave Mode



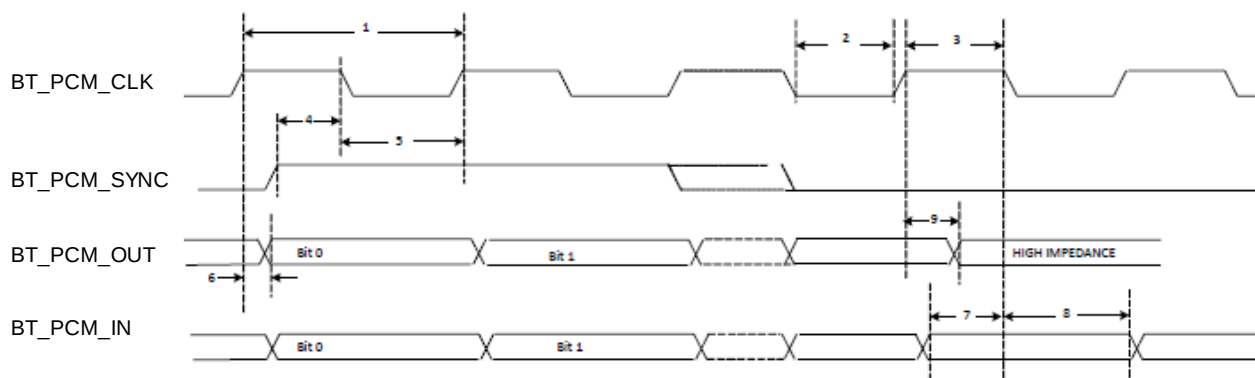
| Reference | Description                                                                                  | Min | Typ | Max | Unit |
|-----------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                      | -   | -   | 12  | MHz  |
| 2         | PCM bit clock Low                                                                            | 41  | -   | -   | ns   |
| 3         | PCM bit clock High                                                                           | 41  | -   | -   | ns   |
| 4         | PCM_SYNC setup                                                                               | 8   | -   | -   | ns   |
| 5         | PCM_SYNC hold                                                                                | 8   | -   | -   | Ns   |
| 6         | PCM_OUT delay                                                                                | 0   | -   | 25  | Ns   |
| 7         | PCM_IN setup                                                                                 | 8   | -   | -   | Ns   |
| 8         | PCM_IN hold                                                                                  | 8   | -   | -   | Ns   |
| 9         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | Ns   |

## 10.8. Long Frame Sync, Master Mode



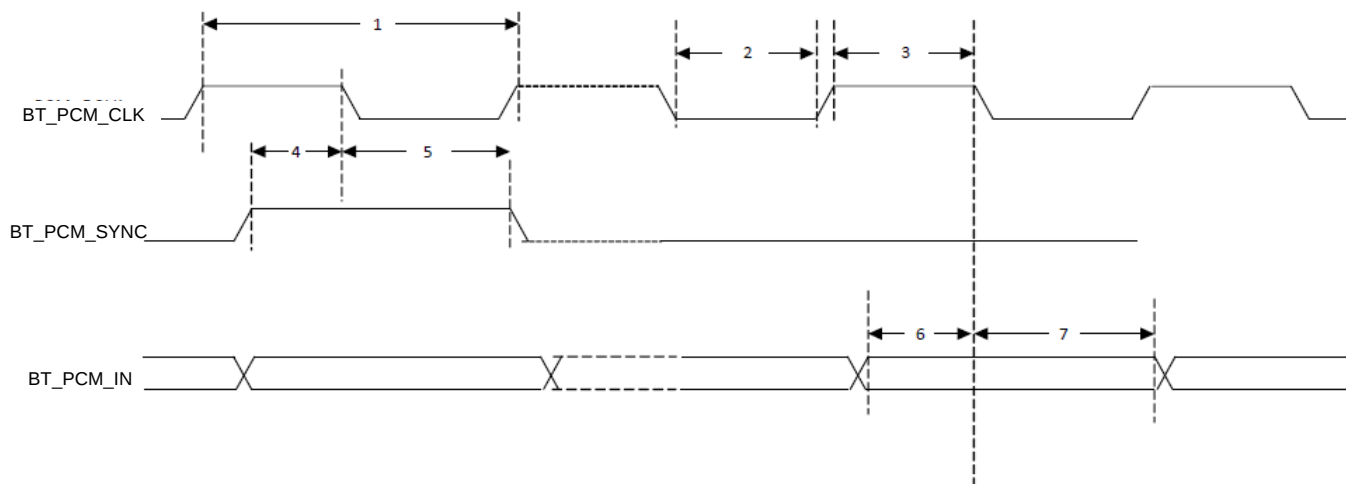
| Reference | Description                                                                                  | Min | Typ | Max | Unit |
|-----------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                      | -   | -   | 12  | MHz  |
| 2         | PCM bit clock High                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock Low                                                                            | 41  | -   | -   | ns   |
| 4         | PCM_SYNC delay                                                                               | 0   | -   | 25  | ns   |
| 5         | PCM_OUT delay                                                                                | 0   | -   | 25  | ns   |
| 6         | PCM_IN setup                                                                                 | 8   | -   | -   | ns   |
| 7         | PCM_IN hold                                                                                  | 8   | -   | -   | ns   |
| 8         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 10.9. Long Frame Sync, Slave Mode



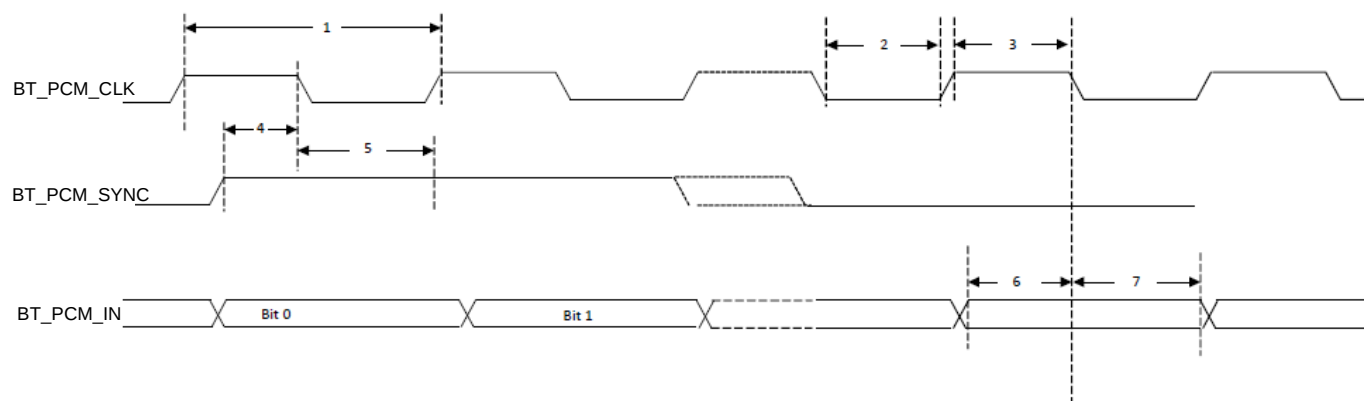
| Reference | Description                                                                                  | Min | Typ | Max | Unit |
|-----------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                      | -   | -   | 12  | MHz  |
| 2         | PCM bit clock High                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock Low                                                                            | 41  | -   | -   | ns   |
| 4         | PCM_SYNC setup                                                                               | 8   | -   | -   | ns   |
| 5         | PCM_SYNC hold                                                                                | 8   | -   | -   | ns   |
| 6         | PCM_OUT delay                                                                                | 0   | -   | 25  | ns   |
| 7         | PCM_IN setup                                                                                 | 8   | -   | -   | ns   |
| 8         | PCM_IN hold                                                                                  | 8   | -   | -   | ns   |
| 9         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

### 10.9.1. Short Frame Sync, Burst Mode



| Reference | Description             | Min  | Typ | Max | Unit |
|-----------|-------------------------|------|-----|-----|------|
| 1         | PCM bit clock frequency | -    | -   | 24  | MHz  |
| 2         | PCM bit clock Low       | 20.8 | -   | -   | ns   |
| 3         | PCM bit clock High      | 20.8 | -   | -   | ns   |
| 4         | PCM_SYNC setup          | 8    | -   | -   | ns   |
| 5         | PCM_SYNC hold           | 8    | -   | -   | ns   |
| 6         | PCM_IN setup            | 8    | -   | -   | ns   |
| 7         | PCM_IN hold             | 8    | -   | -   | ns   |

### 10.9.2. Long Frame Sync, Burst Mode



| Reference | Description             | Min  | Typ | Max | Unit |
|-----------|-------------------------|------|-----|-----|------|
| 1         | PCM bit clock frequency | -    | -   | 24  | MHz  |
| 2         | PCM bit clock Low       | 20.8 | -   | -   | ns   |
| 3         | PCM bit clock High      | 20.8 | -   | -   | ns   |
| 4         | PCM_SYNC setup          | 8    | -   | -   | ns   |
| 5         | PCM_SYNC hold           | 8    | -   | -   | ns   |
| 6         | PCM_IN setup            | 8    | -   | -   | ns   |
| 7         | PCM_IN hold             | 8    | -   | -   | ns   |

## 11. DC / RF Characteristics

ALL DC/RF characteristics are defined by following file.

|                 |                                                                  |
|-----------------|------------------------------------------------------------------|
| WLAN:nvram file | Cyfm4373-sdio.txt                                                |
| BT:hcd file     | 4373A0_Generic_UART_37_4MHz_wlbgA_BU_sLNA_202107091730_0x800.hcd |

### 11.1. DC/RF Characteristics for IEEE802.11b - 2.4GHz

|                   |                   |
|-------------------|-------------------|
| Specification     | IEEE802.11b       |
| Mode              | DSSS / CCK        |
| Channel Frequency | 2412 - 2472MHz    |
| Data rate         | 1, 2, 5.5, 11Mbps |

#### 11.1.1. High Rate Condition for IEEE802.11b – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=17dBm, 11Mbps mode

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
| - DC Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*1                                                                                          |          | 350  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics *1-                                                                                                              | Min.     | Typ. | Max. | Unit |
| 2. Output Power                                                                                                                       | 14.5     | 17   | 19.5 | dBm  |
| 3. Spectrum Mask margin                                                                                                               |          |      |      |      |
| 1) 1st side lobes(-30dBr)                                                                                                             | 0        |      | -    | dB   |
| 2) 2nd side lobes(-50dBr)                                                                                                             | 0        |      | -    | dB   |
| 4. Power-on and Power-down ramp                                                                                                       | -        |      | 2.0  | μsec |
| 5. RF Carrier Suppression                                                                                                             | 15       | -    | -    | dB   |
| 6. Modulation Accuracy (EVM)                                                                                                          | -        |      | 35   | %    |
| 7. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 8. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 9. Minimum Input Level Sensitivity                                                                                                    | -        |      | -76  | dBm  |
| 10. Maximum Input Level (FER ≤ 8%)                                                                                                    | -10      | -    | -    | dBm  |
| 11. Adjacent Channel Rejection<br>(FER ≤ 8%)                                                                                          | 35       | -    | -    | dB   |

\*1: Defined when output power setting is 17dBm at Murata module antenna pad

### 11.1.2. Low Rate Condition for IEEE802.11b – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=17dBm, 1Mbps mode

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
| - DC Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*2                                                                                          |          | 340  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics *2-                                                                                                              | Min.     | Typ. | Max. | Unit |
| 2. Output Power                                                                                                                       | 14.5     | 17   | 19.5 | dBm  |
| 3. Spectrum Mask margin                                                                                                               |          |      |      |      |
| 1) 1st side lobes(-30dBr)                                                                                                             | 0        |      | -    | dB   |
| 2) 2nd side lobes(-50dBr)                                                                                                             | 0        |      | -    | dB   |
| 4. Power-on and Power-down ramp                                                                                                       | -        |      | 2.0  | μsec |
| 5. RF Carrier Suppression                                                                                                             | 15       |      | -    | dB   |
| 6. Modulation Accuracy (EVM)                                                                                                          | -        |      | 35   | %    |
| 7. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 8. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 9. Minimum Input Level Sensitivity                                                                                                    | -        |      | -76  | dBm  |
| 10. Maximum Input Level (FER ≤ 8%)                                                                                                    | -10      | -    | -    | dBm  |
| 11. Adjacent Channel Rejection<br>(FER ≤ 8%)                                                                                          | 35       | -    | -    | dB   |

\*2: Defined when output power setting is 17dBm at Murata module antenna pad

## 11.2. DC/RF Characteristics for IEEE802.11g - 2.4GHz

|                   |                                  |
|-------------------|----------------------------------|
| Specification     | IEEE802.11g                      |
| Mode              | OFDM                             |
| Channel Frequency | 2412 - 2472MHz                   |
| Data rate         | 6, 9, 12, 18, 24, 36, 48, 54Mbps |

### 11.2.1. High Rate Condition for IEEE802.11g – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, 54Mbps mode

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
| - DC Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*3                                                                                          |          | 290  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics*3 -                                                                                                              | Min.     | Typ. | Max. | Unit |
| 2. Output Power                                                                                                                       | 13.5     | 16   | 18.5 | dBm  |
| 3. Spectrum Mask margin                                                                                                               |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                                                                                                          | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)                                                                                                       | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)                                                                                                       | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                                                                                                            | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                                                                                                          | -        |      | -25  | dB   |
| 5. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 6. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | Unit |
| 7. Minimum Input Level Sensitivity                                                                                                    | -        |      | -65  | dBm  |
| 8. Maximum Input Level (PER ≤ 10%)                                                                                                    | -20      | -    | -    | dBm  |
| 9. Adjacent Channel Rejection<br>(PER ≤ 10%)                                                                                          | -1       | -    | -    | dB   |

\*3: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.2.2. Low Rate Condition for IEEE802.11g – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=18dBm, 6Mbps mode

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
| - DC Characteristics -                                                                                                                | Min.     | Typ. | Max. | unit |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*4                                                                                          |          | 310  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics*4 -                                                                                                              | Min.     | Typ. | Max. | unit |
| 2. Output Power                                                                                                                       | 15.5     | 18   | 20.5 | dBm  |
| 3. Spectrum Mask margin                                                                                                               |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                                                                                                          | 0        | -    | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)                                                                                                       | 0        | -    | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)                                                                                                       | 0        | -    | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                                                                                                            | 0        | -    | -    | dB   |
| 4. Constellation Error (EVM)                                                                                                          | -        | -    | -5   | dB   |
| 5. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 6. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | unit |
| 7. Minimum Input Level Sensitivity                                                                                                    | -        | -    | -82  | dBm  |
| 8. Maximum Input Level (PER ≤ 10%)                                                                                                    | -20      | -    | -    | dBm  |
| 9. Adjacent Channel Rejection<br>(PER ≤ 10%)                                                                                          | 16       | -    | -    | dB   |

\*4: Defined when output power setting is 18dBm at Murata module antenna pad

### 11.3. DC/RF Characteristics for IEEE802.11n – 2.4GHz

|                   |                |
|-------------------|----------------|
| Specification     | IEEE802.11n    |
| Mode              | OFDM           |
| Channel Frequency | 2412 - 2472MHz |
| Data rate         | MCS0-MCS7      |

#### 11.3.1. High Rate Condition for IEEE802.11n – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS7

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
|                                                                                                                                       | Min.     | Typ. | Max. | unit |
| - DC Characteristics -                                                                                                                |          |      |      |      |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*5                                                                                          |          | 280  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics*5 -                                                                                                              | Min.     | Typ. | Max. | unit |
| 2. Output Power                                                                                                                       | 11.5     | 14   | 16.5 | dBm  |
| 3. Spectrum Mask                                                                                                                      |          |      |      |      |
| 1) 9MHz to 11MHz (0 ~ -20dBr)                                                                                                         | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20 ~ -28dBr)                                                                                                      | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28 ~ -45dBr)                                                                                                      | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-45dBr)                                                                                                            | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                                                                                                          | -        |      | -27  | dB   |
| 5. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 6. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity                                                                                                    | -        |      | -64  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)                                                                                          | -2       | -    | -    | dB   |

\*5: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.3.2. Low Rate Condition for IEEE802.11n – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, MCS0

| Items                                                                                                                                 | Contents |      |      |      |
|---------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|------|
| - DC Characteristics -                                                                                                                | Min.     | Typ. | Max. | unit |
| 1. DC current                                                                                                                         |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*6                                                                                          |          | 300  |      | mA   |
| 2) Rx mode                                                                                                                            |          | 40   |      | mA   |
| - Tx Characteristics*6 -                                                                                                              | Min.     | Typ. | Max. | unit |
| 2. Output Power                                                                                                                       | 13.5     | 16   | 18.5 | dBm  |
| 3. Spectrum Mask                                                                                                                      |          |      |      |      |
| 1) 9MHz to 11MHz (0 ~ -20dBr)                                                                                                         | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20 ~ -28dBr)                                                                                                      | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28 ~ -45dBr)                                                                                                      | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-45dBr)                                                                                                            | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                                                                                                          | -        |      | -5   | dB   |
| 5. Frequency tolerance                                                                                                                | -20      |      | 20   | ppm  |
| 6. Out band Spurious Emissions                                                                                                        |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)                                                                                                          | -        | -    | -36  | dBm  |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -        | -    | -54  | dBm  |
| 2) 1GHz to 12.75GHz (BW=1MHz)                                                                                                         | -        | -    | -30  | dBm  |
| - Rx Characteristics -                                                                                                                | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity                                                                                                    | -        |      | -82  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)                                                                                          | 16       | -    | -    | dB   |

\*6: Defined when output power setting is 16dBm at Murata module antenna pad

#### 11.4. DC/RF Characteristics for IEEE802.11a - 5GHz

|                   |                                                                             |
|-------------------|-----------------------------------------------------------------------------|
| Specification     | IEEE802.11a                                                                 |
| Mode              | OFDM                                                                        |
| Channel Frequency | 5180 to 5240MHz,<br>5260 to 5320MHz,<br>5500 to 5720MHz,<br>5745 to 5825MHz |
| Data rate         | 6, 9, 12, 18, 24, 36, 48, 54Mbps                                            |

##### 11.4.1. High Rate Condition for IEEE802.11a – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, 54Mbps

| Items                                        | Contents |      |      |      |
|----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                       | Min.     | Typ. | Max. | unit |
| 1. DC current                                |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*7 |          | 290  |      | mA   |
| 2) Rx mode                                   |          | 60   |      | mA   |
| - Tx Characteristics*7 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                              | 12       | 14   | 16   | dBm  |
| 3. Spectrum Mask                             |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)              | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)              | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                   | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                 | -        |      | -25  | dB   |
| 5. Frequency tolerance                       | -20      |      | 20   | ppm  |
| - Rx Characteristics -                       | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity           | -        | .    | -65  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%) | -1       | -    | -    | dB   |

\*7: Defined when output power setting is 14dBm at Murata module antenna pad

#### 11.4.2. Low Rate Condition for IEEE802.11a – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, 6Mbps

| Items                                        | Contents |      |      |      |
|----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                       | Min.     | Typ. | Max. | unit |
| 1. DC current                                |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*8 |          | 310  |      | mA   |
| 2) Rx mode                                   |          | 60   |      | mA   |
| - Tx Characteristics*8 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                              | 14       | 16   | 18   | dBm  |
| 3. Spectrum Mask                             |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)              | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)              | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                   | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                 | -        |      | -5   | dB   |
| 5. Frequency tolerance                       | -20      |      | 20   | ppm  |
| - Rx Characteristics -                       | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity           | -        |      | -82  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%) | 16       | -    | -    | dB   |

\*8: Defined when output power setting is 16dBm at Murata module antenna pad

#### 11.5. DC/RF Characteristics for IEEE802.11n(HT20) - 5GHz

|               |                |
|---------------|----------------|
| Specification | IEEE802.11n    |
| Mode          | OFDM           |
| Frequency     | 5180 - 5825MHz |
| Data rate     | MCS0-MCS7      |

#### 11.5.1. High Rate Condition for IEEE802.11n(HT20) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS7

| Items                                        | Contents |      |      |      |
|----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                       | Min.     | Typ. | Max. | unit |
| 1. DC current                                |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*9 |          | 280  |      | mA   |
| 2) Rx mode                                   |          | 70   |      | mA   |
| - Tx Characteristics*9 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                              | 12       | 14   | 16   | dBm  |
| 3. Spectrum Mask                             |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)              | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)              | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                   | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                 | -        |      | -27  | dB   |
| 5. Frequency tolerance                       | -20      |      | 20   | ppm  |
| - Rx Characteristics -                       | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity           | -        |      | -64  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%) | -2       | -    | -    | dB   |

\*9: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.5.2. Low Rate Condition for IEEE802.11n(HT20) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, MCS0

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*10 |          | 300  |      | mA   |
| 2) Rx mode                                    |          | 60   |      | mA   |
| - Tx Characteristics*10 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 14       | 16   | 18   | dBm  |
| 3. Spectrum Mask                              |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                  | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)               | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -5   | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -82  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | 16       | -    | -    | dB   |

\*10: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.6. DC/RF Characteristics for IEEE802.11ac(HT20) - 5GHz

|               |                |
|---------------|----------------|
| Specification | IEEE802.11ac   |
| Mode          | OFDM           |
| Frequency     | 5180 - 5825MHz |
| Data rate     | MCS0-MCS8      |

#### 11.6.1. High Rate Condition for IEEE802.11ac(VHT20) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=13dBm, MCS8

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*11 |          | 280  |      | mA   |
| 2) Rx mode                                    |          | 60   |      | mA   |
| - Tx Characteristics*11 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 11       | 13   | 15   | dBm  |
| 3. Spectrum Mask                              |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                  | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)               | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -30  | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -59  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | -7       | -    | -    | dB   |

\*11: Defined when output power setting is 13dBm at Murata module antenna pad

### 11.6.2. Low Rate Condition for IEEE802.11ac(VHT20) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, MCS0

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*12 |          | 300  |      | mA   |
| 2) Rx mode                                    |          | 60   |      | mA   |
| - Tx Characteristics*12 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 14       | 16   | 18   | dBm  |
| 3. Spectrum Mask                              |          |      |      |      |
| 1) 9MHz to 11MHz (0~ -20dBr)                  | 0        |      | -    | dB   |
| 2) 11MHz to 20MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 20MHz to 30MHz (-28~ -40dBr)               | 0        |      | -    | dB   |
| 4) 30MHz to 33MHz (-40dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -5   | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -82  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | 16       | -    | -    | dB   |

\*12: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.7. DC/RF Characteristics for IEEE802.11n(HT 40MHz) - 5GHz

|                   |                 |
|-------------------|-----------------|
| Specification     | IEEE802.11n     |
| Mode              | OFDM            |
| Channel Frequency | 5190 to 5795MHz |
| Data rate         | MCS0-MCS7       |

#### 11.7.1. High Rate Condition for IEEE802.11n(HT40) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=13dBm, MCS7, HT 40MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*13 |          | 320  |      | mA   |
| 2) Rx mode                                    |          | 70   |      | mA   |
| - Tx Characteristics*13 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 11       | 13   | 15   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 19MHz to 21MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 21MHz to 40MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 40MHz to 60MHz (-28~ -45dBr)               | 0        |      | -    | dB   |
| 4) 60MHz to 80MHz (-45dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -27  | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -61  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | -2       | -    | -    | dB   |

\*13: Defined when output power setting is 13dBm at Murata module antenna pad

### 11.7.2. Low Rate Condition for IEEE802.11n(HT40) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS0, HT 40MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*14 |          | 350  |      | mA   |
| 2) Rx mode                                    |          | 70   |      | mA   |
| - Tx Characteristics*14 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 12       | 14   | 16   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 19MHz to 21MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 21MHz to 40MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 40MHz to 60MHz (-28~ -45dBr)               | 0        |      | -    | dB   |
| 4) 60MHz to 80MHz (-45dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -5   | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -79  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | 16       | -    | -    | dB   |

\*14: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.8. DC/RF Characteristics for IEEE802.11ac(VHT 40MHz) - 5GHz

|                   |                 |
|-------------------|-----------------|
| Specification     | IEEE802.11ac    |
| Mode              | OFDM            |
| Channel Frequency | 5190 to 5795MHz |
| Data rate         | MCS0-MCS9       |

#### 11.8.1. High Rate Condition for IEEE802.11ac(VHT40) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=11dBm, MCS9, VHT 40MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*15 |          | 320  |      | mA   |
| 2) Rx mode                                    |          | 70   |      | mA   |
| - Tx Characteristics*15 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 9        | 11   | 13   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 19MHz to 21MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 21MHz to 40MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 40MHz to 60MHz (-28~ -45dBr)               | 0        |      | -    | dB   |
| 4) 60MHz to 80MHz (-45dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -32  | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -54  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | -9       | -    | -    | dB   |

\*15: Defined when output power setting is 11dBm at Murata module antenna pad

### 11.8.2. Low Rate Condition for IEEE802.11ac(VHT40) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS0, VHT 40MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*16 |          | 350  |      | mA   |
| 2) Rx mode                                    |          | 70   |      | mA   |
| - Tx Characteristics*16 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 12       | 14   | 16   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 19MHz to 21MHz (0~ -20dBr)                 | 0        |      | -    | dB   |
| 2) 21MHz to 40MHz (-20~ -28dBr)               | 0        |      | -    | dB   |
| 3) 40MHz to 60MHz (-28~ -45dBr)               | 0        |      | -    | dB   |
| 4) 60MHz to 80MHz (-45dBr)                    | 0        |      | -    | dB   |
| 4. Constellation Error (EVM)                  | -        |      | -5   | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -54  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | 16       | -    | -    | dB   |

\*16: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.9. DC/RF Characteristics for IEEE802.11ac(VHT 80MHz) - 5GHz

|                   |                    |
|-------------------|--------------------|
| Specification     | IEEE802.11ac       |
| Mode              | OFDM               |
| Channel Frequency | 5210MHz to 5775MHz |
| Data rate         | MCS0-MCS9          |

### 11.9.1. High Rate Condition for IEEE802.11ac(VHT80) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=12dBm, MCS9, VHT 80MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*17 |          | 340  |      | mA   |
| 2) Rx mode                                    |          | 90   |      | mA   |
| - Tx Characteristics*17 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 9        | 11   | 13   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 39MHz to 41MHz (0~ -20dBr)                 | 0        |      |      | dB   |
| 2) 41MHz to 80MHz (-20~ -28dBr)               | 0        |      |      | dB   |
| 3) 80MHz to 120MHz (-28~ -40dBr)              | 0        |      |      | dB   |
| 4) 120MHz to 140MHz (-40dBr)                  | 0        |      |      | dB   |
| 4. Constellation Error                        | -        |      | -32  | dB   |
| 5. Frequency tolerance                        | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -51  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | -9       | -    | -    | dB   |

\*17: Defined when output power setting is 11dBm at Murata module antenna pad

### 11.9.2. Low Rate Condition for IEEE802.11ac(VHT80) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=13dBm, MCS0,VHT 80MHz

| Items                                         | Contents |      |      |      |
|-----------------------------------------------|----------|------|------|------|
| - DC Characteristics -                        | Min.     | Typ. | Max. | unit |
| 1. DC current                                 |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval)<br>*18 |          | 380  |      | mA   |
| 2) Rx mode                                    |          | 90   |      | mA   |
| - Tx Characteristics*18 -                     | Min.     | Typ. | Max. | unit |
| 2. Output Power                               | 11       | 13   | 15   | dBm  |
| 3. Spectrum Mask margin                       |          |      |      |      |
| 1) 39MHz to 41MHz (0~ -20dBr)                 | 0        |      |      | dB   |
| 2) 41MHz to 80MHz (-20~ -28dBr)               | 0        |      |      | dB   |
| 3) 80MHz to 120MHz (-28~ -40dBr)              | 0        |      |      | dB   |
| 4) 120MHz to 140MHz (-40dBr)                  | 0        |      |      | dB   |
| 4. Constellation Error                        | -        |      | -5   | dB   |
| 5.Frequency tolerance                         | -20      |      | 20   | ppm  |
| - Rx Characteristics -                        | Min.     | Typ. | Max. | unit |
| 6. Minimum Input Level Sensitivity            | -        |      | -76  | dBm  |
| 7. Adjacent Channel Rejection<br>(PER ≤ 10%)  | 16       | -    | -    | dB   |

\*18: Defined when output power setting is 13dBm at Murata module antenna pad

### 11.10. DC/RF Characteristics for Bluetooth®

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V

| Items                                                                                                                                 | Contents                |      |        |          |
|---------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------|--------|----------|
| Bluetooth® specification (power class)                                                                                                | Version 5.2             |      |        |          |
| Channel frequency (spacing)                                                                                                           | 2402 to 2480 MHz (1MHz) |      |        |          |
| Current Consumption                                                                                                                   | Min.                    | Typ. | Max.   | unit     |
| (a) Tx=Rx=DH5 (fully occupied)                                                                                                        | -                       | 55   |        | mA       |
| (b) Tx=Rx=2DH5 (fully occupied)                                                                                                       | -                       | 45   |        | mA       |
| (c) Tx=Rx=3DH5 (fully occupied)                                                                                                       | -                       | 45   |        | mA       |
| Transmitter                                                                                                                           | Min.                    | Typ. | Max.   | Unit     |
| Output Power@DH5                                                                                                                      | 6                       | 10   | 14     | dBm      |
| Frequency range                                                                                                                       | 2400                    | -    | 2483.5 | MHz      |
| 20dB bandwidth                                                                                                                        | -                       |      | 1      | MHz      |
| Adjacent Channel Power *1                                                                                                             |                         |      |        |          |
| (a) [M-N] =2                                                                                                                          | -                       | -    | -20    | dBm      |
| (b) [M-N] ≥3                                                                                                                          | -                       | -    | -40    | dBm      |
| Modulation characteristics                                                                                                            |                         |      |        |          |
| (a) Modulation Δf1avg                                                                                                                 | 140                     |      | 175    | kHz      |
| (b) Modulation Δf2max                                                                                                                 | 115                     |      | -      | kHz      |
| (c) Modulation Δf2avg / Δf1avg                                                                                                        | 0.8                     | 1    | -      |          |
| Carrier Frequency Drift                                                                                                               |                         |      |        |          |
| (a) 1slot                                                                                                                             | -25                     | -    | 25     | kHz      |
| (b) 3slot / 5slot                                                                                                                     | -40                     | -    | 40     | kHz      |
| (c) Maximum drift rate                                                                                                                |                         | -    | 20     | kHz/50us |
| EDR Relative Power                                                                                                                    | -4                      | -    | 1      | dB       |
| EDR Carrier Frequency Stability and Modulation Accuracy                                                                               |                         |      |        |          |
| (a) ωi                                                                                                                                | -75                     | -    | 75     | kHz      |
| (b) ωi+ωo                                                                                                                             | -75                     | -    | 75     | kHz      |
| (c) ωo                                                                                                                                | -10                     | -    | 10     | kHz      |
| (d) RMS DEVM (DQPSK)                                                                                                                  | -                       | -    | 20     | %        |
| (e) Peak DEVM (DQPSK)                                                                                                                 | -                       | -    | 35     | %        |
| (f) 99% DEVM (DQPSK)                                                                                                                  | -                       | -    | 30     | %        |
| (g) RMS DEVM (8DPSK)                                                                                                                  | -                       | -    | 13     | %        |
| (h) Peak DEVM (8DPSK)                                                                                                                 | -                       | -    | 25     | %        |
| (i) 99% DEVM (8DPSK)                                                                                                                  | -                       | -    | 20     | %        |
| Spurious Emissions                                                                                                                    |                         |      |        |          |
| (a) 30MHz to 1GHz (BW=100kHz)                                                                                                         | -                       | -    | -36    | dBm      |
| annotation<br>47MHz to 74MHz(BW=100kHz)<br>87.5MHz to 118MHz(BW=100kHz)<br>174MHz to 230MHz(BW=100kHz)<br>470MHz to 862MHz(BW=100kHz) | -                       | -    | -54    | dBm      |
| (b) 1GHz to 12.75GHz (BW=1MHz)                                                                                                        | -                       | -    | -30    | dBm      |
| Receiver                                                                                                                              | Min.                    | Typ. | Max.   | unit     |
| BDR Sensitivity (BER≤0.1%)                                                                                                            | -                       |      | -80    | dBm      |
| EDR Sensitivity (BER≤0.007%)@8DPSK                                                                                                    | -                       |      | -77    | dBm      |
| C/I Performance (BER≤0.1%) *2                                                                                                         |                         |      |        |          |
| (a) co-channel                                                                                                                        | -                       | -    | 11     | dB       |
| (b) 1MHz                                                                                                                              | -                       | -    | 0      | dB       |
| (c) 2MHz                                                                                                                              | -                       | -    | -30    | dB       |
| (d) 3MHz                                                                                                                              | -                       | -    | -40    | dB       |
| (e) image (+4MHz)                                                                                                                     | -                       | -    | -9     | dB       |
| (f) image +/- 1MHz                                                                                                                    | -                       | -    | -20    | dB       |
| Maximum Input Level (BER≤0.1%)                                                                                                        | -20                     | -    | -      | dBm      |

\*1: Up to three spurious responses within Bluetooth® limits are allowed.

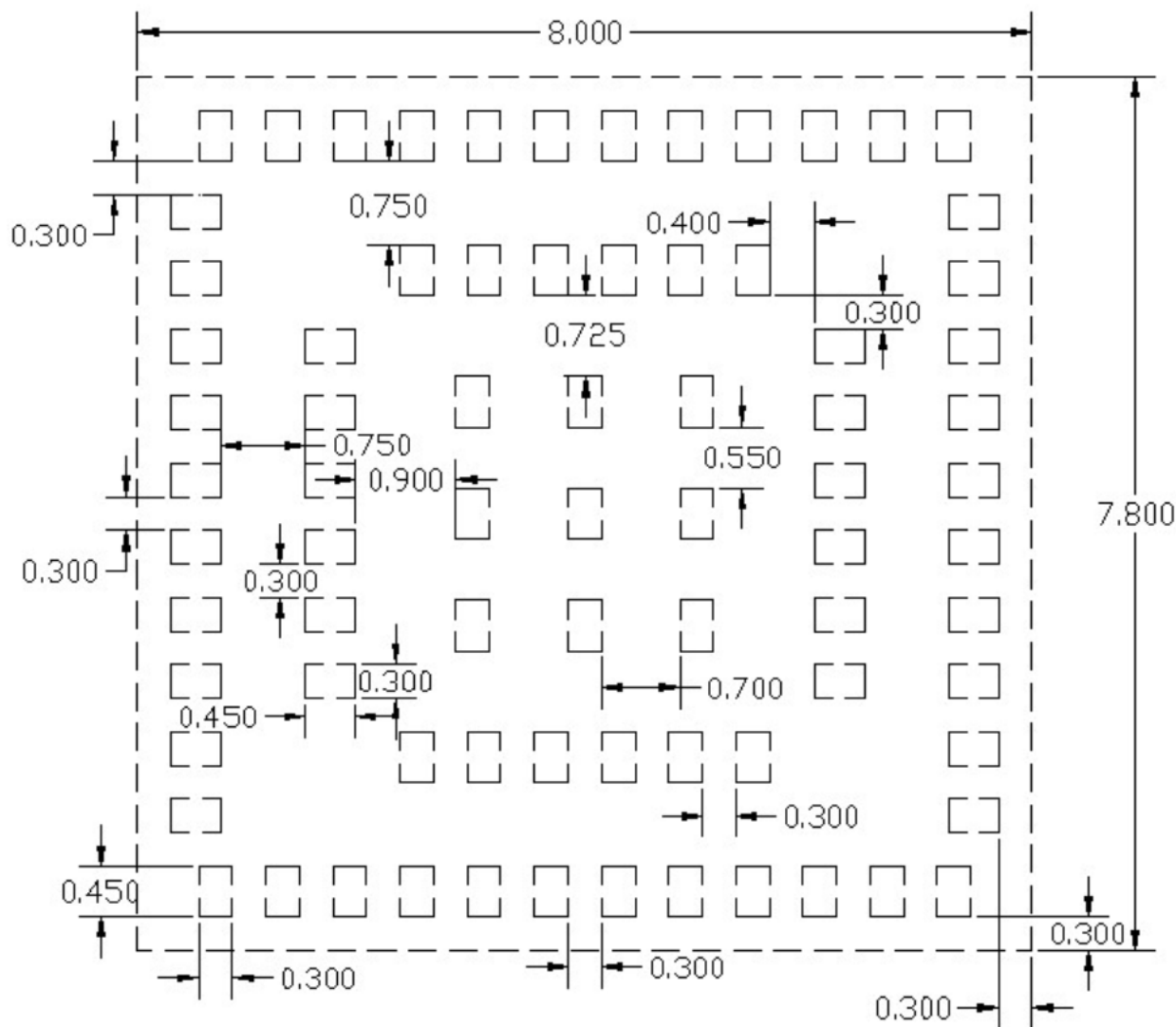
\*2: Up to five spurious responses within Bluetooth® limits are allowed.

### 11.11. DC/RF Characteristics for Bluetooth® (LE)

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V

| Items                                                | Contents                |      |      |      |
|------------------------------------------------------|-------------------------|------|------|------|
| Bluetooth® specification (power class)               | Version 5.2(LE)         |      |      |      |
| Channel frequency (spacing)                          | 2402 to 2480 MHz (2MHz) |      |      |      |
| Number of RF Channel                                 | 40                      |      |      |      |
| Item / Condition                                     | Min.                    | Typ. | Max. | Unit |
| Center Frequency                                     | 2402                    | -    | 2480 | MHz  |
| Channel Spacing                                      | -                       | 2    | -    | MHz  |
| Number of RF channel                                 | -                       | 40   | -    | -    |
| Output power                                         | -                       | 8    | -    | dBm  |
| Modulation Characteristics                           |                         |      |      |      |
| 1) $\Delta f_{1\text{avg}}$                          | 225                     | -    | 275  | kHz  |
| 2) $\Delta f_{2\text{max}}$ (at 99.9%)               | 185                     | -    | -    | kHz  |
| 3) $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                     | -    | -    | -    |
| Carrier frequency offset and drift                   |                         |      |      |      |
| 1) Frequency offset                                  | -                       | -    | 150  | kHz  |
| 2) Frequency drift                                   | -                       | -    | 50   | kHz  |
| 3) Drift rate                                        | -                       | -    | 20   | kHz  |
| Receiver sensitivity (PER < 30.8%)                   | -                       | -    | -70  | dBm  |
| Maximum input signal level (PER < 30.8%)             | -10                     | -    | -    | dBm  |
| PER Report Integrity (-30dBm input)                  | 50                      | -    | 65.4 | %    |

## 12. Land Patterns



(unit : mm)

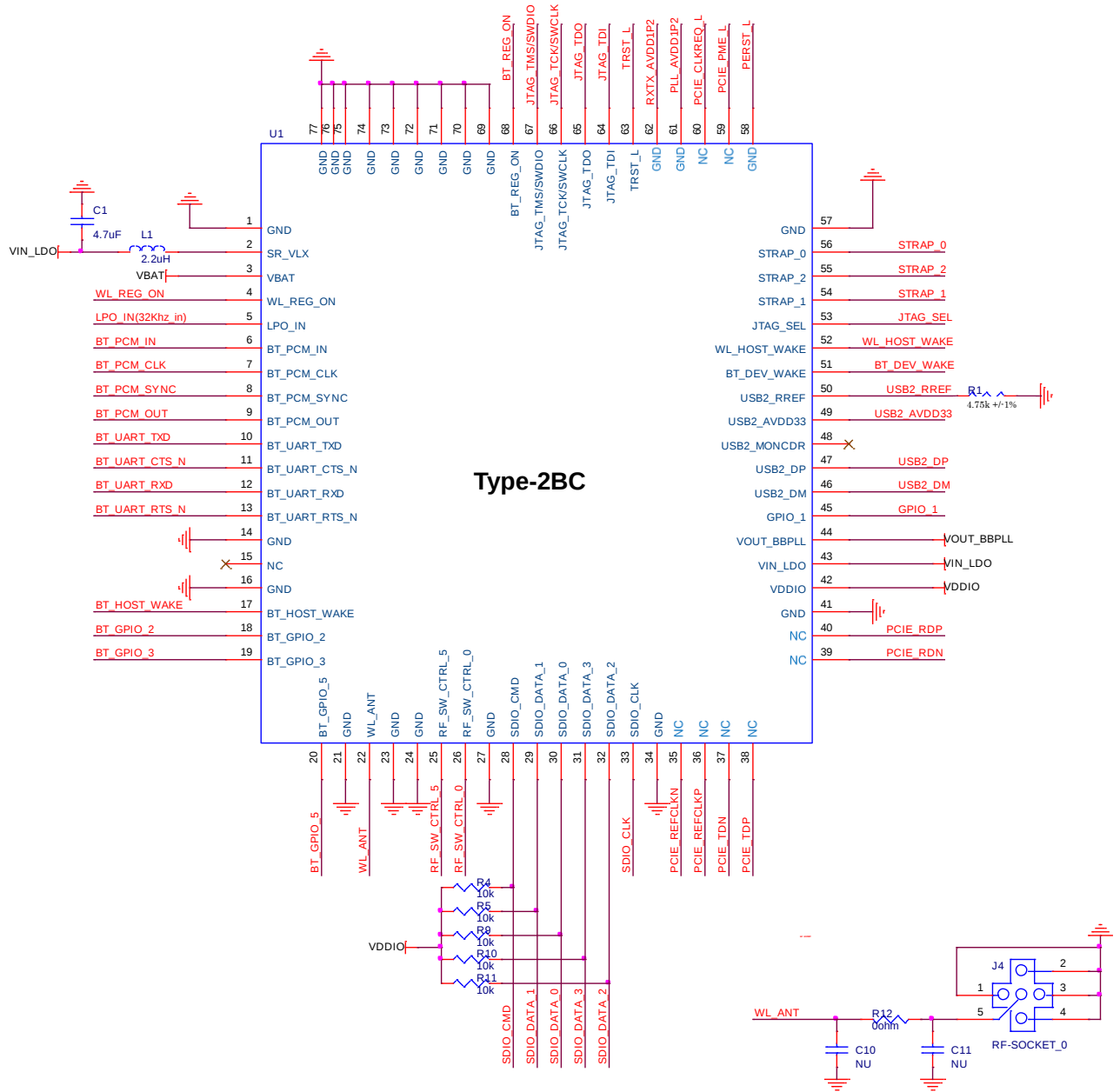
Note:

This land pattern is for reference purpose only.

Consult your manufacturing group to ensure your company's manufacturing guidelines are met.

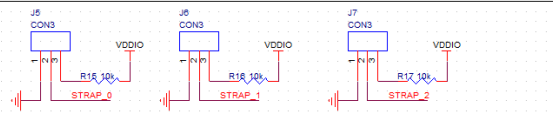
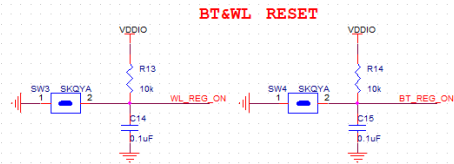
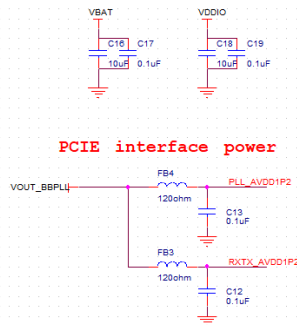
## 13. Reference Circuit

Module



## Power supply and configuration

- 1.VBAT typical value is 3.3 +/-5% V
- 2.VDDIO can be provided 1.8V or 3.3V
- 3.LFO\_IN must be provided
- 4.For LI selection, recommended inductor P/N is DFE201612E-2R2M(muRata)
- 5.JTAG\_SEL must be kept connect to ground if the JTAG interface is not used.
- It must be high to select SWD OR JTAG

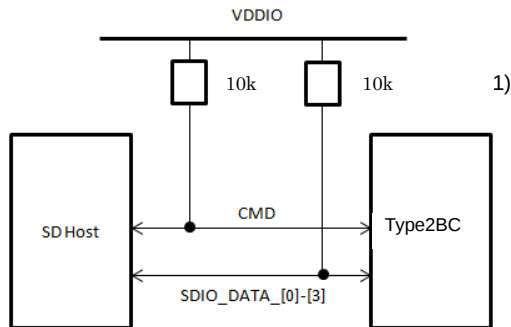


**Strapping options**

| Mode Selected | Strap_2 | Strap_1 | Strap_0 | J7             | J6             | J5             |
|---------------|---------|---------|---------|----------------|----------------|----------------|
| SDIO 3.3V     | 1       | 0       | 0       | Jump on Pin2,3 | Jump on Pin1,2 | Jump on Pin1,2 |
| SDIO 1.8V     | 1       | 0       | 1       | Jump on Pin2,3 | Jump on Pin1,2 | Jump on Pin2,3 |
| USB           | 0       | 0       | 0       | Jump on Pin1,2 | Jump on Pin1,2 | Jump on Pin1,2 |

### \*1) SDIO Pull-UP Requirements

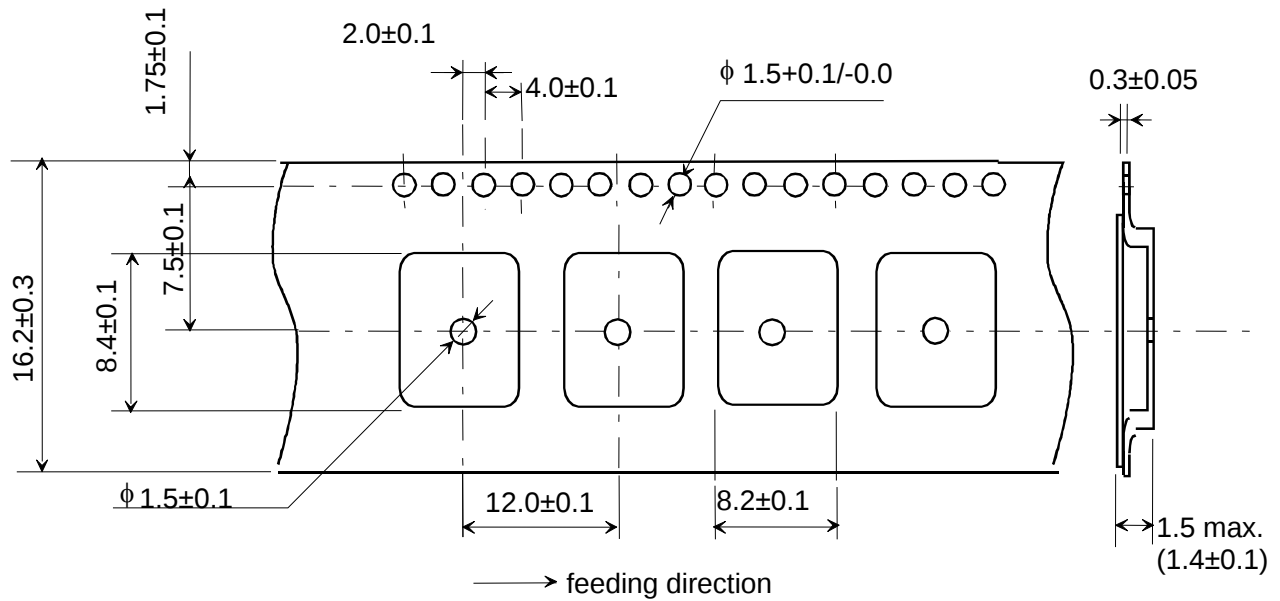
10 to 100k ohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO Host pull-ups. The CYW4373 module (LBEE5PK2BC-771) does not have internal pull-ups on these lines.



## 14. Tape and Reel Packing

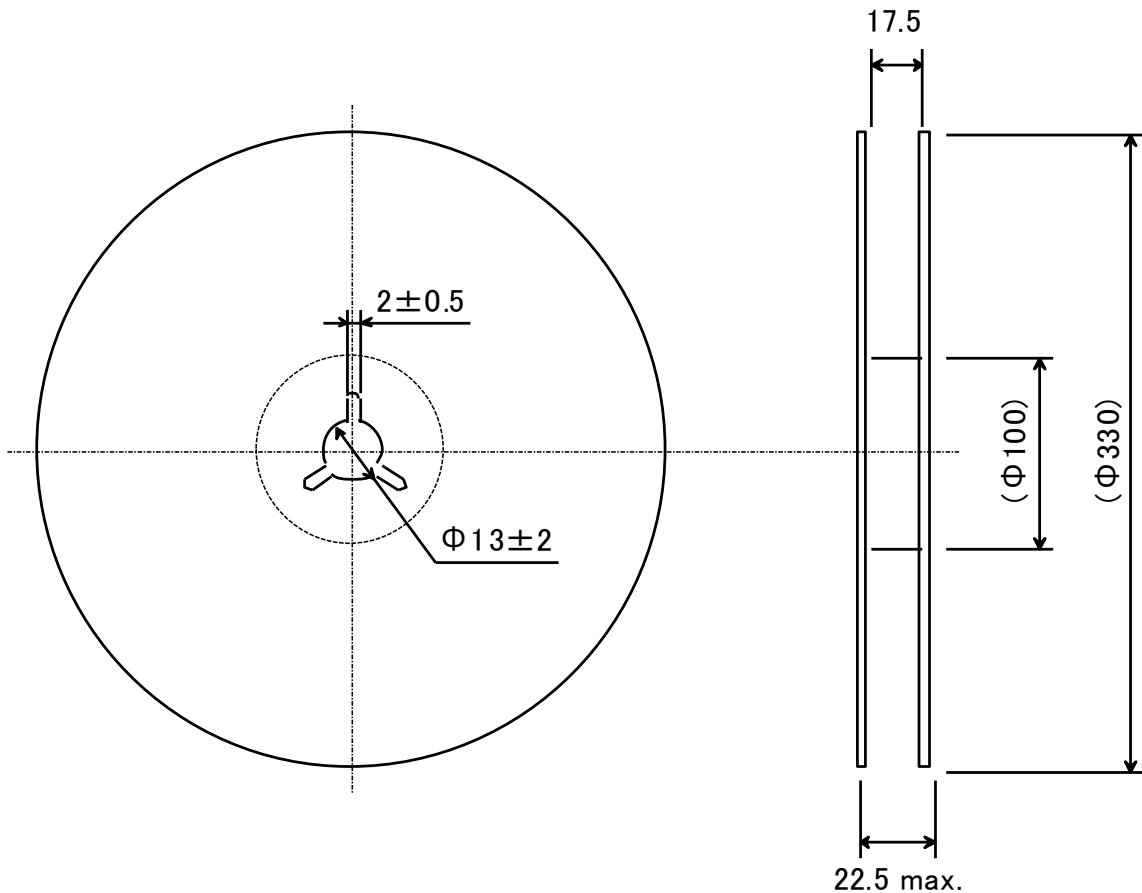
### (1) Dimensions of Tape (Plastic tape)

\*1. Cumulative tolerance of max.  $40.0 \pm 0.15$  every 10 pitches



(Unit : mm)

### (2) Dimensions of Reel



(unit : mm)

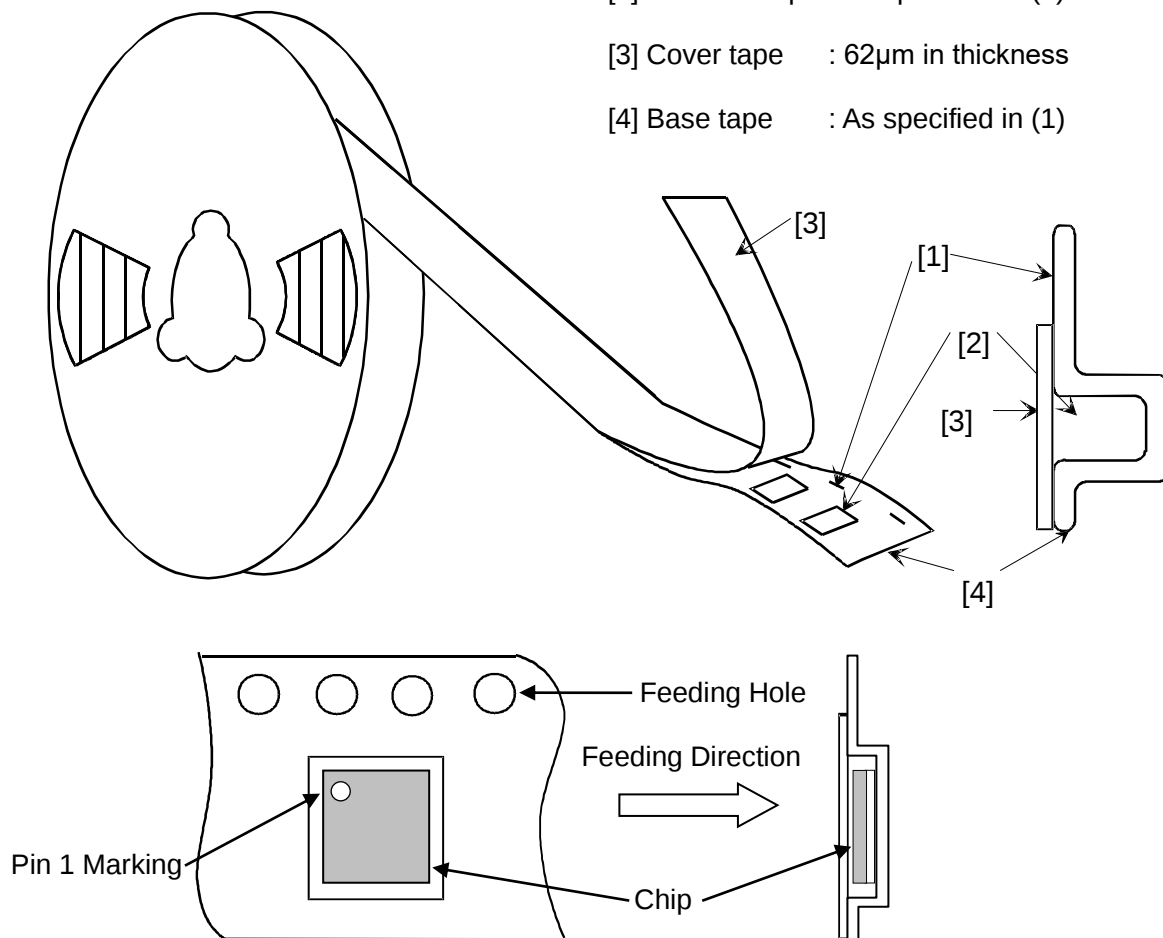
### (3) Taping Diagrams

[1] Feeding Hole : As specified in (1)

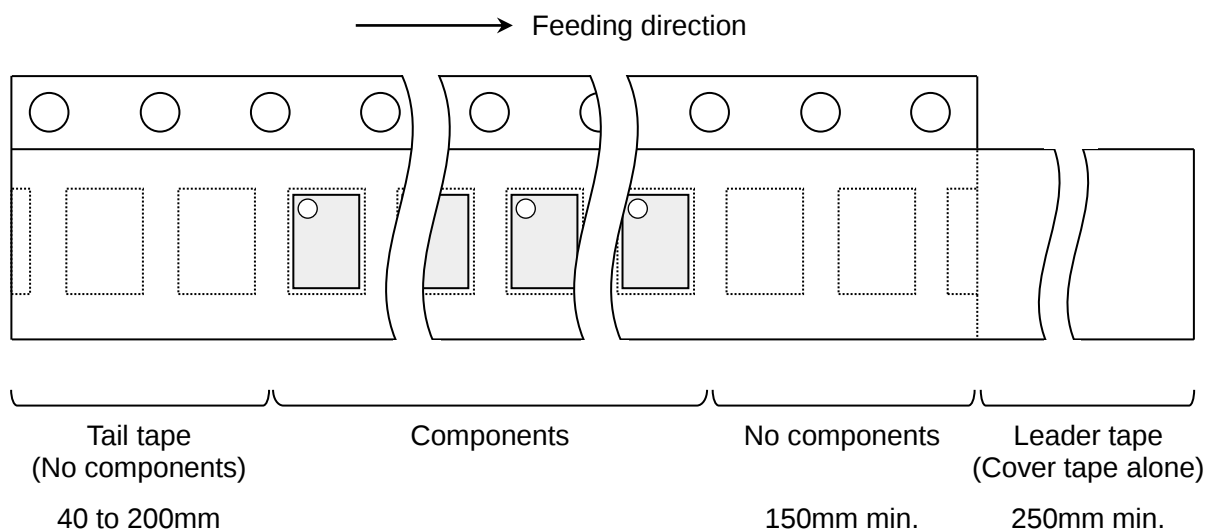
[2] Hole for chip : As specified in (1)

[3] Cover tape : 62μm in thickness

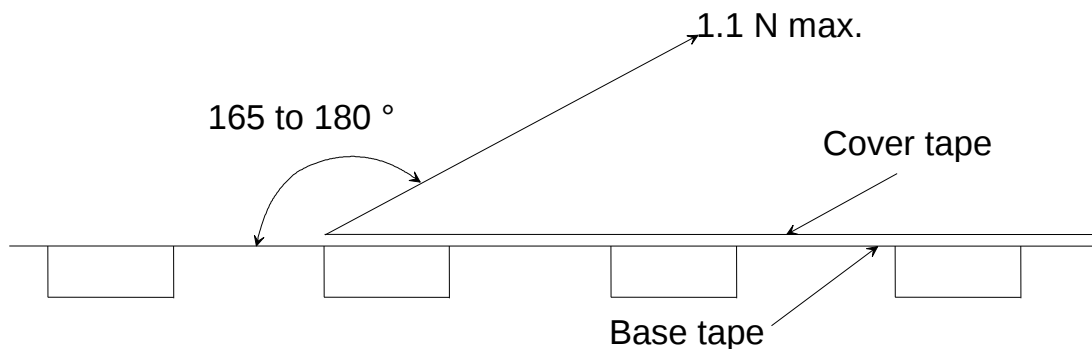
[4] Base tape : As specified in (1)



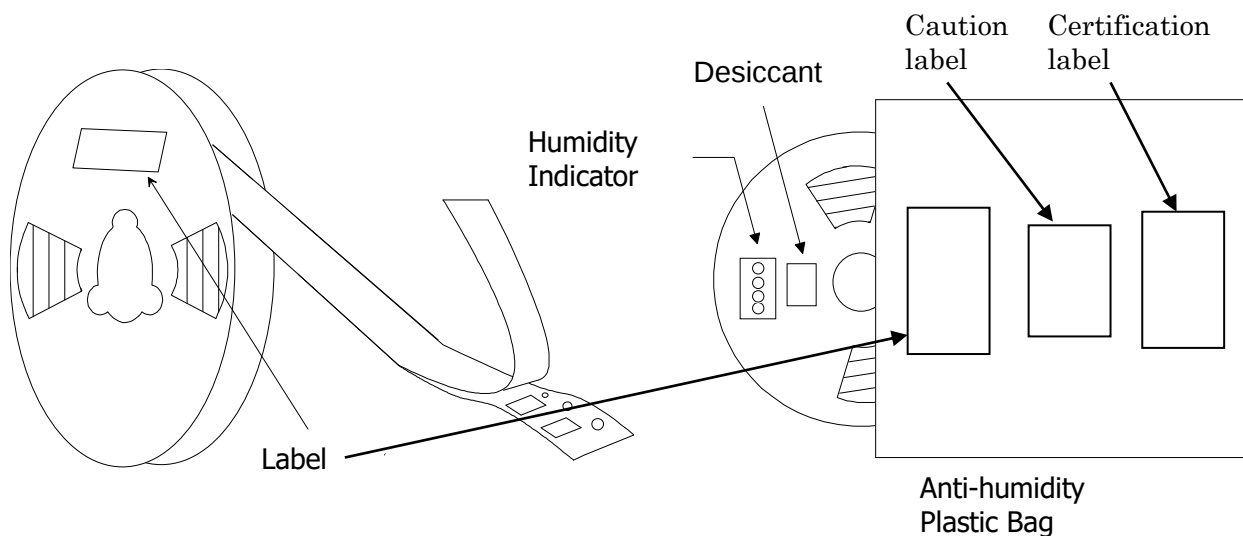
### (4) Leader and Tail tape



- (5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- (6) The cover tape and base tape are not adhered at no components area for 250mm min.
- (7) Tear off strength against pulling of cover tape : 5N min.
- (8) Packaging unit : 1000pcs./ reel
- (9) material : Base tape : Plastic  
Real : Plastic  
Cover tape, cavity tape and reel are made the anti-static processing.
- (10) Peeling of force : 1.1N max. in the direction of peeling as shown below.



- (11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

## **15. Notice**

### **15.1. Storage Conditions**

Please use this product within 6month after receipt.

- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.

(Packing materials, in particular, may be deformed at the temperature over 40 °C)

- The product left more than 6months after reception, it needs to be confirmed the solder ability before used.

- The product shall be stored in non-corrosive gas (CL2, NH3, SO2, NOx, etc.).

- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)

- After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.

Please record and manage the time after opening.

- Product should be repacked with desiccating agent immediately after using.

- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125 +5/-0 °C, 24 hours, 1 time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

\*For the MSL standard, see IPC/JEDEC J-STD-020 (can be downloaded from [www.jedec.org](http://www.jedec.org)).

If the storage environment is not conducted above standard conditions, it will cause some issue (e.g., Operation issue, Overcurrent, Malfunction) we shall not be responsible for that.

Before using please refer to "PRECONDITIONS TO USE MURATA PRODUCTS"

### **15.2. Handling Conditions**

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability.

### **15.3. Standard PCB Design (Land Pattern and Dimensions)**

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

### **15.4. Notice for Chip Placer :**

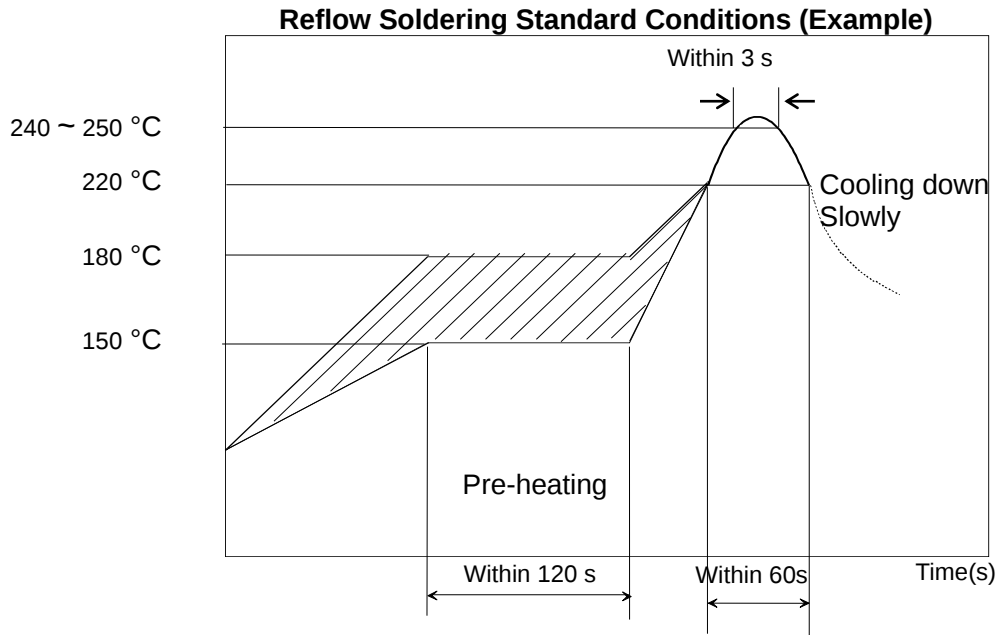
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

### **15.5. Soldering Conditions :**

The recommendation conditions of soldering are as in the following figure.

When products are immersed in solvent after mounting, pay special attention to maintain the temperature difference within 100 °C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C.

Contact Murata before use if concerning other soldering conditions.



Please use the reflow within 2 times.

Use rosin Type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

#### **15.6. Cleaning :**

Since this Product is Moisture Sensitive, any cleaning is not permitted.

#### **15.7. Operational Environment Conditions :**

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (CL<sub>2</sub>, NH<sub>3</sub>, SO<sub>x</sub>, NO<sub>x</sub>, etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

#### **15.8. Input Power Capacity :**

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

## **16. Regulatory Statements**

### **16.1. FCC Statements**

T.B.D.

### **16.2. IC Statements**

T.B.D.

## **17. PRECONDITION TO USE OUR PRODUCTS**

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

WE HEREBY DISCLAIMS ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You agree that you will use any and all software or program code (including but not limited to hcd, firmware, nvram, and blob) we may provide or to be embedded into our product ("Software") provided that you use the Software bundled with our product. YOU AGREE THAT THE SOFTWARE SHALL BE PROVIDED TO YOU "AS-IS" BASIS, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES THAT THE SOFTWARE IS ERROR-FREE OR WILL OPERATE WITHOUT INTERRUPTION. AND MORE, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED WITH RESPECT TO THE SOFTWARE. MURATA EXPRESSLY DISCLAIM ANY AND ALL WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE NOR THE WARRANTY OF TITLE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You shall indemnify and hold harmless us, our affiliates and our licensor from and against any and all claims, costs, expenses and liabilities (including attorney's fees), which arise in connection with the using the Software.

The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment
- Undersea equipment.
- Power plant control equipment
- Medical equipment.
- Traffic signal equipment.
- Burning / explosion control equipment
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.

Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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- deviation or lapse in function of engineering sample,
- improper use of engineering samples.

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