RJK1053DPB

100V, 25A, 13mΩ max.
Silicon N Channel Power MOS FET
Power Switching

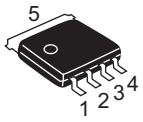
R07DS0084EJ0200
Rev.2.00
Apr 11, 2013

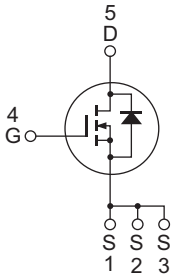
Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 10 mΩ typ. (at V_{GS} = 10 V)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)





1, 2, 3	Source
4	Gate
5	Drain

Application

- Switching Mode Power Supply

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ Note1	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} Note 2	12.5	A
Avalanche energy	E_{AS} Note 2	15.6	mJ
Channel dissipation	Pch Note3	65	W
Channel to Case Thermal Resistance	θch-C	1.92	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

This product is for the low voltage drive (≤ 10V).
If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ($V_{GS(off)}$) which characteristics has been improved.

Electrical Characteristics

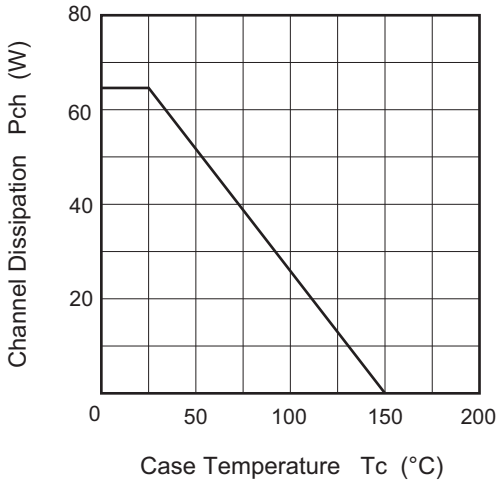
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	10	13	mΩ	I_D = 12.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	11	15	mΩ	I_D = 12.5A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	—	70	—	S	I_D = 12.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	6160	—	pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance	Coss	—	508	—	pF	
Reverse transfer capacitance	Crss	—	193	—	pF	
Gate Resistance	Rg	—	0.5	—	Ω	
Total gate charge	Qg	—	43	—	nC	V_{DD} = 50 V, V_{GS} = 4.5 V, I_D = 25 A
Gate to source charge	Qgs	—	19	—	nC	
Gate to drain charge	Qgd	—	12.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	13	—	ns	V_{GS} = 10 V, I_D = 12.5 A, V_{DD} ≅ 30 V, R_L = 2.4 Ω, Rg = 4.7 Ω
Rise time	t_r	—	5.6	—	ns	
Turn-off delay time	$t_{d(off)}$	—	68	—	ns	
Fall time	t_f	—	9.0	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.83	1.1	V	I_F = 25 A, V_{GS} = 0 V Note4
Body–drain diode reverse recovery time	t_{rr}	—	52	—	ns	I_F = 25 A, V_{GS} = 0 V di_F/ dt = 100 A/ μs

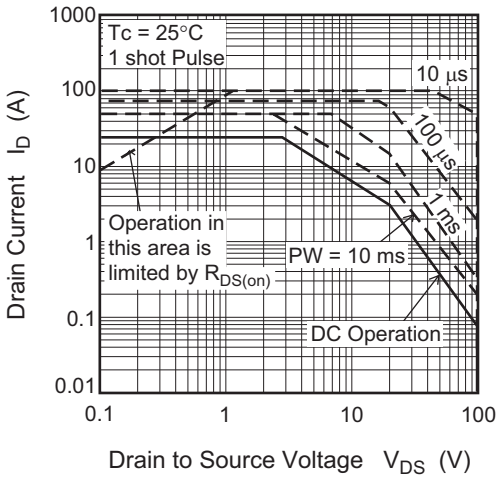
Notes: 4. Pulse test

Main Characteristics

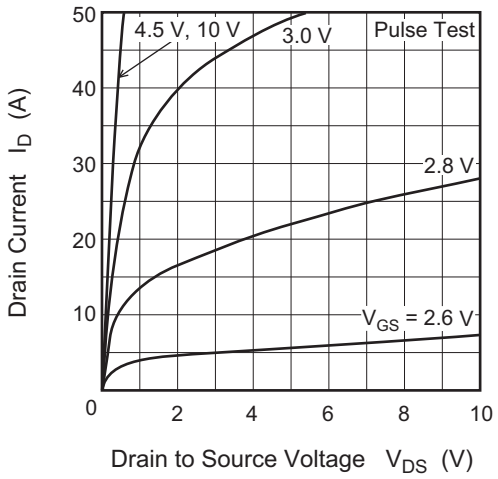
Power vs. Temperature Derating



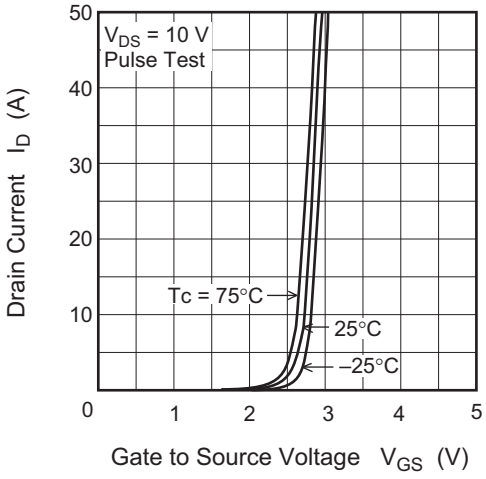
Maximum Safe Operation Area



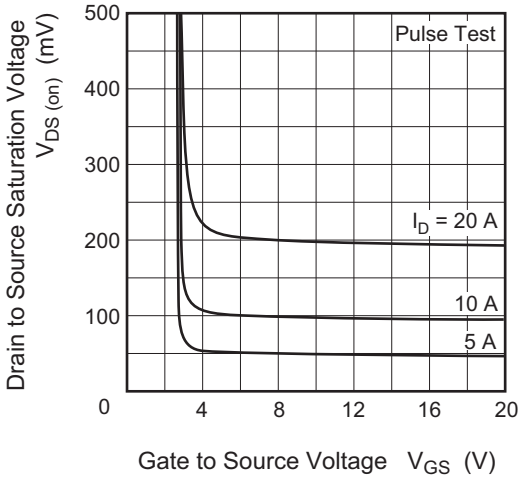
Typical Output Characteristics



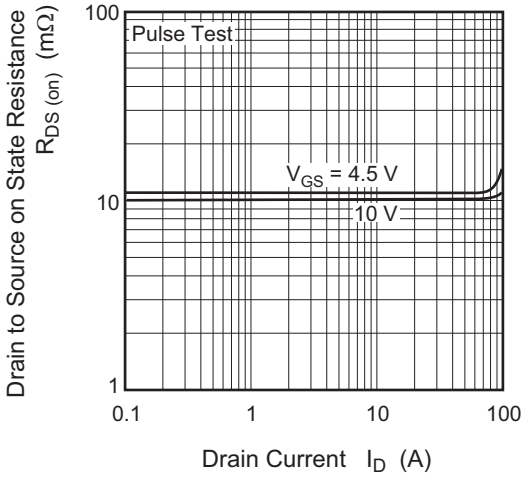
Typical Transfer Characteristics



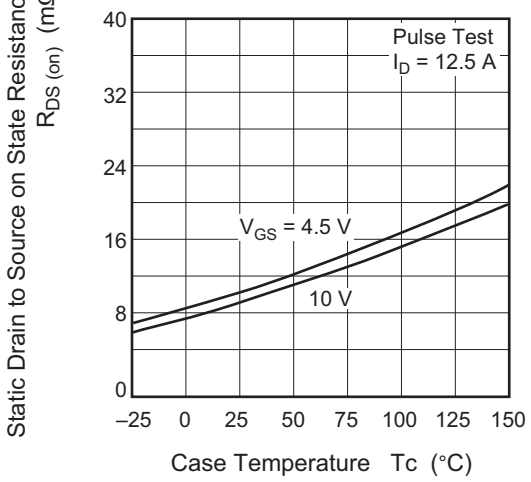
Drain to Source Saturation Voltage vs. Gate to Source Voltage



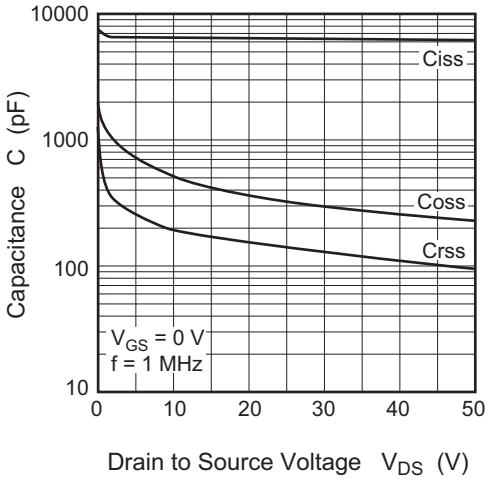
Static Drain to Source on State Resistance vs. Drain Current



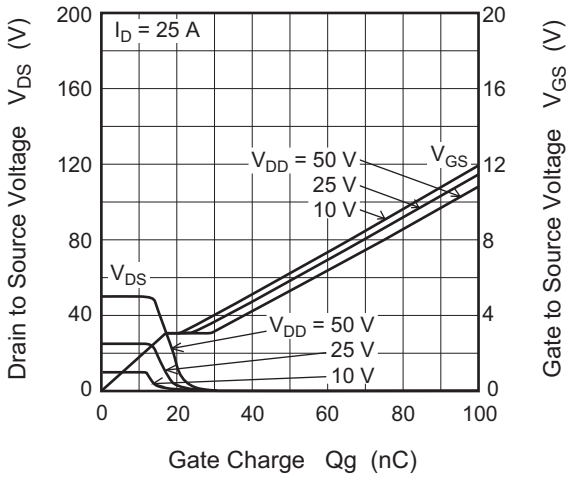
Static Drain to Source on State Resistance vs. Temperature



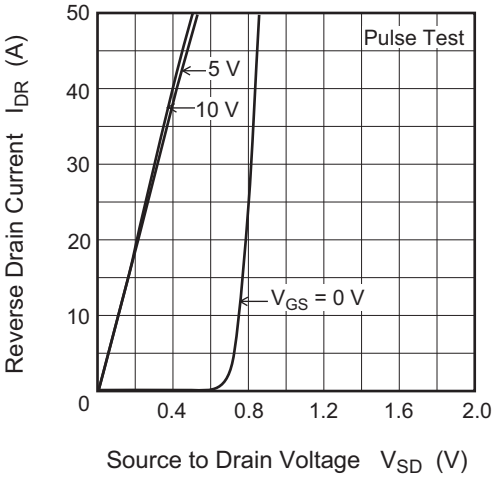
Typical Capacitance vs. Drain to Source Voltage



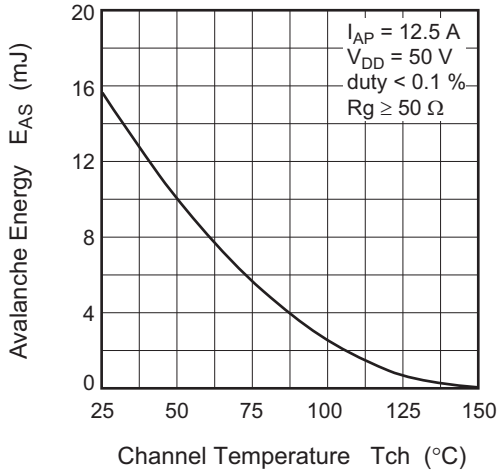
Dynamic Input Characteristics



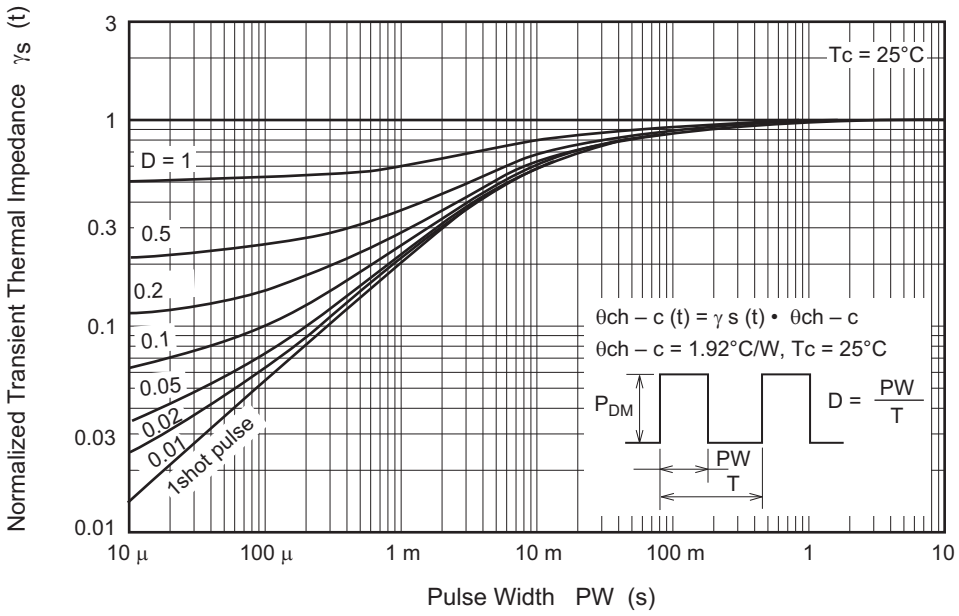
Reverse Drain Current vs. Source to Drain Voltage



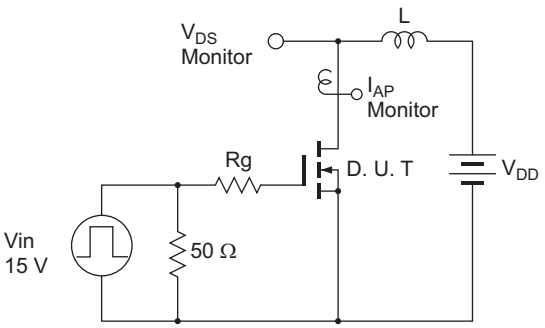
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

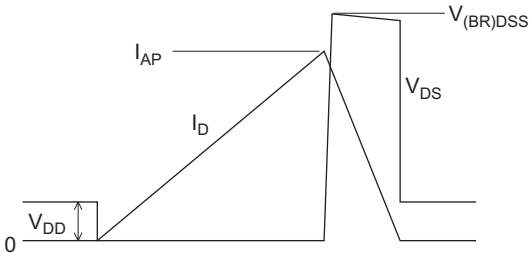


Avalanche Test Circuit

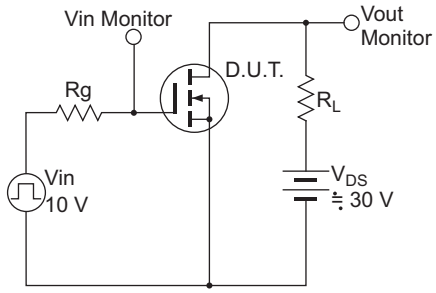


Avalanche Waveform

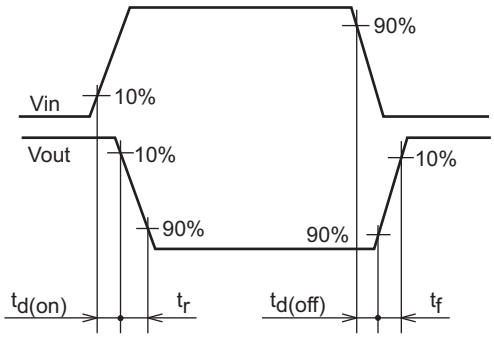
$$E_{AS} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



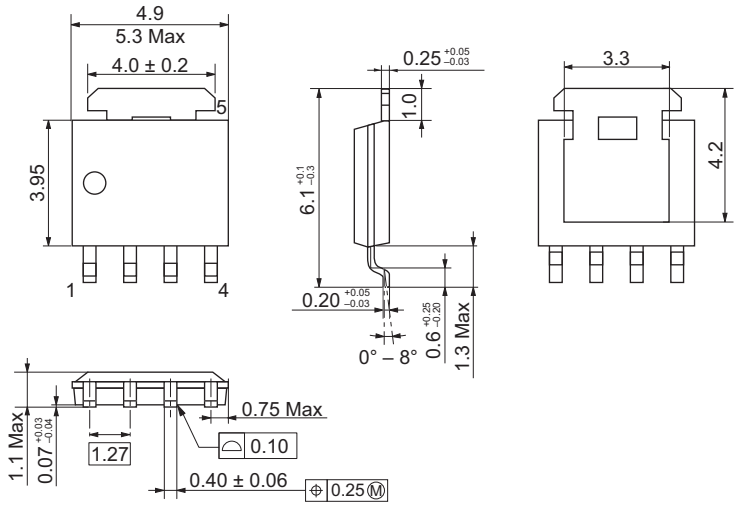
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part No.	Quantity	Shipping Container
RJK1053DPB-00-J5	2500 pcs	Taping

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