System Clock for Embedded AMD™ based Systems

Recommended Application:

AMD M690T/780E systems

Output Features:

- Integrated series resistors on all differential outputs.
- 1 - Greyhound compatible low-power CPU pair
- 6 - low-power differential SRC pairs
- 2 - low-power differential chipset SouthBridge SRC pairs
- 1 - Selectable low-power differential 100MHz non-spread SATA/ SRC output
- 1 - Selectable low-power differential SRC / 27MHz Single Ended output
- 1 - Selectable HT3 100MHz low-power differential hypertransport clock / HT66MHz Single Ended output
- 2 - 48MHz USB clock
- 3 - 14.318MHz Reference clock
- 3 - low-power differential ATIG pairs
- 5- Dedicated CLKREQ# pins

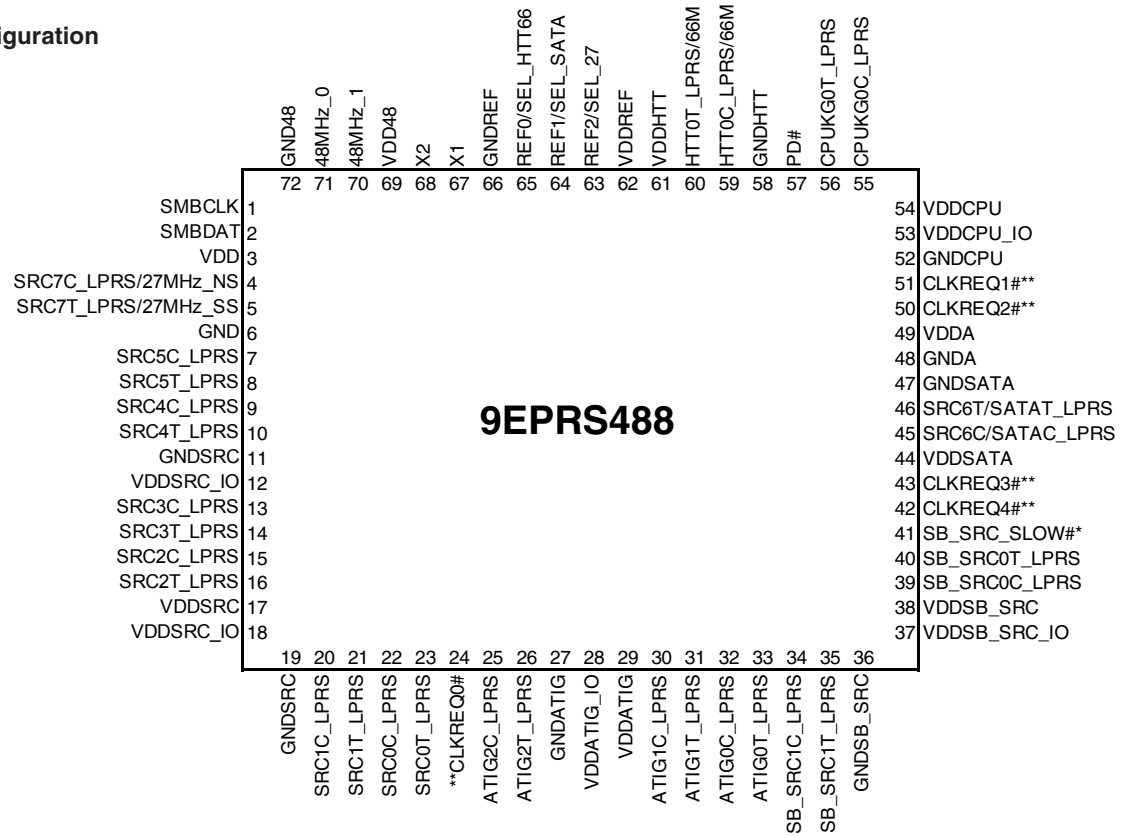
Key Specifications:

- CPU outputs cycle-to-cycle jitter < 150ps
- SRC outputs cycle-to-cycle jitter < 125ps
- SB_SRC outputs cycle-to-cycle jitter < 125ps
- +/- 100ppm frequency accuracy on CPU, SRC, ATIG
- 0ppm frequency accuracy on 48MHz

Features/Benefits:

- Power Saving Features:
  SB_SRC_SLOW# input to throttle Chipset clocks (SB_SRC) to 80% of normal.
  Optional Separate supply rail for SRC low Voltage I/O
  - ~33% power saving when 1.5V is used for this rail
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy

Pin Configuration



*** Internal 120Kohm Pull-Up Resistor**
**** Internal Pull-Down Resistor**

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*Other names and brands may be claimed as the property of others.

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
2	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
3	VDD	PWR	Power supply for SRC7/27MHz
4	SRC7C_LPRS/27MHz_NS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)/27MHz 3.3V Single-ended non-spread output for discrete graphics
5	SRC7T_LPRS/27MHz_SS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)/27MHz 3.3V Single-ended spreading output for discrete graphics
6	GND	GND	Ground pin for SRC7/27MHz
7	SRC5C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
8	SRC5T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
9	SRC4C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
10	SRC4T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
11	GNDSRC	GND	Ground pin for the SRC outputs
12	VDDSRC_IO	PWR	Power supply for differential SRC outputs, nominal 1.05V to 3.3V
13	SRC3C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
14	SRC3T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
15	SRC2C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
16	SRC2T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
17	VDDSRC	PWR	Supply for SRC core, 3.3V nominal
18	VDDSRC_IO	PWR	Power supply for differential SRC outputs, nominal 1.05V to 3.3V
19	GNDSRC	GND	Ground pin for the SRC outputs
20	SRC1C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
21	SRC1T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
22	SRC0C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
23	SRC0T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
24	**CLKREQ0#	IN	Clock Request pin for SRC0 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low
25	ATIG2C_LPRS	OUT	Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
26	ATIG2T_LPRS	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
27	GNDATIG	GND	Ground pin for the ATIG outputs
28	VDDATIG_IO	PWR	Power supply for differential ATIG outputs, nominal 1.05V to 3.3V
29	VDDATIG	PWR	Power supply for ATIG core, nominal 3.3V
30	ATIG1C_LPRS	OUT	Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
31	ATIG1T_LPRS	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
32	ATIG0C_LPRS	OUT	Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
33	ATIG0T_LPRS	OUT	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
34	SB_SRC1C_LPRS	OUT	Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
35	SB_SRC1T_LPRS	OUT	True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
36	GNDSB_SRC	GND	Ground pin for the SB_SRC outputs

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Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	VDDSB_SRC_IO	PWR	Power supply for differential SB_SRC outputs, nominal 1.05V to 3.3V
38	VDDSB_SRC	PWR	Supply for SB SRC PLL core, 3.3V nominal
39	SB_SRC0C_LPRS	OUT	Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
40	SB_SRC0T_LPRS	OUT	True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
41	SB_SRC_SLOW#*	IN	When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation.
42	CLKREQ4#**	IN	Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low
43	CLKREQ3#**	IN	Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low
44	VDDSATA	PWR	Power supply for SATA core logic, nominal 3.3V
45	SRC6C/SATAC_LPRS	OUT	Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
46	SRC6T/SATAT_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
47	GNDSATA	GND	Ground pin for the SRC outputs
48	GNDA	GND	Ground for the Analog Core
49	VDDA	PWR	3.3V Power for the Analog Core
50	CLKREQ2#**	IN	Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low
51	CLKREQ1#**	IN	Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low
52	GNDCPU	GND	Ground pin for the CPU outputs
53	VDDCPU_IO	PWR	Power supply for differential CPU outputs, nominal 1.05V to 3.3V
54	VDDCPU	PWR	Supply for CPU core, 3.3V nominal
55	CPUKG0C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed)
56	CPUKG0T_LPRS	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor.(no 33 ohm series resistor needed)
57	PD#	IN	Enter /Exit Power Down. 0 = Power Down, 1 = normal operation.
58	GNDHTT	PWR	Ground pin for the HTT outputs
59	HTT0C_LPRS/66M	OUT	Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended 66MHz hyper transport clock
60	HTT0T_LPRS/66M	OUT	True signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) /1.8V single ended 66MHz hyper transport clock
61	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
62	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
63	REF2/SEL_27	OUT	14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7 0 = 100MHz differential spreading SRC clock, 1 = 27MHz non-spreading singled clock on pin 4 and 27MHz spread clock on pin 5.
64	REF1/SEL_SATA	I/O	14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select function of SRC6/SATA output 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock
65	REF0/SEL_HTT66	I/O	14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock Frequency. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock
66	GNDREF	GND	Ground pin for the REF outputs.
67	X1	IN	Crystal input, nominally 14.318MHz
68	X2	OUT	Crystal output, nominally 14.318MHz
69	VDD48	PWR	Power pin for the 48MHz outputs and core. 3.3V
70	48MHz_1	OUT	48MHz clock output.
71	48MHz_0	OUT	48MHz clock output.
72	GND48	GND	Ground pin for the 48MHz outputs

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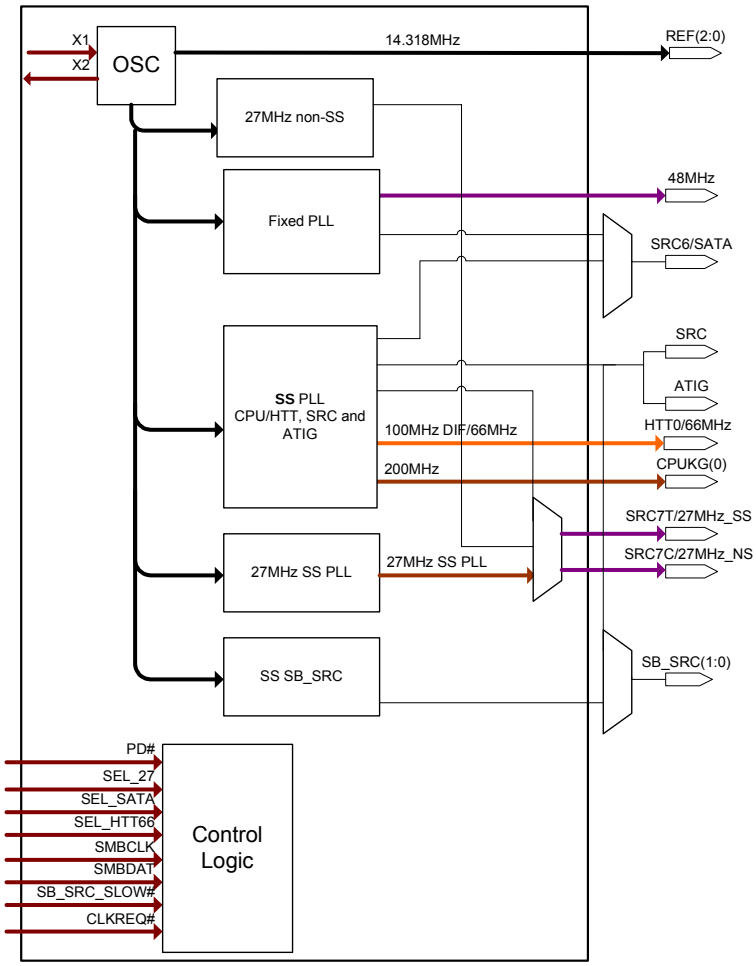
General Description

The **ICS9EPRS488** is a main clock synthesizer chip that provides all clocks required for AMD M690T or 780E embedded systems. An SMBus interface allows full control of the device.

Block Diagram



Power Groups

Pin Number			Description
VDD	VDDIO	GND	
69		72	USB_48 outputs
3		6	SRC/27MHz Outputs
17		11,19	SRC Logic Core
	12,18		SRC differential outputs (IO's)
38		36	SB_SRC Core Logic
	37		SB_SRC differential outputs (IO's)
44		47	SRC/SATA differential output
29		27	ATIG Core Logic
	28		ATIG differential outputs (IO's)
49		48	3.3V Analog
54		52	CPUKG Core Logic
	53		CPUKG differential outputs (IO's)
61		58	HTTCLK output
62		66	REF outputs

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Table1: CPU/HTT, SRC and ATIG Frequency Selection Table

Byte 0	Byte 3				CPU (MHz)	HTT Single-ended	Differential HTT	SRC/ATIG	Spread %	CPU OverClock %
Bit0	Bit3	Bit2	Bit1	Bit0						
SS_EN	CPU FS3	CPU FS2	CPU FS1	CPU FS0		SEL_HTT66 = 1	SEL_HTT66 = 0			
0	0	0	0	0	173.63	57.88	86.81	86.81	Off	-13%
0	0	0	0	1	177.17	59.06	88.58	88.58		-11%
0	0	0	1	0	180.78	60.26	90.39	90.39		-10%
0	0	0	1	1	184.47	61.49	92.24	92.24		-8%
0	0	1	0	0	188.24	62.75	94.12	94.12		-6%
0	0	1	0	1	192.08	64.03	96.04	96.04		-4%
0	0	1	1	0	196.00	65.33	98.00	98.00		-2%
0	**0**	**1**	**1**	**1**	**200.00**	**66.67**	**100.00**	**100.00**		**0%**
0	1	0	0	0	204.00	68.00	102.00	102.00		2%
0	1	0	0	1	208.08	69.36	104.04	104.04		4%
0	1	0	1	0	212.24	70.75	106.12	106.12		6%
0	1	0	1	1	216.49	72.16	108.24	108.24		8%
0	1	1	0	0	220.82	73.61	110.41	110.41		10%
0	1	1	0	1	225.23	75.08	112.62	112.62		13%
0	1	1	1	0	229.74	76.58	114.87	114.87		15%
0	1	1	1	1	234.33	78.11	117.17	117.17		17%
1	0	0	0	0	173.63	57.88	86.81	86.81	-0.5%	-13%
1	0	0	0	1	175.00	59.06	88.58	88.58		-11%
1	0	0	1	0	180.78	60.26	90.39	90.39		-10%
1	0	0	1	1	184.47	61.49	92.24	92.24		-8%
1	0	1	0	0	188.24	62.75	94.12	94.12		-6%
1	0	1	0	1	192.08	64.03	96.04	96.04		-4%
1	0	1	1	0	196.00	65.33	98.00	98.00		-2%
1	0	1	1	1	**200.00**	**66.67**	**100.00**	**100.00**		**0%**
1	1	0	0	0	204.00	68.00	102.00	102.00		2%
1	1	0	0	1	208.08	69.36	104.04	104.04		4%
1	1	0	1	0	212.24	70.75	106.12	106.12		6%
1	1	0	1	1	216.49	72.16	108.24	108.24		8%
1	1	1	0	0	220.82	73.61	110.41	110.41		10%
1	1	1	0	1	225.23	75.08	112.62	112.62		13%
1	1	1	1	0	229.74	76.58	114.87	114.87		15%
1	1	1	1	1	234.33	78.11	117.17	117.17		17%

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Table 2: SB_SRC Frequency Selection Table

Byte 0	Byte 4				SRC (MHz)	Spread %	SB_SRC OverClock %
Bit0	Bit3	Bit2	Bit1	Bit0			
SS_EN	SB FS3	SB FS2	SB FS1	SB FS0			
0	0	0	0	0	80.00	Off	-20%
0	0	0	0	1	81.25		-19%
0	0	0	1	0	82.63		-17%
0	0	0	1	1	84.00		-16%
0	0	1	0	0	85.25		-15%
0	0	1	0	1	86.63		-13%
0	0	1	1	0	88.00		-12%
0	0	1	1	1	89.25		-11%
0	1	0	0	0	90.63		-9%
0	1	0	0	1	92.00		-8%
0	1	0	1	0	93.25		-7%
0	1	0	1	1	94.63		-5%
0	1	1	0	0	96.00		-4%
0	1	1	0	1	97.25		-3%
0	1	1	1	0	98.63		-1%
0	**1**	**1**	**1**	**1**	**100.00**		0%
1	0	0	0	0	80.00	-0.50%	20%
1	0	0	0	1	175.00		-19%
1	0	0	1	0	82.63		-17%
1	0	0	1	1	84.00		-16%
1	0	1	0	0	85.25		-15%
1	0	1	0	1	86.63		-13%
1	0	1	1	0	88.00		-12%
1	0	1	1	1	89.25		-11%
1	1	0	0	0	90.63		-9%
1	1	0	0	1	92.00		-8%
1	1	0	1	0	93.25		-7%
1	1	0	1	1	94.63		-5%
1	1	1	0	0	96.00		-4%
1	1	1	0	1	97.25		-3%
1	1	1	1	0	98.63		-1%
1	1	1	1	1	100.00		0%

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Table 3: 27Mhz_Spread and Frequency Selection Table

SS Enable B2b1	SS3 Byte 4 bit 7	SS2 Byte 4 bit 6	SS1 Byte 4 bit 5	SS0 Byte 4 bit 4	27MHz_Spread (MHz)	Spread % (when enabled)	
0	**0**	**0**	**0**	**0**	27.00	No Spread	
0	0	0	0	1	27.00		
0	0	0	1	0	27.00		
0	0	0	1	1	27.00		
0	0	1	0	0	27.00		
0	0	1	0	1	27.00		
0	0	1	1	0	27.00		
0	0	1	1	1	27.00		
0	1	0	0	0	27.00		
0	1	0	0	1	27.00		
0	1	0	1	0	27.00		
0	1	0	1	1	27.00		
0	1	1	0	0	27.00		
0	1	1	0	1	27.00		
0	1	1	1	0	27.00		
0	1	1	1	1	27.00		
1	0	0	0	0	27.00	-0.50	Down
1	0	0	0	1	27.00	-1.00	Down
1	0	0	1	0	175.00	-1.50	Down
1	0	0	1	1	27.00	-2.00	Down
1	0	1	0	0	27.00	-0.75	Down
1	0	1	0	1	27.00	-1.25	Down
1	0	1	1	0	27.00	-1.75	Down
1	0	1	1	1	27.00	-2.25	Down
1	1	0	0	0	27.00	+/-0.25	Center
1	1	0	0	1	27.00	+/-0.5	Center
1	1	0	1	0	27.00	+/-0.75	Center
1	1	0	1	1	27.00	+/-1.0	Center
1	1	1	0	0	27.00	+/-0.25	Center
1	1	1	0	1	27.00	+/-0.5	Center
1	1	1	1	0	27.00	+/-0.75	Center
1	1	1	1	1	27.00	+/-1.0	Center

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Table 4: CPU Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	**0001**	**3**	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 5: SRC, SB_SRC, ATIG Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	**0101**	**6**	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	14	1011	28	1111	56
	LSB	Address	Div	Address		Address	Div	Address	Div

Differential Output Power Management Table

PD#	**CLKREQ#**	**SMBus Register OE**	**True output**	**Complement Output**	**True output**	**Complement Output**
			Free-Run		**CLKREQ# Selected**	
1	**0**	Enable	Running	Running	Running	Running
0	X	X	Low/20K	Low	Low/20K	Low
1	**1**	Enable	Running	Running	Low/20K	Low
X	X	**Disable**	Low/20K	Low	Low/20K	Low

Note: 20K means 20Kohm Pull Down

Singled-ended Power Management Table

PD#	**SMBus Register OE**	**48MHz**	**27MHz**	**HTT66MHz**	**REF(2:0)**
1	Enable	Running	Running	Running	Running
0	Enable	Low	Low	Low	Hi-Z

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Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-		3.3	GND + 3.9V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-	3.135	3.3	3.465	V	1
Input High Voltage	V_{IH}	VDD = 3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	VDD = 3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	VDD = 3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	VDD = 3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	3.3V VDD current, all outputs driven			175	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs low/low			2	mA	1
Input Frequency	F_i	VDD = 3.3 V +/-5%		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			3	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	$I_{PULLUPSMB}$		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

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AC Electrical Characteristics - Low-Power DIF Outputs: CPUKG and HTT

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
Frequency - CPU	f_{CPU}	Spread Specturm On	198.8		200	MHz	1,3
Frequency - HTT	f_{HTT}	Spread Specturm On	99.4		100	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-300		+300	ppm	1,11
Rising Edge Slew Rate	S_{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S_{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement			150	ps	1,6
Accumulated Jitter	t_{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	$V_{D(PK-PK)}$	Differential Measurement	400		2400	mV	1,8
Differential Voltage	V_D	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in V_D DC cycle to cycle	-75		75	mV	1,10
CPU[1:0] Skew	CPU_{SKEW10}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not

[3]Minimum Frequency is a result of 0.5% down spread spectrum

[4]Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] Max difference of t_{CYCLE} between any two adjacent cycles.

[7] Accumulated tjc.over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

[8] VD(PK-PK) is the overall magnitude of the differential signal.

[9] VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

[10] The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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AC Electrical Characteristics - Low-Power DIF Outputs: SRC, SB_SRC and ATIG

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.6		4	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.6		4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
SRC, ATIG, Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement			125	ps	1
SRC[5:0] Skew	SRC_{SKEW}	Differential Measurement			250	ps	1
SB_SRC[1:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1
ATIG[2:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - Single-ended HTT 66MHz Clock

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
HTT66 Clock period	T_{period}	66.67MHz output nominal	14.9955		15.0045	ns	2
		66.67MHz output spread	14.9955		15.0799	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	1.6	1.8	3.3	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0	0.2	V	1
Rise Time	t_{r1}	V_{OL} = 0.36 V, V_{OH} = 1.44 V			1.5	ns	1
Fall Time	t_{f1}	V_{OH} = 1.44 V, V_{OL} = 0.36 V			1.5	ns	1
Duty Cycle	d_{t1}	V_T = 0.9 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 0.9 V			300	ps	1
Jitter, Long Term	t_{LTJ}	V_T = 0.9 V			1	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

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Electrical Characteristics - USB - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1.5	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1.5	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			130	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics - 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		50	ppm	1,2
			-15		15		1,2,3
Clock period	T_{period}	27.000MHz output nominal	37.0365		37.0376	ns	2
Output High Voltage(27SS)	V_{OH}	I_{OH} = -1 mA	2.1			V	1,10
Output High Voltage (27NSS)	V_{OH}	I_{OH} = -1 mA	0.8			V	1,11
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-29			mA	1,10
		V_{OH} = 3.135 V			-23	mA	1,10
Output Low Current	I_{OL}	V_{OL} = 1.95 V	29			mA	1,10
		V_{OL} = 0.4 V			27	mA	1,10
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate V_T @ 20%-80%	1	2	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	t_{ltj}	Long Term (10us)			300	ps	1
	$t_{jcyc-cyc}$	V_T = 1.5 V			200	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[10] V_{DD} = 3.3V

[11] V_{DD} = 1.1V

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Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		1.5	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		1.5	ns	1
Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			200	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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General SMBus serial interface information for the ICS9EPRS488

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Latched Input Readback Output Enable Control Register

Byte 0	Name	Description	Type	0	1	Default
Bit 7	SEL_HTT66 readback	Hypertransport Select	R	100MHz Differential HTT clock	66 MHz 3.3V Single-ended HTT clock	Latch
Bit 6	SEL_SATA readback	SATA Select	R	SRC6/SATA pair is SRC SS capable output	SRC6/SATA pair is SATA non-spread output	Latch
Bit 5	REF0_OE	Output Enable	RW	Hi-Z	Enabled	1
Bit 4	REF1_OE	Output Enable	RW	Hi-Z	Enabled	1
Bit 3	REF2_OE	Output Enable	RW	Hi-Z	Enabled	1
Bit 2	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
Bit 1	48MHz_0_OE	Output Enable	RW	Low	Enabled	1
Bit 0	SS_Enable	Spread Spectrum Enable (CPU, SRC, SB_SRC, ATIG)	RW	Spread Off	Spread On	0

SMBus Table:Output Enable Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SRC7/27MHz_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 6	SRC6/SATA_OE Enable	Output Enable	RW	Low/Low	Enabled	1
Bit 5	SRC5_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 4	SRC4_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 0	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: Output Enable and 48MHz Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SB_SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 6	SB_SRC0_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 5	48MHz_0_Slew Rate	Slew Rate Control	RW	These bits program the slew rate of the single ended outputs. The maximum slew rate is 1.9V/ns and the minimum slew rate is 1.1V/ns. The slew rate selection is as follows: 11 = 1.9V/ns 10 = 1.6V/ns 01 = 1.1V/ns 00 = tristated		1
Bit 4						1
Bit 3	ATIG1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	ATIG0_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	27MHz_SS_Enable	Spread Spectrum Enable 27MHz_SS	RW	Spread Off	Spread On	0
Bit 0	Reserved	Reserved	RW	-	-	X

SMBus Table: CPU/HTT Frequency Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	CPU0_OE	Output enable	RW	Low/Low	Enable	1
Bit 6	SEL_27 readback	SRC7/27MHz Select	R	SRC7 Output	27MHz Output	Latch
Bit 5	ATIG2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 4	HTT/66MHz_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	CPU_FS3	CPU Frequency Select	RW	See CPU/HTT/SRC/ATIG Frequency Select Table Default value corresponds to 200MHz. Note that the HTT frequency tracks the CPU frequency.		0
Bit 2	CPU_FS2	CPU Frequency Select	RW			1
Bit 1	CPU_FS1	CPU Frequency Select	RW			1
Bit 0	CPU_FS0	CPU Frequency Select LSB	RW			1

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SMBus Table: SB_SRC Frequency Control Register

Byte	4	Name	Control Function	Type	0	1	Default
	Bit 7	S3	27_SSC Spread Select	RW	S[1:0]: 00 = -0.5% Default, 01 =1.0%, 10 = -1.5%, 11 = -2%. See Table 3: 27Mhz_Spread, LCDCLK Spread and Frequency Selection Table for additional selections.		0
	Bit 6	S2		RW			0
	Bit 5	S1		RW			0
	Bit 4	S0		RW			0
	Bit 3	SB_SRC_FS3	SB_SRC Frequency Select	RW	See SB_SRC Frequency Select Table.		1
	Bit 2	SB_SRC_FS2	SB_SRC Frequency Select	RW			1
	Bit 1	SB_SRC_FS1	SB_SRC Frequency Select	RW			1
	Bit 0	SB_SRC_FS0	SB_SRC Freq. Select LSB	RW			1

SMBus Table: 27MHz Slew Rate Control Register

Byte	5	Name	Control Function	Type	0	1	Default
	Bit 7	27M_SS_Slew Rate	Slew Rate Control	RW	These bits program the slew rate of the single ended outputs. The maximum slew rate is 1.9V/ns and the minimum slew rate is 1.1V/ns. The slew rate selection is as follows: 11 = 1.9V/ns 10 = 1.6V/ns 01 = 1.1V/ns 00 = tristated		1
	Bit 6						1
	Bit 5	27M_NS_Slew Rate	Slew Rate Control	RW			1
	Bit 4						1
	Bit 3	SB_SRC Source	SB_SRC Source Selection	RW	SB_SRC PLL	SRC PLL	1
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBus Table: I/O Vout Control Register

Byte	6	Name	Control Function	Type	0	1	Default
	Bit 7	SRC Diff AMP	SRC Differential output Amplitude Control	RW	00 = 700mV	01 = 800mV	0
	Bit 6	SRC Diff AMP		RW	10 = 900mV	11 = 1000mV	1
	Bit 5	CPU Diff AMP	CPU Differential output Amplitude Control	RW	00 = 700mV	01 = 800mV	0
	Bit 4	CPU Diff AMP		RW	10 = 900mV	11 = 1000mV	1
	Bit 3	SB_SRC Diff AMP	SB_SRC Differential output Amplitude Control	RW	00 = 700mV	01 = 800mV	0
	Bit 2	SB_SRC Diff AMP		RW	10 = 900mV	11 = 1000mV	1
	Bit 1	Reserved					X
	Bit 0	Reserved					X

SMBus Table: Vendor & Revision ID Register

Byte	7	Name	Control Function	Type	0	1	Default
	Bit 7	RID3	REVISION ID	R	-	-	0
	Bit 6	RID2		R	-	-	1
	Bit 5	RID1		R	-	-	0
	Bit 4	RID0		R	-	-	0
	Bit 3	VID3	VENDOR ID	R	-	-	0
	Bit 2	VID2		R	-	-	0
	Bit 1	VID1		R	-	-	0
	Bit 0	VID0		R	-	-	1

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SMBus Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	BC5	Byte Count bit 5 (MSB)	RW	Determines the number of bytes that are read back from the device. Default is 0F hex.		0
Bit 4	BC4	Byte Count bit 4	RW			0
Bit 3	BC3	Byte Count bit 3	RW			1
Bit 2	BC2	Byte Count bit 2	RW			1
Bit 1	BC1	Byte Count bit 1	RW			1
Bit 0	BC0	Byte Count bit 0 (LSB)	RW			1

SMBus Table: WatchDog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hartd Alarm Timer, Clear WD Hard status bit.	Enable Timer	0
Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

SMBus Table: WD Timer Safe Frequency Control Register

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW			1
Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW			1
Bit 4	WD SF4	Watch Dog Safe Freq Programming bits	RW	These bits configure the safe frequency that the device returns to if the Watchdog Timer expires. The value show here corresponds to the power up default of the device. See the various Frequency Select Tables for the exact frequencies.		0
Bit 3	WD SF3		RW			0
Bit 2	WD SF2		RW			1
Bit 1	WD SF1		RW			1
Bit 0	WD SF0		RW			1

SMBus Table: CPU PLL Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the VCO frequency. Default at power up = Byte 3 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0) .		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bits	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

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SMBus Table: CPU PLL Frequency Control Register

Byte	12	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming b(10:3)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the VCO frequency. Default at power up = Byte 3 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0) .		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	13	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming b(7:0)	RW	Bytes 13 and 14 set the CPU/HTT/SRC/ATIG spread pecentage.Please contact ICS for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	14	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					X
	Bit 6	SSP14	Spread Spectrum Programming b(14:8)	RW	Bytes 13 and 14 set the CPU/HTT/SRC/ATIG spread pecentage.Please contact ICS for the appropriate values.		X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

SMBUS Table: CPU Output Divider Register

Byte	15	Name	Control Function	Type	0	1	Default
	Bit 7	CPU NDiv0	LSB N Divider Programming	RW	CPU M/N programming.		X
	Bit 6	Reserved					X
	Bit 5	Reserved					X
	Bit 4	Reserved					X
	Bit 3	CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	CPUDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	CPUDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	CPUDiv0		RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	X

SMBUS Table: SB_SRC Frequency Control Register

Byte	16	Name	Control Function	Type	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 16 and 17 configure the SB_SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div1	N Divider Prog bit 1	RW			X
	Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
	Bit 4	M Div4		RW			X
	Bit 3	M Div3		RW			X
	Bit 2	M Div2		RW			X
	Bit 1	M Div1		RW			X
	Bit 0	M Div0		RW			X

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SMBUS Table: SB_SRC Frequency Control Register

Byte	17	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 16 and 17 configure the SB_SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	18	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	Bytes 18 and 19 set the the SB_SRC spread pecentages. Please contact ICS for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	19	Name	Control Function	Type	0	1	Default
	Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	Bytes 18 and 19 set the the SB_SRC spread pecentages. Please contact ICS for the appropriate values.		X
	Bit 6	SSP14		RW			X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

SMBUS Table: SB_SRC Output Divider Control Register

Byte	20	Name	Control Function	Type	0	1	Default
	Bit 7	SB_SRC NDiv0	LSB N Divider Programming	RW	SB_SRC M/N programming.		X
	Bit 6	Reserved					X
	Bit 5	Reserved					X
	Bit 4	Reserved					X
	Bit 3	SB_SRCDiv3	SRC Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	SB_SRCDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	SB_SRCDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	SB_SRCDiv0		RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	X

SMBus Table: Device ID register

Byte	21	Name	Control Function	Type	0	1	Default
	Bit 7	Device ID7	Device ID	R	76 hex		0
	Bit 6	Device ID6		R			1
	Bit 5	Device ID5		R			1
	Bit 4	Device ID4		R			1
	Bit 3	Device ID3		R			0
	Bit 2	Device ID2		R			1
	Bit 1	Device ID1		R			1
	Bit 0	Device ID0		R			0

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SMBus Table: CLKREQ# Configuration Register

Byte 22	Name	Control Function	Type	0	1	Default
Bit 7	CPU/HTT/SRC/ATIG M/N En	CPU/HTT/SRC/ATIG PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	SB_SRC M/N En	SB_SRC M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	X
Bit 1	Reserved	Reserved	RW	-	-	X
Bit 0	Reserved	Reserved	RW	-	-	X

SMBus Table: CLKREQ# Configuration Register

Byte 23	Name	Control Function	Type	0	1	Default
Bit 7	Reserved	Reserved	RW	-	-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	CLKREQ4#_Enable	CLKREQ4# controls SRC5	RW	Not Controlled	Controlled	1
Bit 4	CLKREQ4#_Enable	CLKREQ4# controls SRC4	RW	Not Controlled	Controlled	1
Bit 3	CLKREQ3#_Enable	CLKREQ3# controls SRC3	RW	Not Controlled	Controlled	1
Bit 2	CLKREQ2#_Enable	CLKREQ2# controls SRC2	RW	Not Controlled	Controlled	1
Bit 1	CLKREQ1#_Enable	CLKREQ1# controls SRC1	RW	Not Controlled	Controlled	1
Bit 0	CLKREQ0#_Enable	CLKREQ0# controls SRC0	RW	Not Controlled	Controlled	1

SMBus Table: Test Mode Configuration Register

Byte 24	Name	Control Function	Type	0	1	Default
Bit 7	Test_Md_Sel	Selects Test Mode	**RW**	Normal mode	All ouputs are REF/N	0
Bit 6	DIAG Enable#	DIAG enable CPU and LCD PLL	RW	Reset forces B24[6:4,2,0] to 0	DIAG mode Enabled	0
Bit 5	CPU PLL_LOCK signal	CPU PLL Lock Detect	R	unlocked	Locked	HW
Bit 4	27MHz PLL_LOCK signal	27MHz PLL Lock Detect	R	unlocked	Locked	HW
Bit 3	Fixed PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
Bit 2	SRC PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
Bit 1	Frequency Check	Primary PLL or external crystal Frequency Accuracy	R	Not Accurate	Accurate	HW
Bit 0	PWRGD Status	Power on Reset Status	R	Invalid voltage levels on any of the VDDs. CKPWRGD is not asserted or external XTAL not detected.	Valid voltage levels exist on all the VDD. CKPWRGD is asserted and external XTAL is detected.	HW

SMBus Table:Slew Rate Select Register

Byte 25	Name	Control Function	Type	0	1	Default
Bit 7	48MHz_1_Slew Rate	Slew Rate Control	RW	These bits program the slew rate of the single ended outputs. The maximum slew rate is 1.9V/ns and the minimum slew rate is 1.1V/ns. The slew rate selection is as follows: 11 = 1.9V/ns 10 = 1.6V/ns 01 = 1.1V/ns 00 = tristated		1
Bit 6						1
Bit 5	REF2_Slew Rate	Slew Rate Control	RW			1
Bit 4						1
Bit 3	REF1_Slew Rate	Slew Rate Control	RW			1
Bit 2						1
Bit 1	REF0_Slew Rate	Slew Rate Control	RW			1
Bit 0						1

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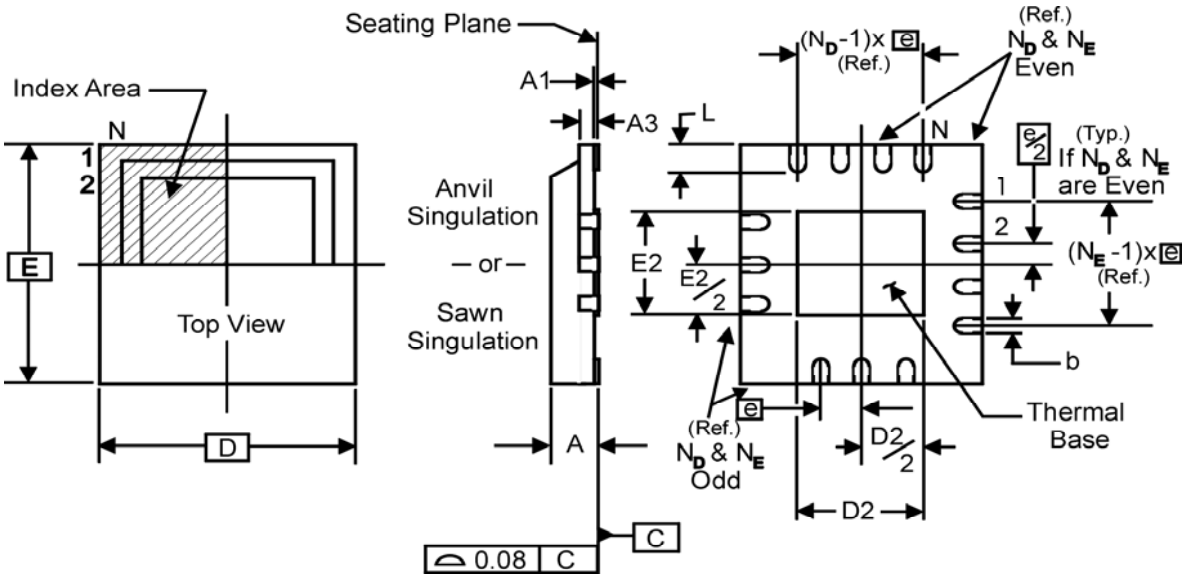

THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	ICS 72L TOLERANCE
N	72
N_D	18
N_E	18
D x E BASIC	10.00 x 10.00
D2 MIN. / MAX.	5.75 / 6.15
E2 MIN. / MAX.	5.75 / 6.15
L MIN. / MAX.	0.30/ 0.50

Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9EPRS488CKLF	Tubes	72-pin MLF	0 to +70° C
9EPRS488CKLFT	Tape and Reel	72-pin MLF	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
Due to package size constraints, actual top-side marking may differ from the full orderable part number.

1616—08/20/09

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Revision History

Rev.	Issue Date	Description	Page #
0.1	7/31/2009	Initial Release	-
A	8/20/2009	Release to final	-

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