

TLX9304

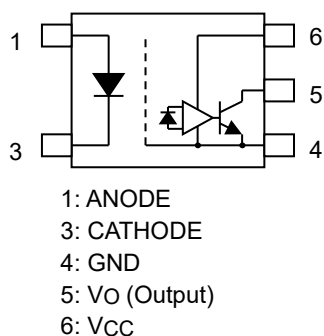
- Unit: mm

The drawing shows the mechanical specifications for the 11-4L1 component. The top view is a rectangle with a circular feature in the bottom-left corner. It has six pins: two on the left (labeled 1 and 3), two on the top (labeled 6, 5, and 4), and two on the right. The width is 4.65 ± 0.28 mm. The side view shows a component with a total width of 7.0 ± 0.4 mm. The mounting surface has a thickness of 0.15 mm. The base has a width of 2.54 mm and a central cutout with a width of 1.27 mm. The distance from the left edge to the start of the cutout is 3.7 +0.26/-0.15 mm. The distance from the left edge to the center of the cutout is 0.1 ± 0.1 mm. The distance from the left edge to the right edge of the cutout is 0.4 mm. The distance from the right edge of the cutout to the right edge of the component is 0.5 min mm.

	JEDEC	JEITA	TOSHIBA
	—	—	11-4L1

Weight: 0.08 g (typ.)

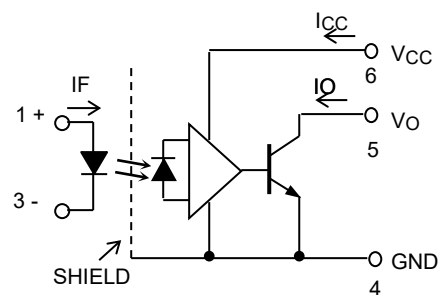
- ## Pin Configuration



Truth Table

Input	LED	Output
H	ON	L
L	OFF	H

Schematic



A ceramic capacitor ($0.1\ \mu\text{F}$) should be connected from pin 6 (VCC) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. The total lead length between capacitor and coupler should not exceed 1 cm.

Absolute Maximum Ratings (Note) (Ta = 25 °C, unless otherwise specified)

Characteristic		Symbol	Rating	Unit
LED	DC Forward Current	I _F	25	mA
	DC Forward Current (Ta=125°C)	I _F	15	mA
	DC Forward Current Derating (Ta ≥ 85°C)	ΔI _F /°C	-0.25	mA/°C
	Peak Transient Forward Current (Note 1)	I _{FPT}	1	A
	Input Power Dissipation	P _D	50	mW
	DC Reverse Voltage	V _R	5	V
DETECTOR	Output Current	I _O	15	mA
	Peak Output Current	I _{OP}	30	mA
	Output Voltage	V _O	-0.5 to 30	V
	Supply Voltage	V _{CC}	-0.5 to 30	V
	Output Power Dissipation	P _O	100	mW
	Output Power Dissipation Derating (Ta ≥ 85°C)	ΔP _O /°C	-1.83	mW/°C
Operating Temperature Range		T _{opr}	-40 to 125	°C
Storage Temperature Range		T _{stg}	-55 to 150	°C
Lead Soldering Temperature (10 s)		T _{sol}	260	°C
Isolation Voltage (R.H. ≤ 60%, AC, 60 s.) (Note 2)		BV _s	3750	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width ≤ 1 μs, 300 pps

Note 2: This device is considered as two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Recommended Operating Conditions (Note)

Characteristic	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{CC}	4.5	-	20	V
Output Voltage	V _O	-	-	V _{CC}	V
Forward Current	I _F	-	10	15	mA
Operating Temperature (Note 1)	T _{opr}	-40	-	125	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: Denotes the operating range, not the recommended operating condition.

Electrical Characteristics (Note)**(Unless otherwise specified, $T_a = -40$ to $125\text{ }^{\circ}\text{C}$, $V_{CC} = 4.5$ to 20 V)**

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Input Forward voltage	V_F	$I_F = 10\text{ mA}$, $T_a = 25^{\circ}\text{C}$	1.45	1.56	1.75	V
		$I_F = 10\text{ mA}$	1.35	—	1.9	
Input Reverse current	I_R	$V_R = 5\text{ V}$, $T_a = 25^{\circ}\text{C}$	—	—	10	μA
Input Capacitance between terminals	C_T	$V_F = 0\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^{\circ}\text{C}$	—	45	—	pF
High level output current	I_{OH}	$I_F = 0\text{ mA}$, $V_O = 20\text{ V}$	—	—	50	μA
Low level output voltage	V_{OL}	$I_F = 10\text{ mA}$, $I_O = 2.4\text{ mA}$	—	0.3	0.6	V
High level supply current	I_{CCH}	$I_F = 0\text{ mA}$	—	—	1.3	mA
Low level supply current	I_{CCL}	$I_F = 10\text{ mA}$	—	—	1.3	mA
Input current logic LOW output	I_{FHL}	$I_O = 0.75\text{ mA}$, $V_O < 0.8\text{ V}$	—	1	5	mA
Input voltage logic HIGH output	V_{FLH}	$I_O = 0.75\text{ mA}$, $V_O > 2.0\text{ V}$	0.8	—	—	V
Output current	I_O	$I_F = 10\text{ mA}$, $V_O = 0.6\text{ V}$	4.0	—	—	mA

Note: All typical values at $V_{CC} = 5\text{ V}$ and $T_a = 25^{\circ}\text{C}$.**Isolation Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$)**

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Stray Capacitance (input to output)	C_S	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	—	0.5	—	pF
Isolation resistance	R_S	$V_S = 500\text{ V}$, R.H. $\leq 60\%$	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s	3750	—	—	V_{rms}

Note : This device is considered as two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Switching Characteristics (Note)**(Unless otherwise specified, $T_a = -40$ to 125°C)**

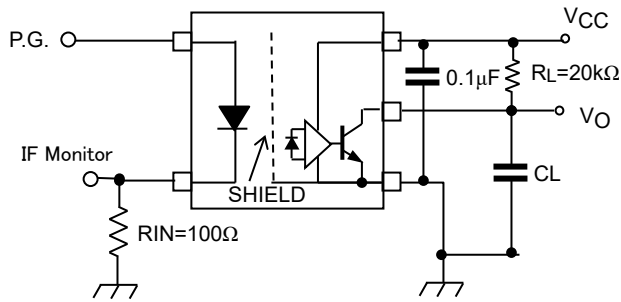
Characteristic	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Propagation delay time (H→L)	t _{pHL} (1)	Fig.1	I _F = 10 mA, R _L = 4.7 kΩ V _{CC} = 5 V	C _L = 100 pF	30	100	400	ns
				C _L = 10 pF	—	90	—	
Propagation delay time (L→H)	t _{pLH} (1)			C _L = 100 pF	200	300	550	
				C _L = 10 pF	—	140	—	
Switching Time Dispersion between ON and OFF	t _{pLH} -t _{pHL} (1)			C _L = 100 pF	0	200	400	
Propagation Delay Skew (Note 1)	t _{psk} (1)				-50	200	450	
Propagation delay time (H→L)	t _{pHL} (2)		I _F = 10 mA, R _L = 20 kΩ V _{CC} = 15 V	C _L = 100 pF	30	150	400	ns
				C _L = 10 pF	—	100	—	
Propagation delay time (L→H)	t _{pLH} (2)			C _L = 100 pF	200	350	550	
				C _L = 10 pF	—	150	—	
Switching Time Dispersion between ON and OFF	t _{pLH} -t _{pHL} (2)			C _L = 100 pF	0	200	400	
Propagation Delay Skew (Note 1)	t _{psk} (2)				-50	200	450	
Common mode transient immunity at high output level (Note 2)	CM _H	Fig.2	V _{CC} = 15 V, C _L = 100 pF, V _{CM} = 1500 V _{p-p} , I _F = 0 mA, R _L = 20 kΩ, T _a =25°C		15	—	—	kV/μs
Common mode transient Immunity at low output level (Note 2)	CM _L		V _{CC} = 15 V, C _L = 100 pF, V _{CM} = 1500 V _{p-p} , I _F = 10 mA, R _L = 20 kΩ, T _a =25°C		-15	—	—	kV/μs

Note: All typical values at $V_{CC} = 5\text{ V}$ and $T_a = 25^\circ\text{C}$.Note 1: The propagation delay skew, t_{psk} , is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).Note 2: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 11\text{ V}$) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1.0\text{ V}$).

Fig. 1: t_{pHL} , t_{pLH}

$I_F = 10\text{mA (P.G.)}$

($f = 10\text{kHz}$, $\text{duty} = 10\%$, $t_r = t_f = 5\text{ns}$)



C_L includes probe and stray capacitance.
P.G.: Pulse generator

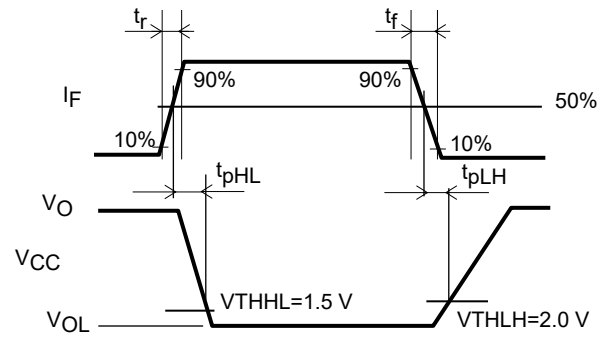
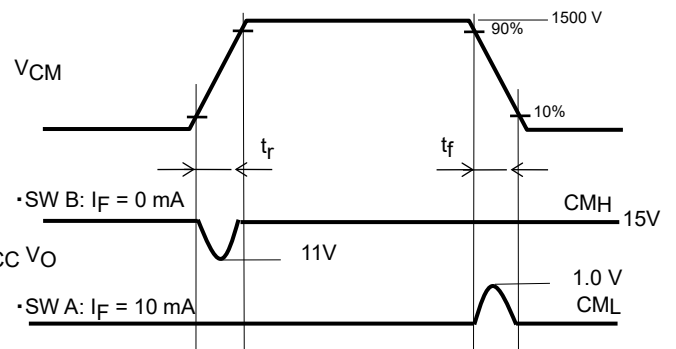
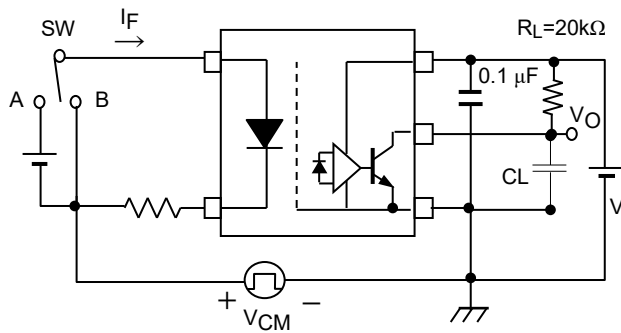
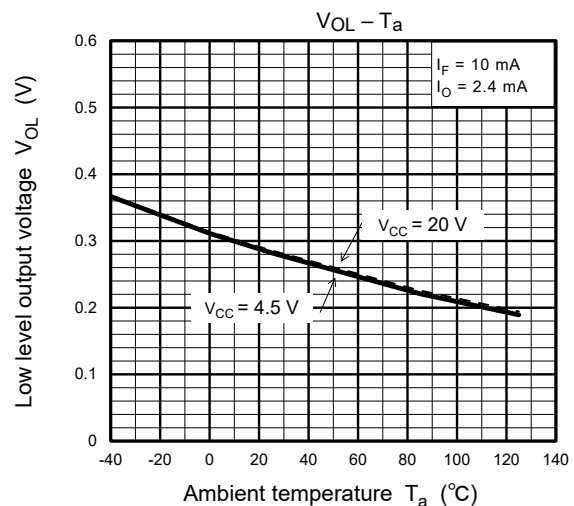
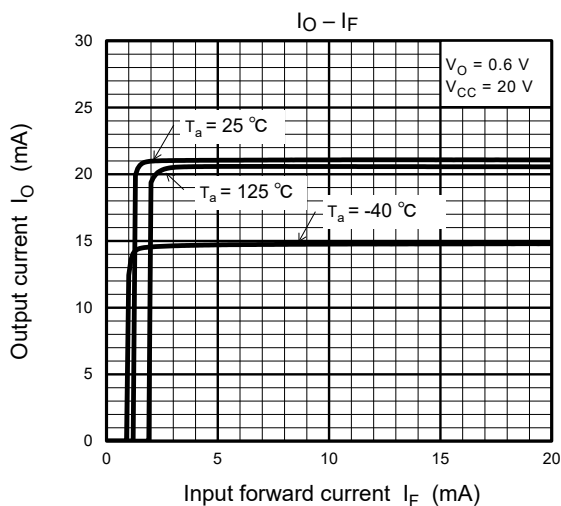
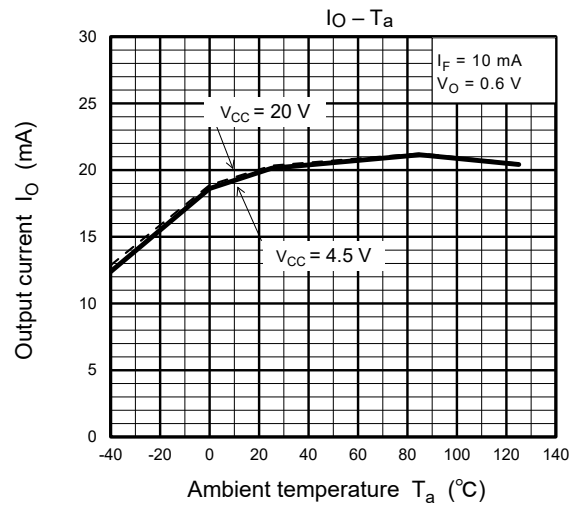
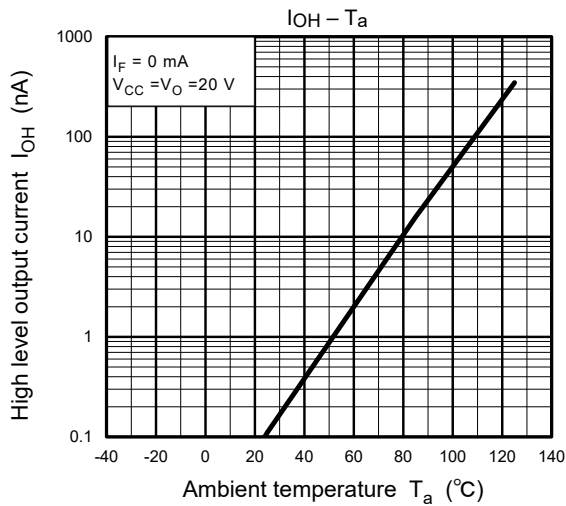
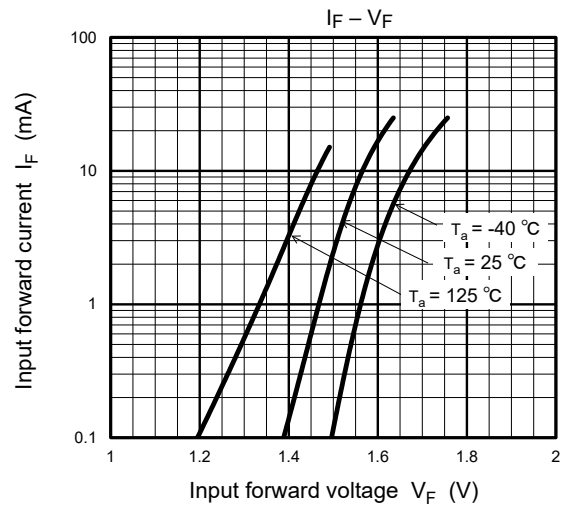
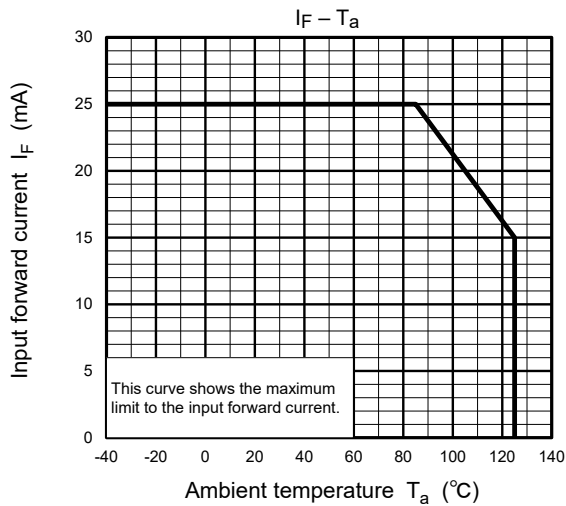


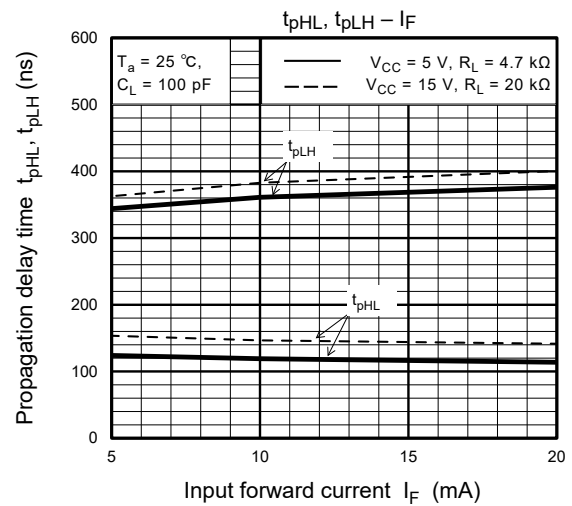
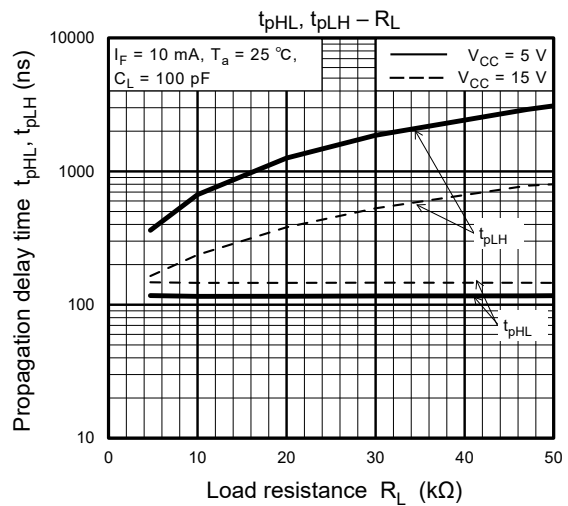
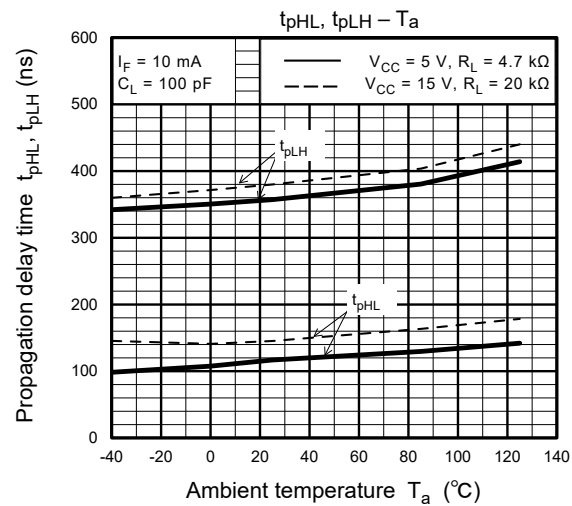
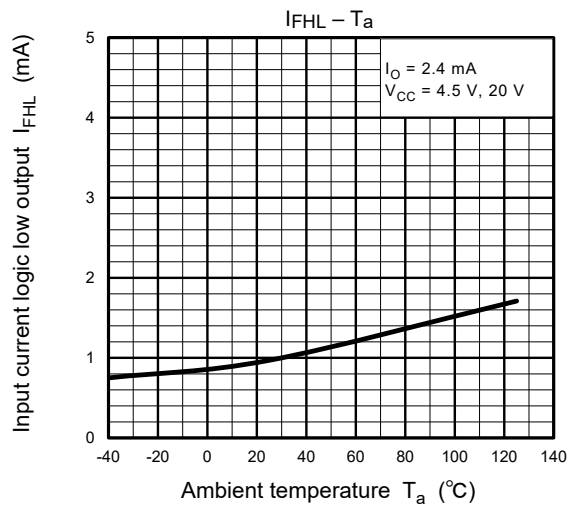
Fig. 2: CM_H , CM_L



$$CM_H = \frac{1200(V)}{tr(\mu s)} \quad CM_L = -\frac{1200(V)}{tf(\mu s)}$$

Characteristics Curves (Note)





Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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