

RJK0330DPB-01

Silicon N Channel Power MOS FET
Power Switching

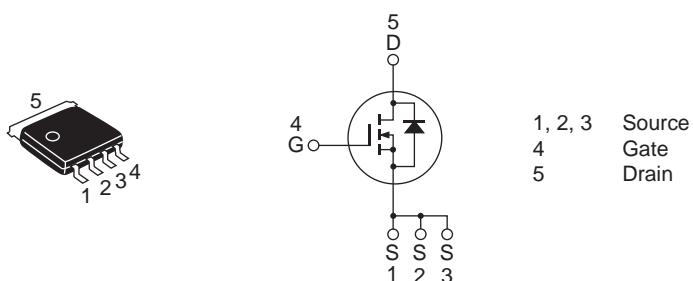
R07DS0266EJ0500
(Previous: REJ03G1639-0400)
Rev.5.00
Mar 01, 2011

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 2.1 \text{ m}\Omega \text{ typ. (at } V_{GS} = 10 \text{ V)}$
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	45	A
Drain peak current	$I_{D(\text{pulse})}$ ^{Note 1}	180	A
Body-drain diode reverse drain current	I_{DR}	45	A
Avalanche current	I_{AP} ^{Note 2}	22	A
Avalanche energy	E_{AR} ^{Note 2}	48.4	mJ
Channel dissipation	P_{ch} ^{Note 3}	55	W
Channel to case thermal resistance	θ_{ch-c} ^{Note 3}	2.27	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. $T_c = 25^\circ\text{C}$

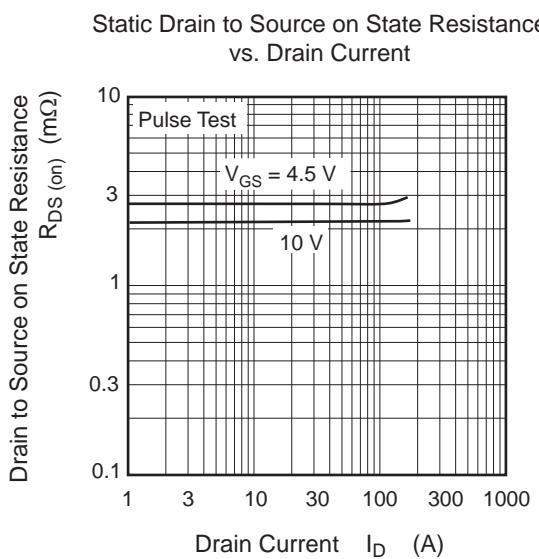
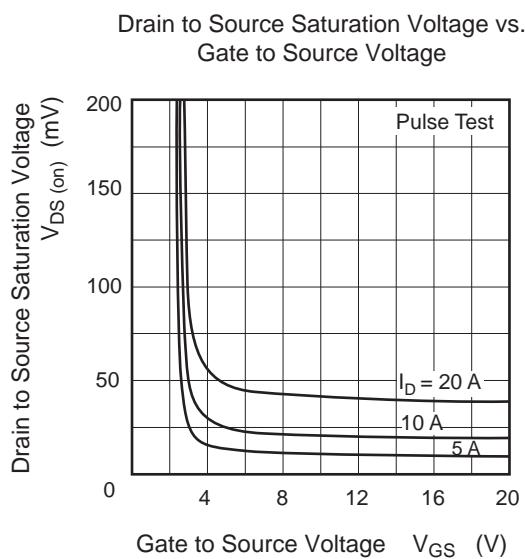
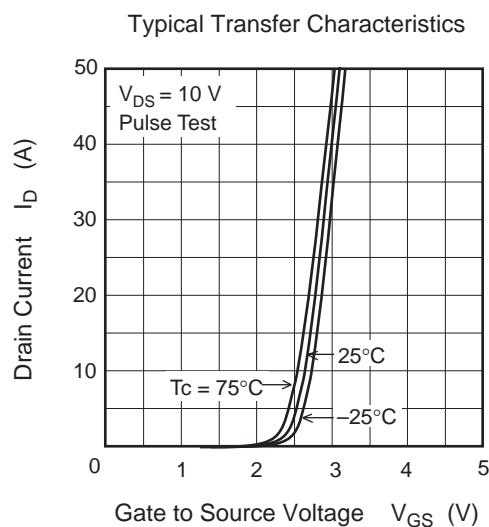
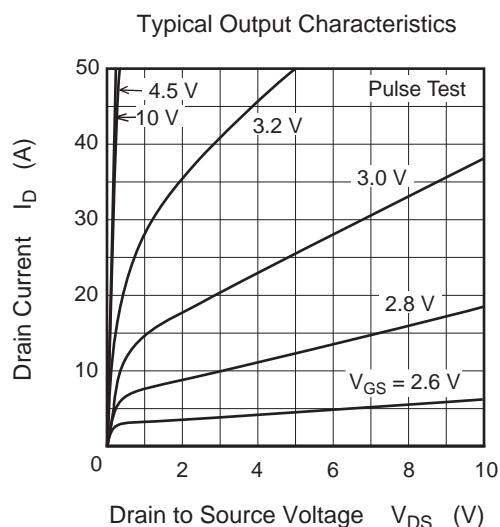
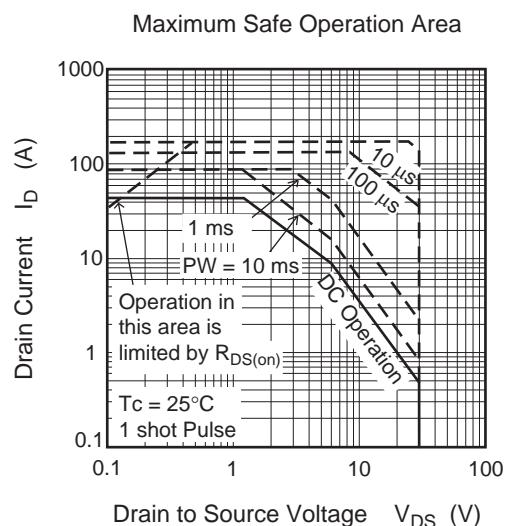
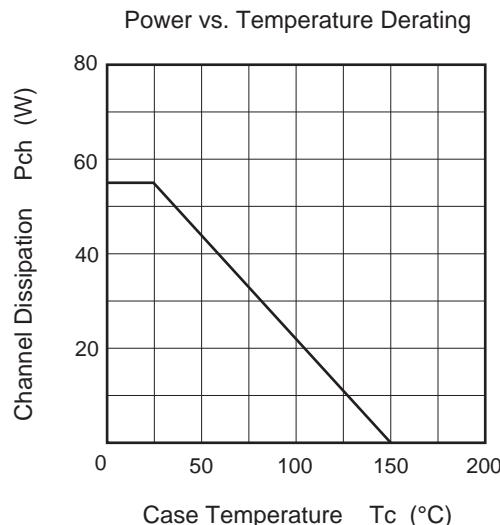
Electrical Characteristics

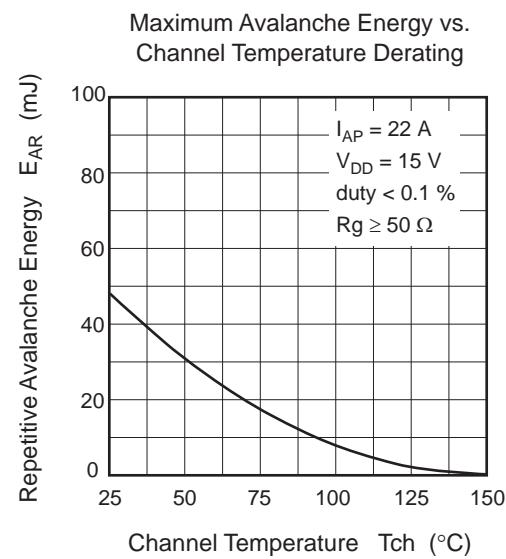
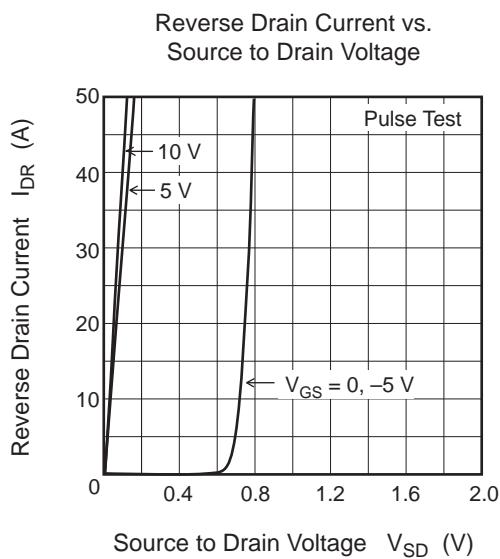
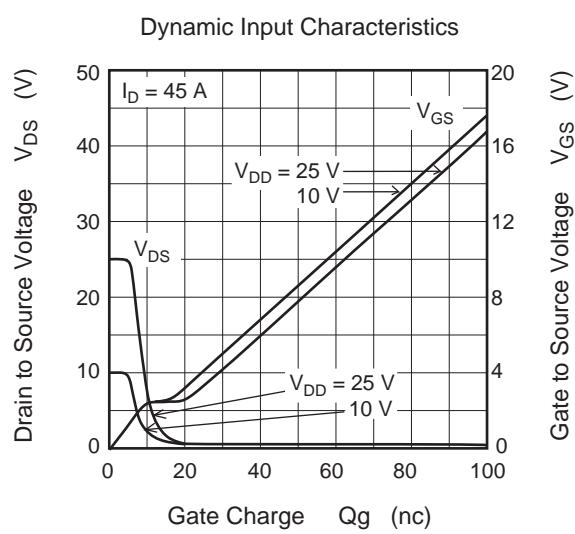
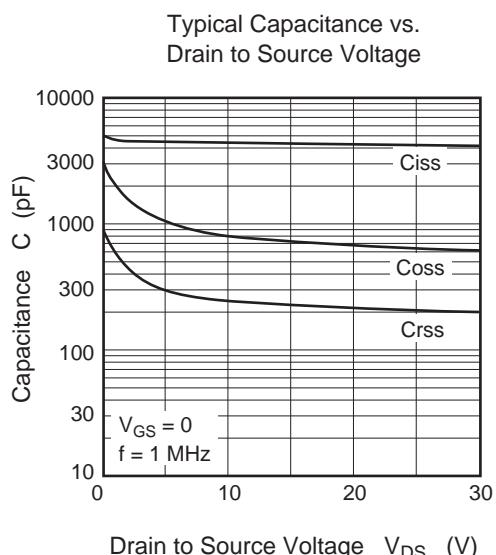
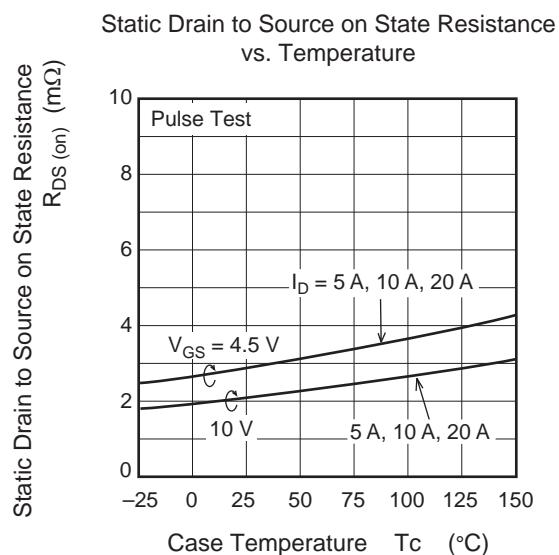
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	30	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±20 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 30 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.2	—	2.5	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	2.1	2.7	mΩ	I _D = 22.5 A, V _{GS} = 10 V ^{Note4}
	R _{DS(on)}	—	2.8	3.9	mΩ	I _D = 22.5 A, V _{GS} = 4.5 V ^{Note4}
Forward transfer admittance	y _{fs}	—	90	—	S	I _D = 22.5 A, V _{DS} = 10 V ^{Note4}
Input capacitance	C _{iss}	—	4300	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	800	—	pF	
Reverse transfer capacitance	C _{rss}	—	245	—	pF	
Gate Resistance	R _g	—	0.4	—	Ω	
Total gate charge	Q _g	—	27	—	nC	V _{DD} = 10 V, V _{GS} = 4.5 V, I _D = 45 A
Gate to source charge	Q _{gs}	—	10.5	—	nC	
Gate to drain charge	Q _{gd}	—	5.8	—	nC	
Turn-on delay time	t _{d(on)}	—	6.8	—	ns	V _{GS} = 10 V, I _D = 22.5 A, V _{DD} ≈ 10 V, R _L = 0.44 Ω, R _g = 4.7 Ω
Rise time	t _r	—	3.9	—	ns	
Turn-off delay time	t _{d(off)}	—	50	—	ns	
Fall time	t _f	—	5.4	—	ns	
Body-drain diode forward voltage	V _{DF}	—	0.78	1.02	V	I _F = 45 A, V _{GS} = 0 ^{Note4}
Body-drain diode reverse recovery time	t _{rr}	—	36	—	ns	I _F = 45 A, V _{GS} = 0 di _F /dt = 100 A/μs
Body-drain diode reverse recovery charge	Q _{rr}	—	34	—	nC	

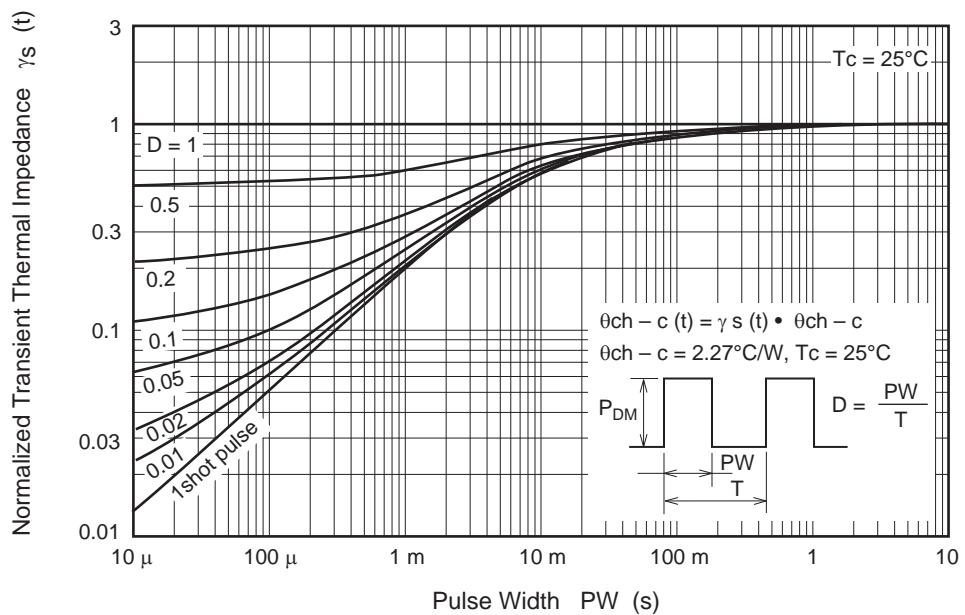
Notes: 4. Pulse test

Main Characteristics

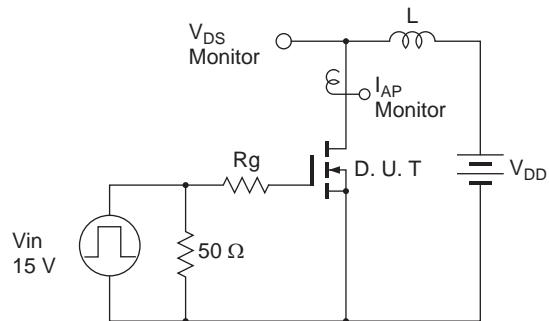




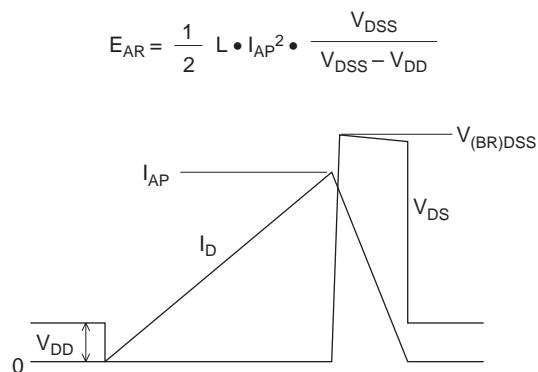
Normalized Transient Thermal Impedance vs. Pulse Width



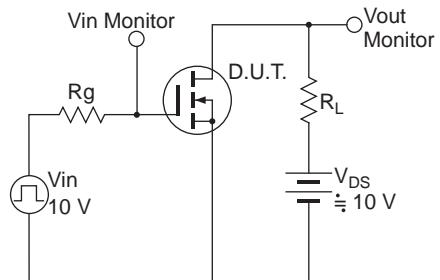
Avalanche Test Circuit



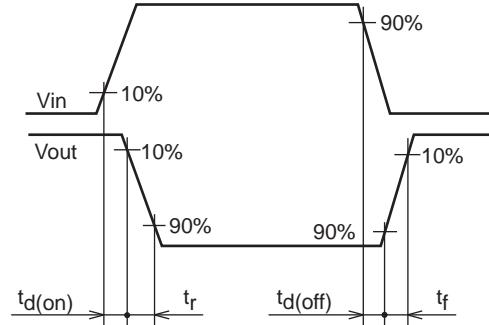
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
LFPACK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g	

(Ni/Pd/Au plating)

Ordering Information

Part No.	Quantity	Shipping Container
RJK0330DPB-01-J0	2500 pcs	Taping

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