

MOSFET

OptiMOS™ Small Signal Transistor, -60 V

Features

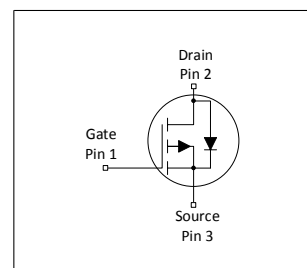
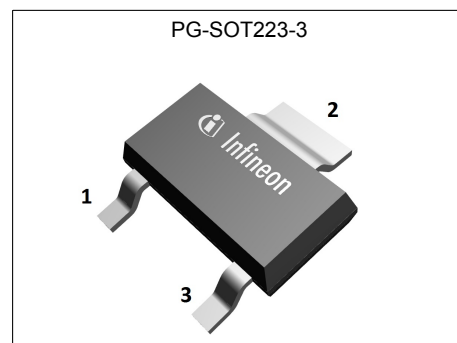
- P-Channel
- Very low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- Normal Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	125	m Ω
I_D	-2.8	A



Type / Ordering Code	Package	Marking	Related Links
ISP13DP06NMS	PG-SOT223-3	13DP06NS	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-2.8	A	$V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=70\text{ °C/W}$
Continuous drain current ¹⁾	I_D	-	-	-1.7	A	$V_{GS}=-10\text{ V}$, $T_A=100\text{ °C}$, $R_{THJA}=70\text{ °C/W}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	-11.2	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	608	mJ	$I_D=-3.0\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	5.0 1.8	W	$T_S=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=70\text{ °C/W}^{1)}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - soldering point	R_{thJS}	-	-	25	°C/W	-
Device on PCB, 6 cm ² cooling area ¹⁾	R_{thJA}	-	-	70	°C/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	-2.1	-3	-4	V	$V_{DS}=V_{GS}$, $I_D=-520\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	1 -100	μA	$V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	100	125	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-2.8\text{ A}$
Gate resistance	R_G	-	5	-	Ω	-
Transconductance	g_{fs}	-	5.2	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=-2.8\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	790	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	120	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	30	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-2.8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-2.8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	23	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-2.8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-2.8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-3.5	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-2.4	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate to drain charge	Q_{gd}	-	-6.9	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Switching charge	Q_{sw}	-	-8.0	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge total	Q_g	-	-20.2	-	nC	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-4.4	-	V	$V_{DD}=-30\text{ V}$, $I_D=-2.8\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge	Q_{oss}	-	-8.7	-	nC	$V_{DD}=-30\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ See diagram, Gate charge waveforms, for gate charge parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-1.5	A	$T_A=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-6	A	$T_A=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.78	-1.2	V	$V_{GS}=0\text{ V}$, $I_F=-1.5\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	33	-	ns	$V_R=-30\text{ V}$, $I_F=-1.5\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	-63	-	nC	$V_R=-30\text{ V}$, $I_F=-1.5\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

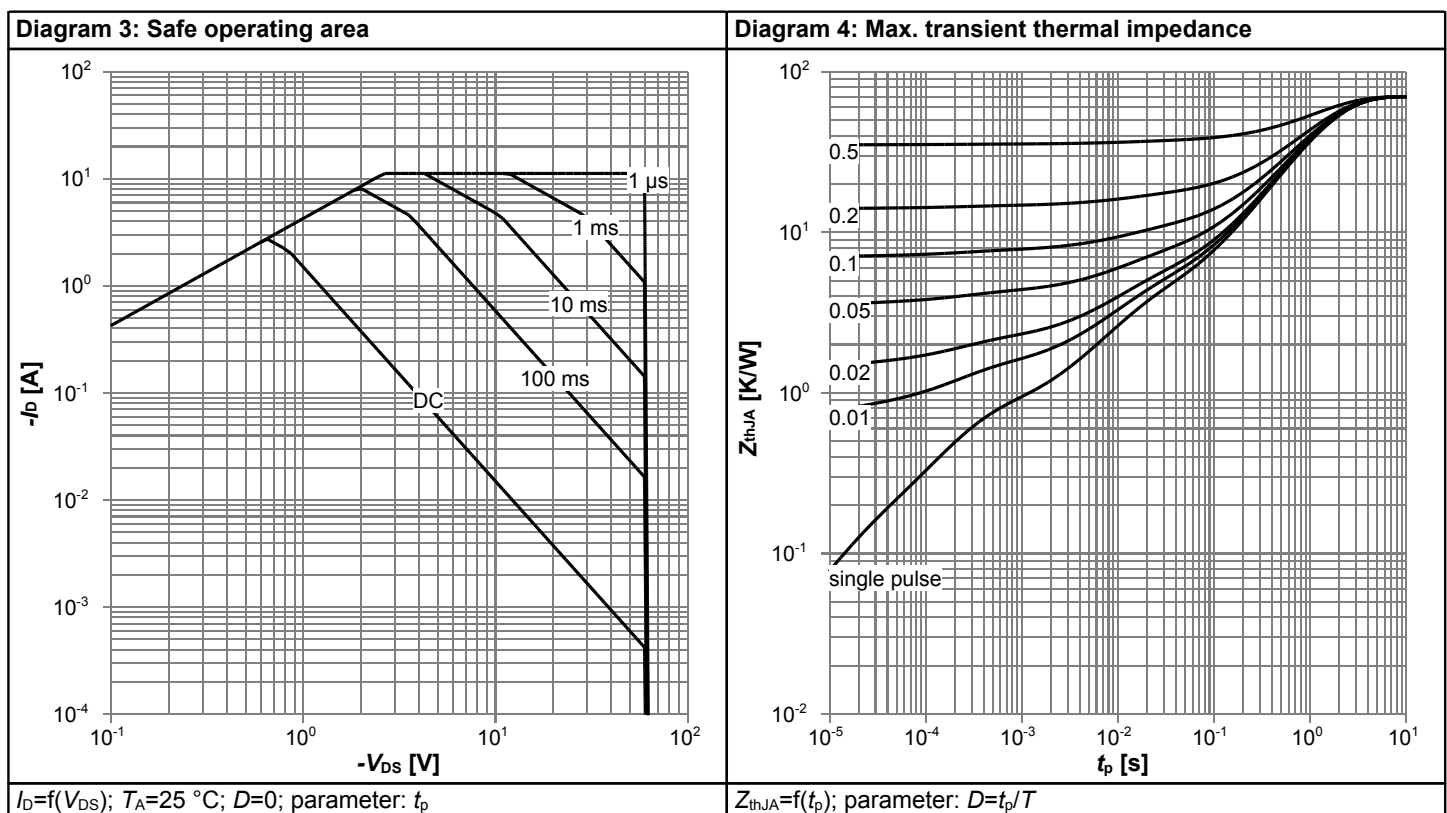
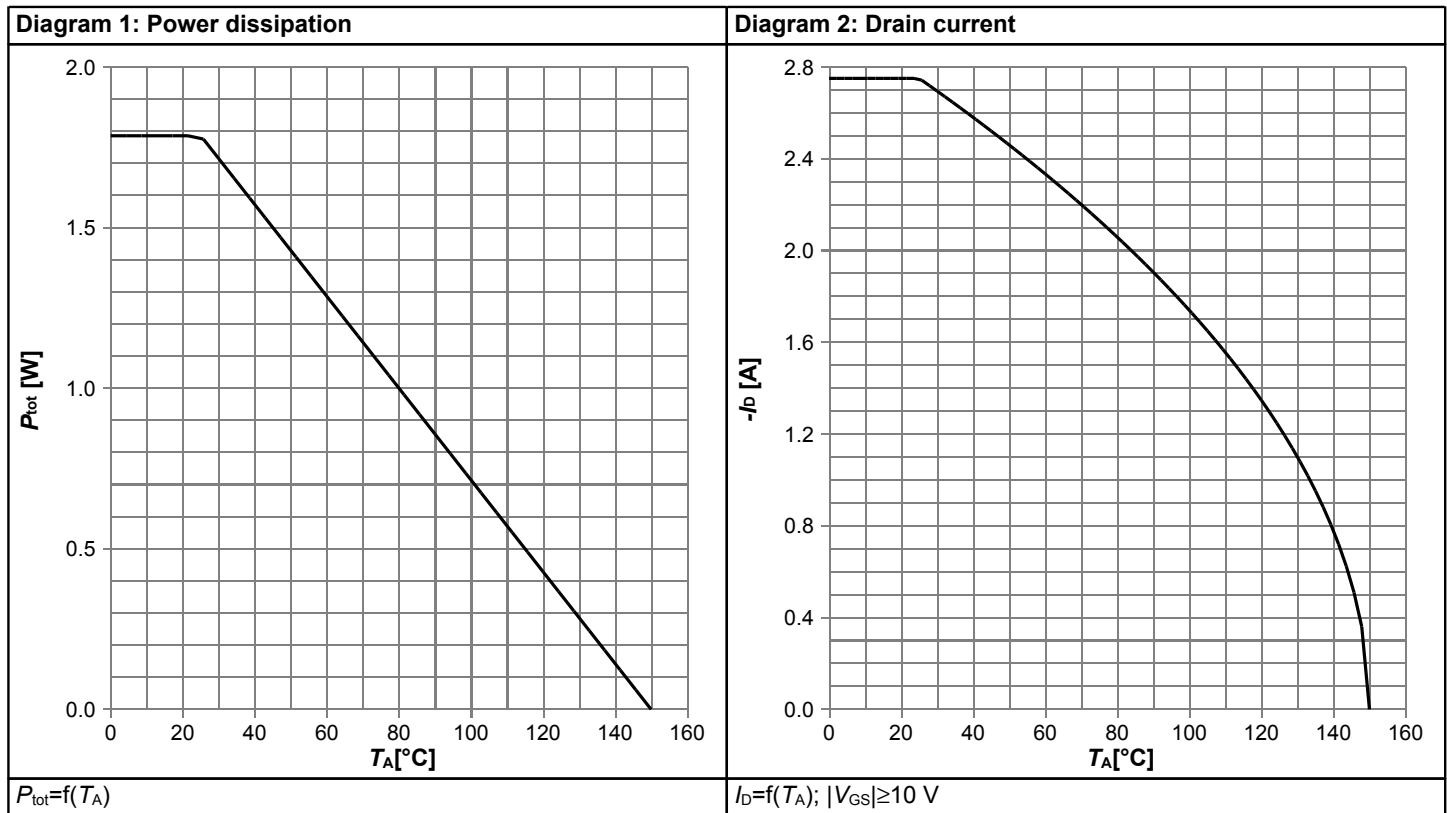
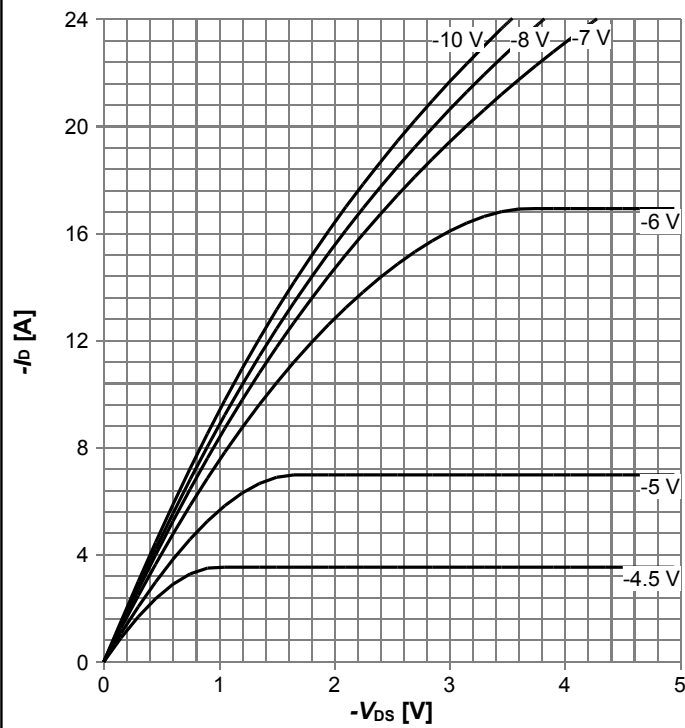
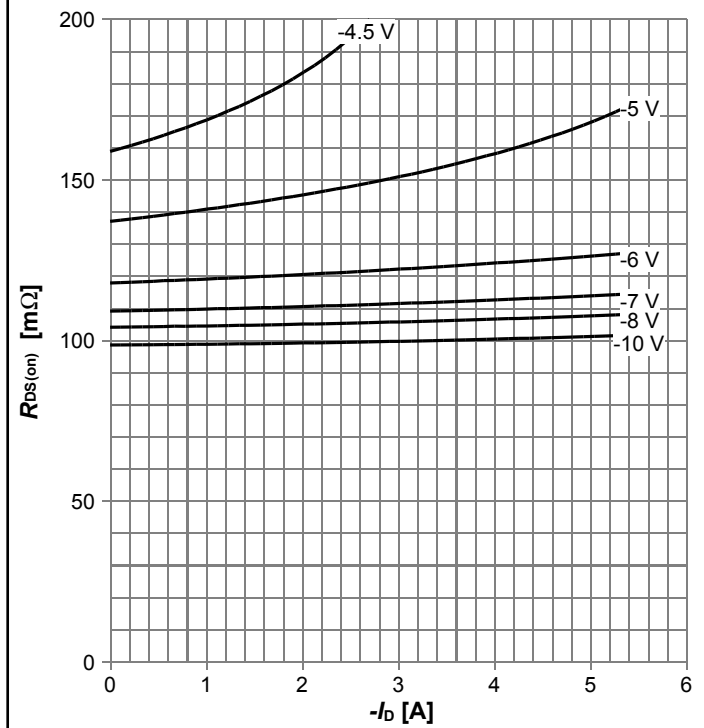


Diagram 5: Typ. output characteristics



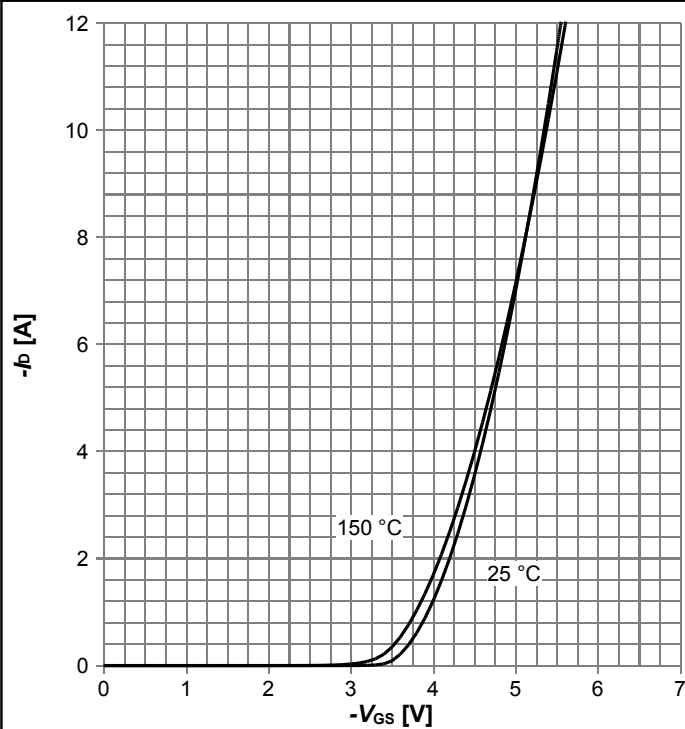
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



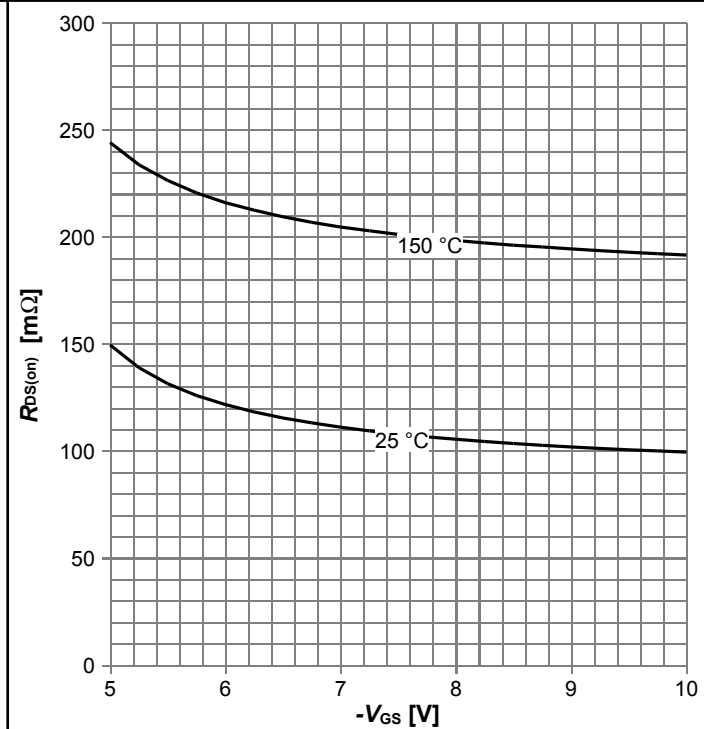
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



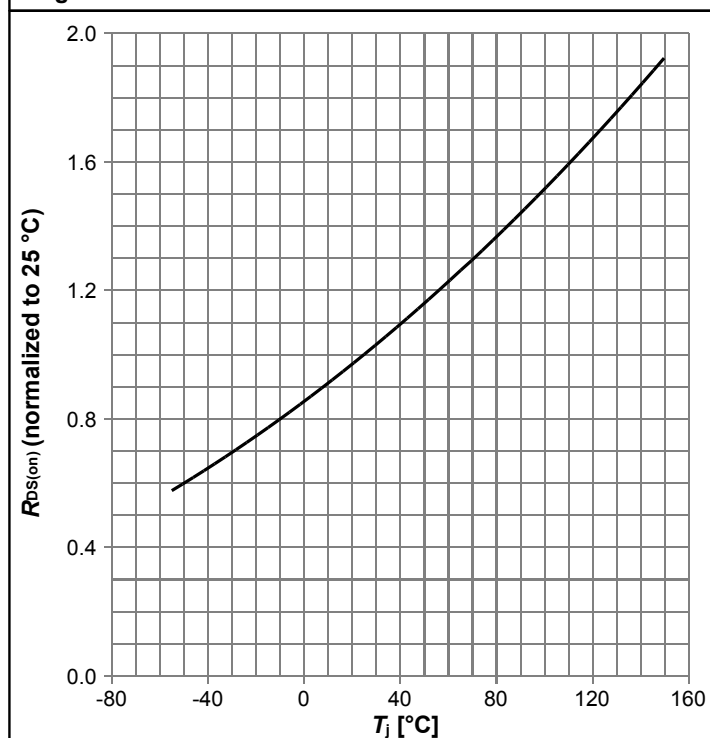
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



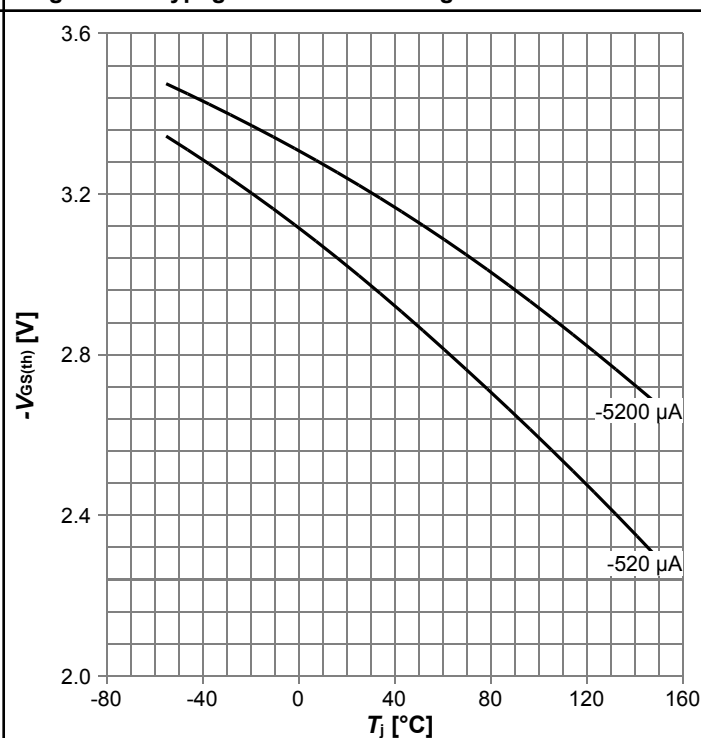
$R_{DS(on)} = f(V_{GS})$, $I_D = -2.8$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



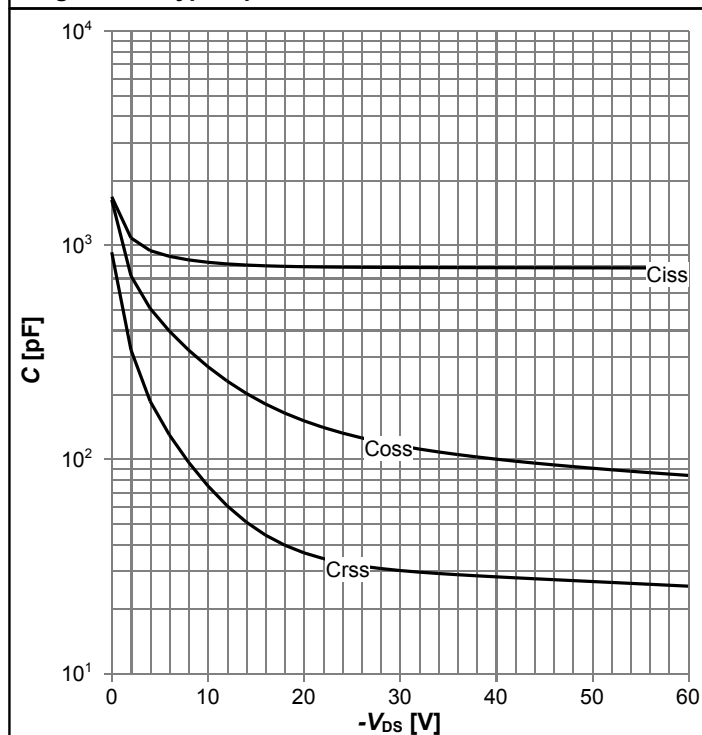
$R_{DS(on)} = f(T_j)$, $I_D = -2.8$ A, $V_{GS} = -10$ V

Diagram 10: Typ. gate threshold voltage



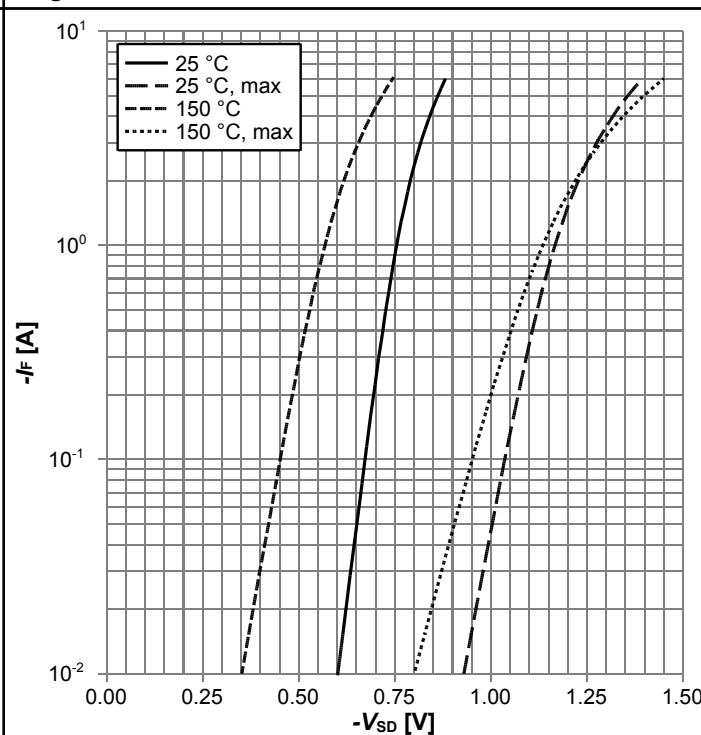
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



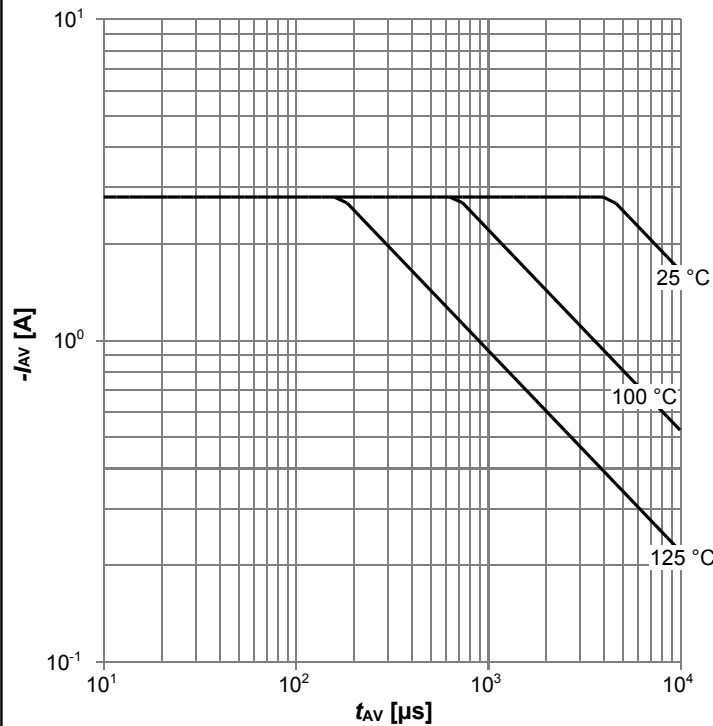
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



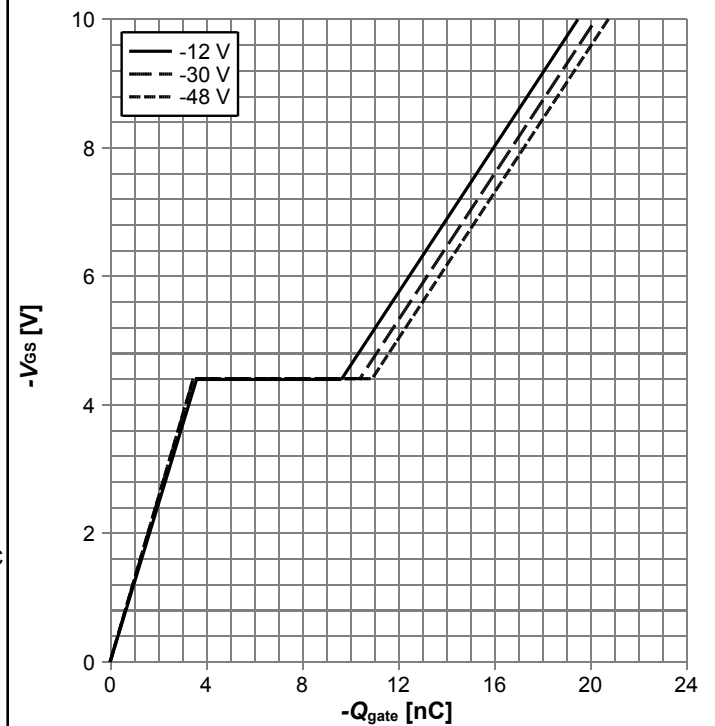
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



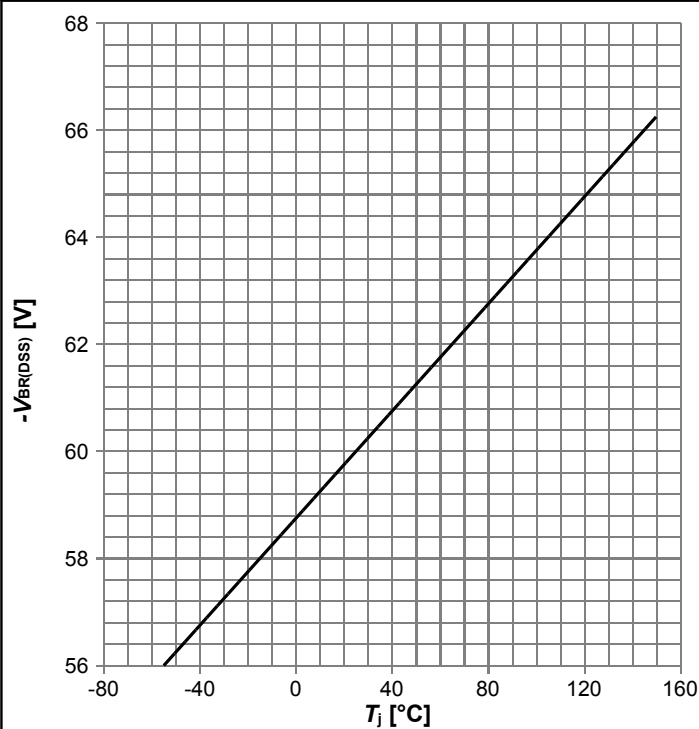
$I_{AS}=f(t_{AV})$; $R_{GS}=25\text{ }\Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate})$, $I_D=-2.8\text{ A}$ pulsed, $T_j=25\text{ }^{\circ}\text{C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

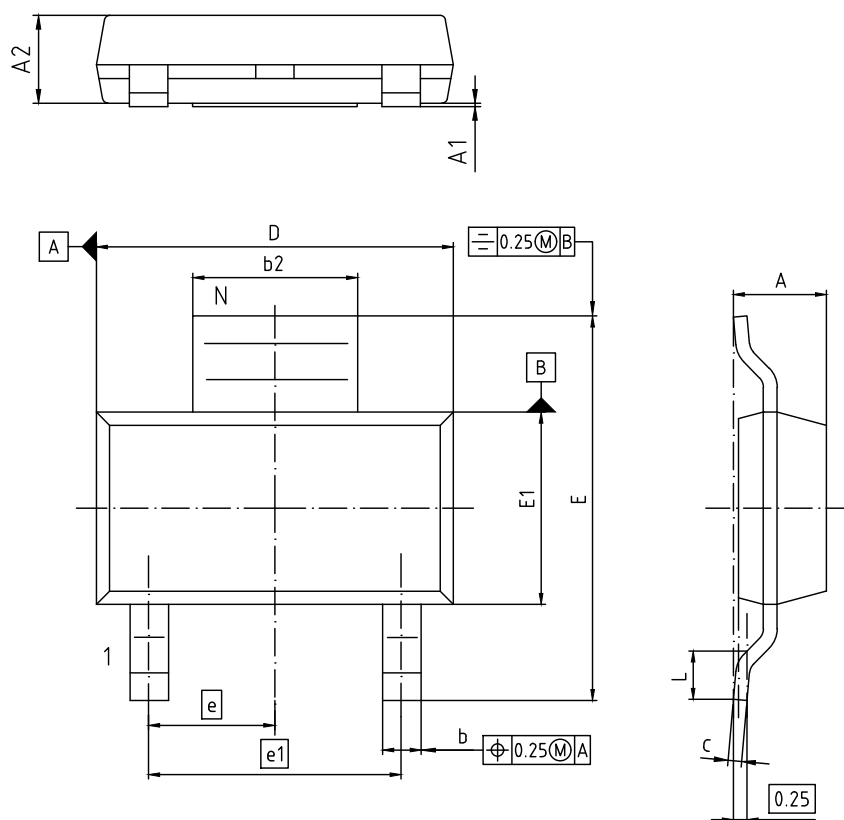


$V_{BR(DSS)}=f(T_j)$; $I_D=-250\text{ }\mu\text{A}$

Diagram Gate charge waveforms



5 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

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REVISION 01

Figure 1 Outline PG-SOT223-3, dimensions in mm/inches

Revision History

ISP13DP06NMS

Revision: 2019-01-30, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-01-22	Release of final version
2.1	2019-01-30	Update package drawings

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