

120mΩ, 2.5A Power Switch with Adjustable Current Limit

General Description

The RT2528A is a cost effective, low voltage, P-MOSFET power switch IC with an adjustable current limit feature. Low on-resistance (74mΩ typ.) and low supply current (120μA typ.) are designed in this IC.

The RT2528A offers an adjustable current limit threshold between 0.5A and 2.5A (typ.) via an external resistor. The ±10% current limit accuracy can be realized for all current limit settings.

The RT2528A is an ideal solution for power supply applications since it is functional for various current limit requirements. The RT2528A is available in the thermal enhanced SOP-8 (Exposed Pad) package.

Ordering Information

RT2528A □ □

- Package Type
SP : SOP-8 (Exposed Pad-option 2)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT2528A
GSPYMDNN

RT2528AGSP : Product Number

YMDNN : Date Code

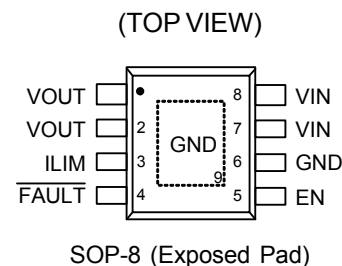
Features

- Adjustable Current Limit : 0.5A to 2.5A (typ.)
- ±10% Current Limit Accuracy @ 2A Over Temperature
- 120mΩ (max) P-MOSFET
- Low Supply Current : 120μA
- Input Operating Voltage Range : 2.5V to 5.5V
- Reverse Input-Output Voltage Protection
- Built-in Soft-Start
- AEC-Q100 Grade 3 Qualified
- RoHS Compliant and Halogen Free

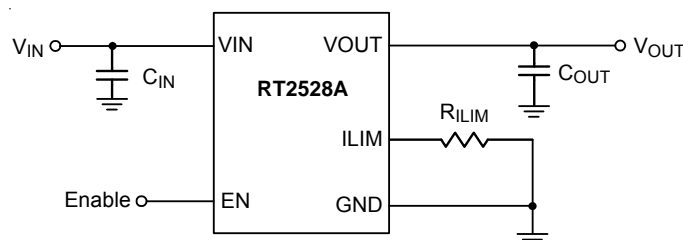
Applications

- Automotive Audio, Navigation & Info Systems
- Industrial Grade General Purpose Point of Load
- Digital Set Top Boxes
- Vehicle Electronics

Pin Configuration



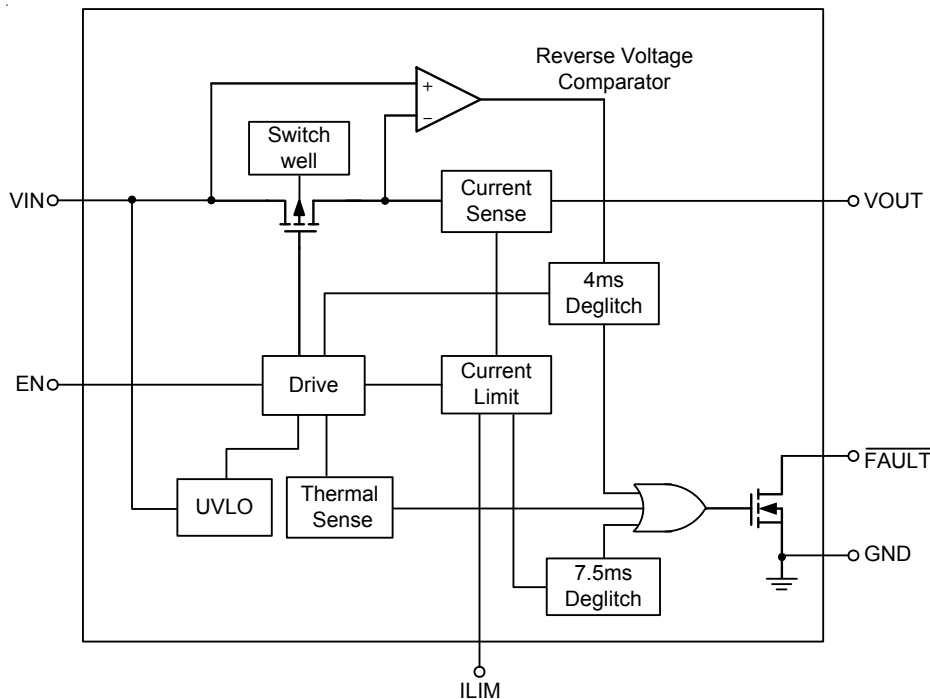
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VOUT	Output.
3	ILIM	Current limit setting. Connect an external resistor is used to set current limit threshold, and $10\text{k}\Omega \leq R_{ILIM} \leq 49.9\text{k}\Omega$ is recommended.
4	$\overline{\text{FAULT}}$	Active-low open-drain output. Asserted during over-current, over-temperature, or reverse-voltage conditions.
5	EN	Enable control input. Logic high turns on the power switch.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7, 8	VIN	Power input. Connect a $10\mu\text{F}$ or greater ceramic capacitor from the VIN to GND as close to the IC as possible.

Functional Block Diagram



Operation

The RT2528A is a current-limited power switch using P-MOSFETs for applications where short-circuit or heavy capacitive loads will be encountered. These devices allow users to adjust the current limit threshold between 500mA and 2.5A (typ.) via an external resistor. Additional device shutdown features include over-temperature protection and reverse-voltage protection.

The RT2528A provides built-in soft-start function. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rising time and falling time of the output voltage to limit large inrush current and voltage surges. The RT2528A enters constant-current mode when the load exceeds the current limit threshold.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage, V_{IN}	-----	-0.3V to 6V
Other Pins	-----	-0.3V to 6V
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$		
SOP-8 (Exposed Pad)	-----	2.041W
Package Thermal Resistance (Note 2)		
SOP-8 (Exposed Pad), θ_{JA}	-----	49°C/W
SOP-8 (Exposed Pad), θ_{JC}	-----	8°C/W
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Junction Temperature	-----	150°C
Storage Temperature Range	-----	-65°C to 150°C
ESD Susceptibility (Note 3)		
HBM (Human Body Model)	-----	2kV

Recommended Operating Conditions (Note 4)

Supply Input Voltage, V_{IN}	-----	2.5V to 5.5V
Temperature Range Junction	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

Electrical Characteristics

($V_{IN} = 5V$, $T_A = T_J = -40^\circ\text{C}$ to 85°C , unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current		ISHDN	V _{EN} = 0V, I _{OUT} = 0A	--	1	5	μA
Quiescent Current		I _Q	I _{OUT} = 0A	--	120	300	μA
EN Input Voltage	Logic-High	V _{IH}		1.2	--	--	V
	Logic-Low	V _{IL}		--	--	0.4	
EN Input Current		I _{EN}	V _{IN} = 5.5V V _{EN} = 0V or 5.5V	--	0.02	0.5	μA
Current Limit Setting Resistor Range		R _{ILIM}		10	--	65	kΩ
Reverse Leakage Current		I _{REV}	V _{OUT} = 5V, V _{IN} = 0V	--	1	10	μA
Static Drain-Source On-State Resistance		R _{DS(ON)}	I _{OUT} = 0.2A	--	74	120	mΩ
Reverse Voltage Comparator Trip Point		I _{REV_HYS}	V _{OUT} – V _{IN}	100	135	300	mV
Current Limit		I _{LIM}	R _{ILIM} = 13kΩ	1800	2000	2200	mA
			R _{ILIM} = 13kΩ, T _A = 25°C	1840	2000	2160	
			R _{ILIM} = 49.9kΩ	468	520	572	
FAULT Deglitch			FAULT assertion or de-assertion due to over-current condition	2	7.5	14	ms
FAULT Flag Assertion Offset		V _{FAULT_OFS}	Offset between fault flag assertion level versus ILIM trigger level (Note 5)	–100	--	0	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown Threshold	T_{SD}	(Note 5)	--	160	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

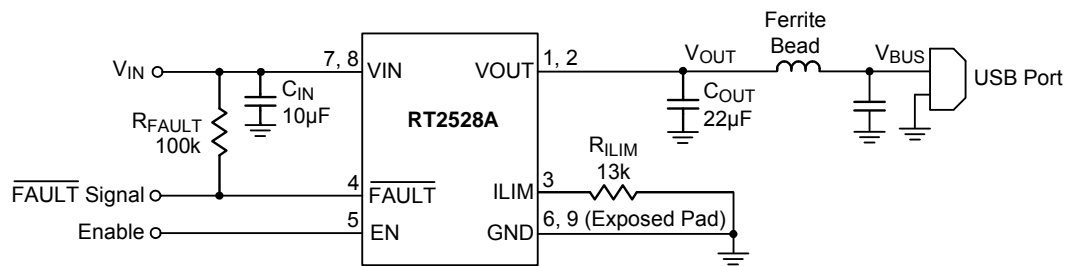
Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^{\circ}\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package. The PCB copper area with exposed pad is 70mm^2 .

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

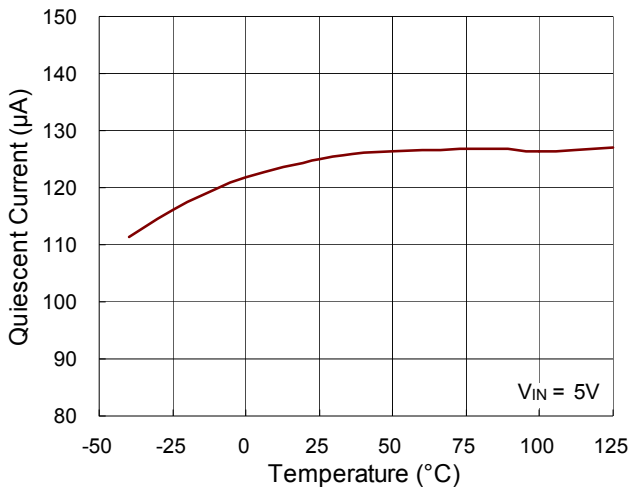
Typical Application Circuit



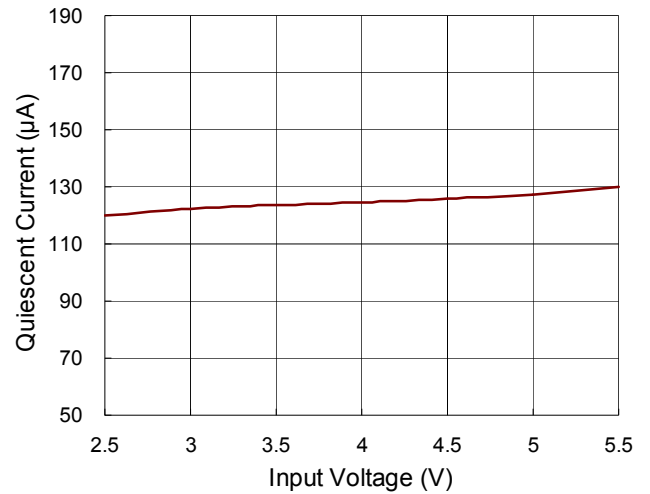
Note : R_{LIM} = 13kΩ for 2A Power Switch Operation

Typical Operating Characteristics

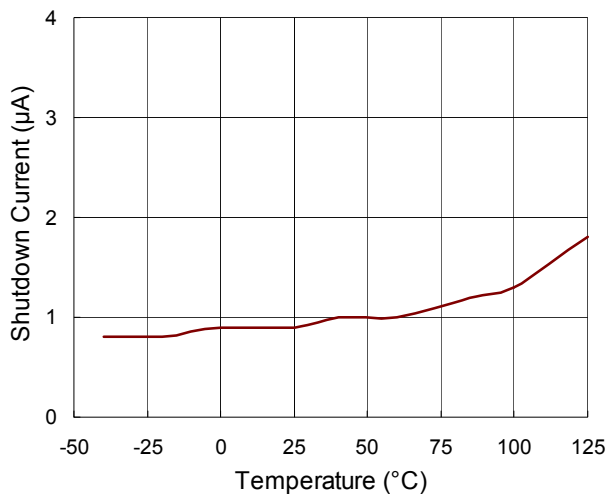
Quiescent Current vs. Temperature



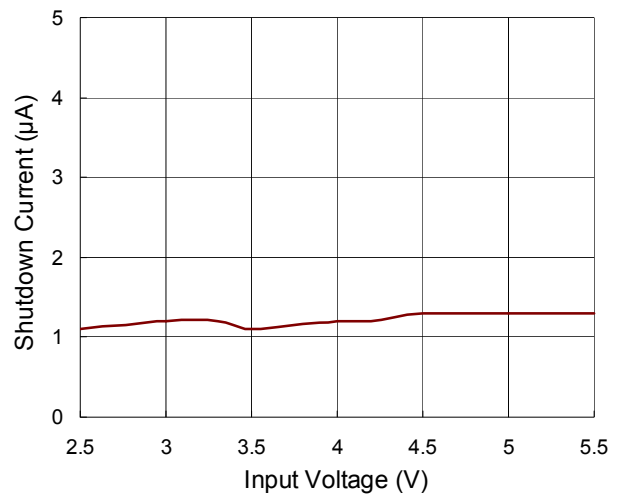
Quiescent Current vs. Input Voltage



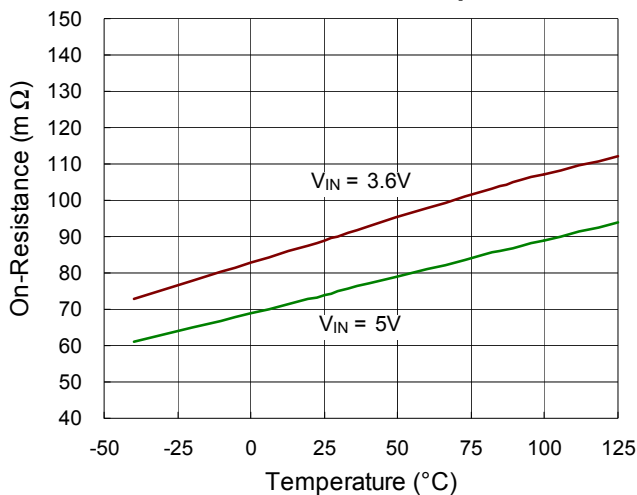
Shutdown Current vs. Temperature



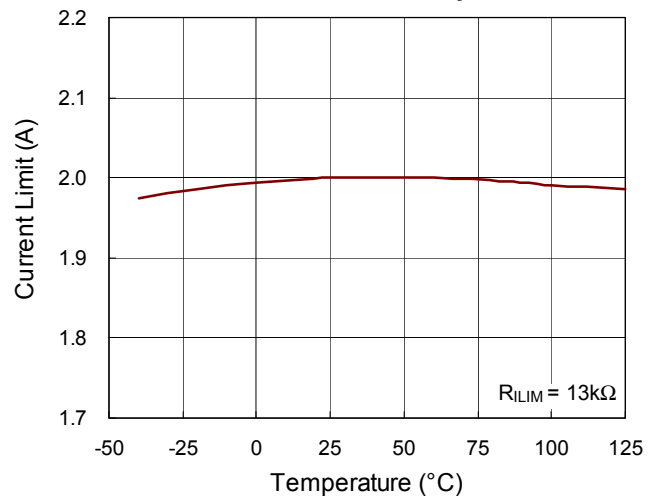
Shutdown Current vs. Input Voltage



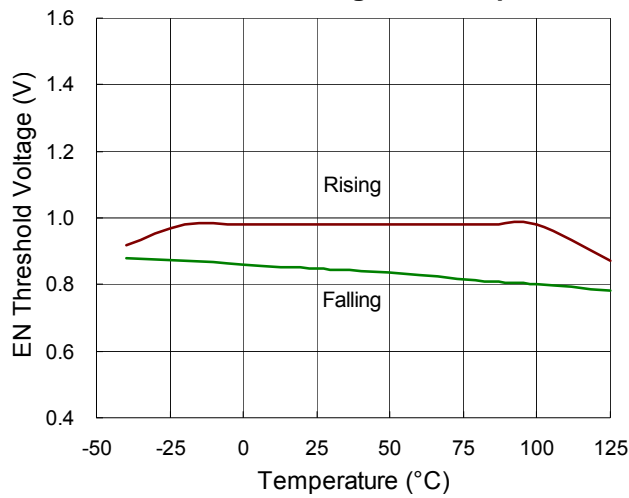
On-Resistance vs. Temperature



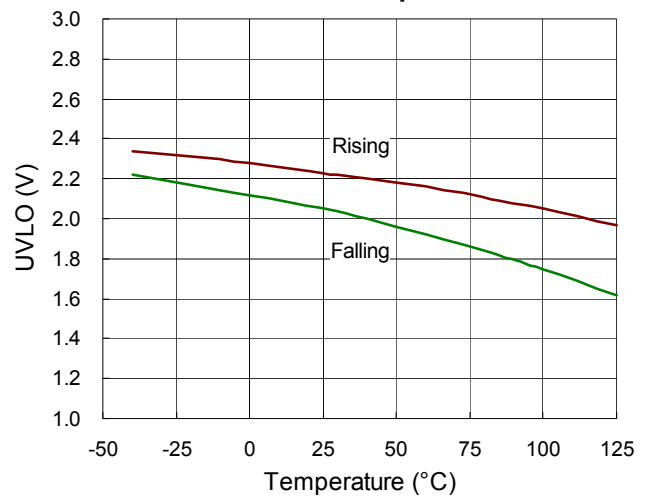
Current Limit vs. Temperature



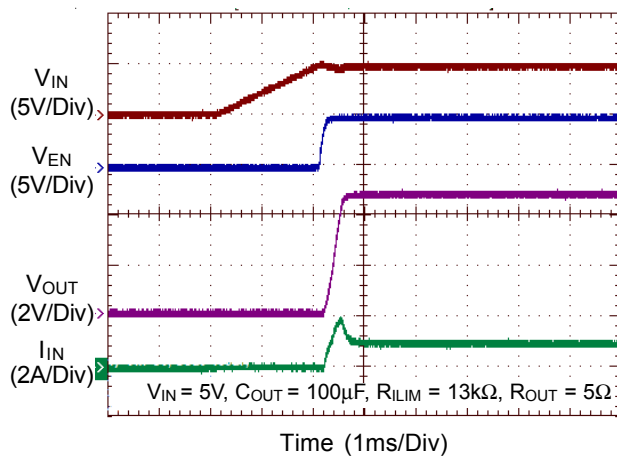
EN Threshold Voltage vs. Temperature



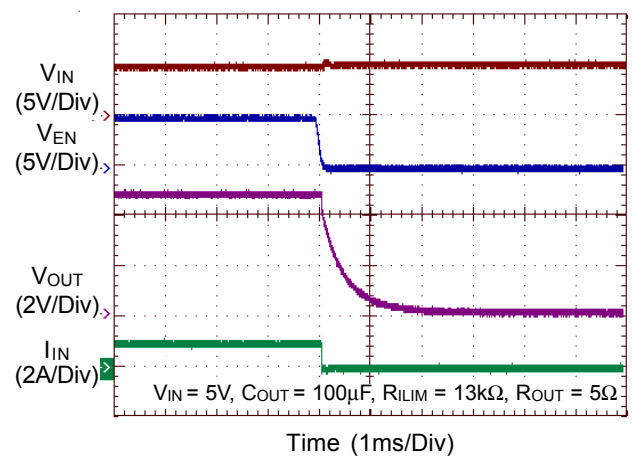
UVLO vs. Temperature



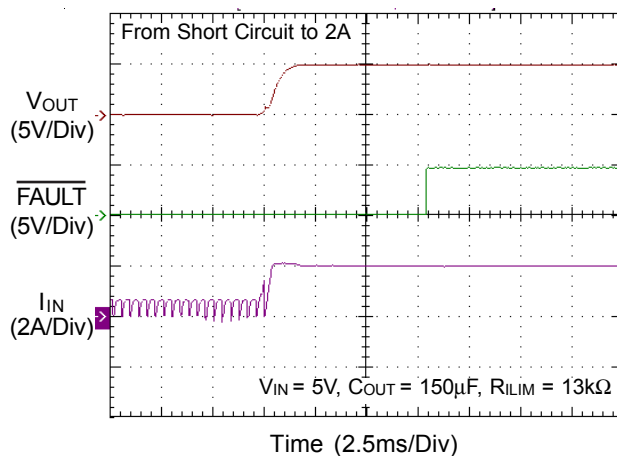
Power On from EN



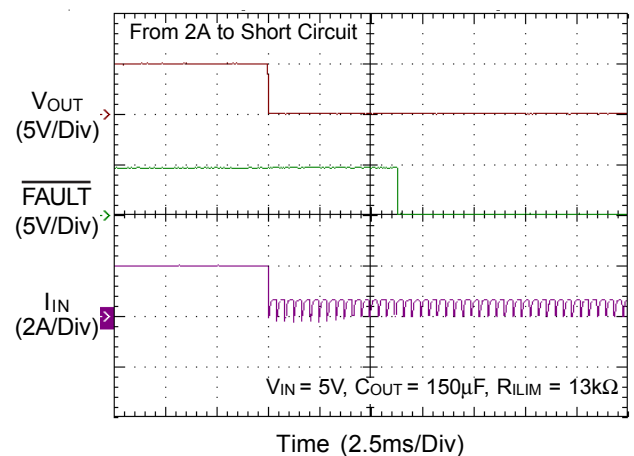
Power Off from EN



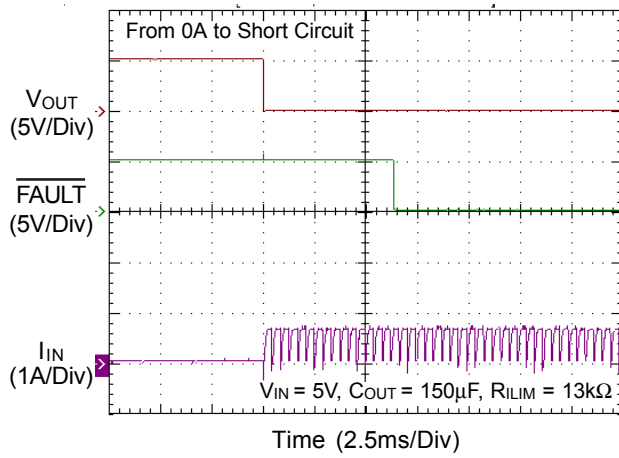
Short Circuit Protection



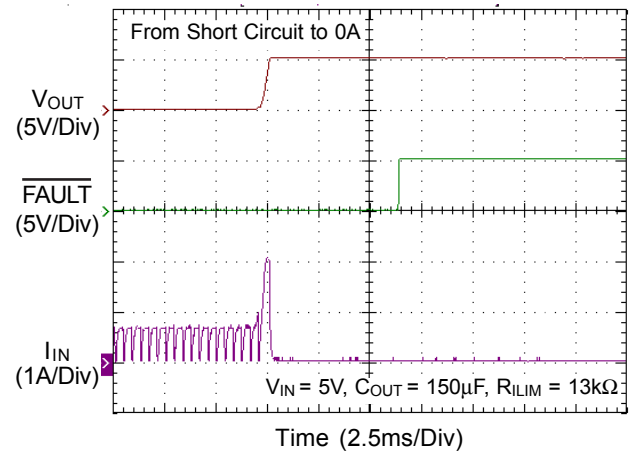
Short Circuit Protection



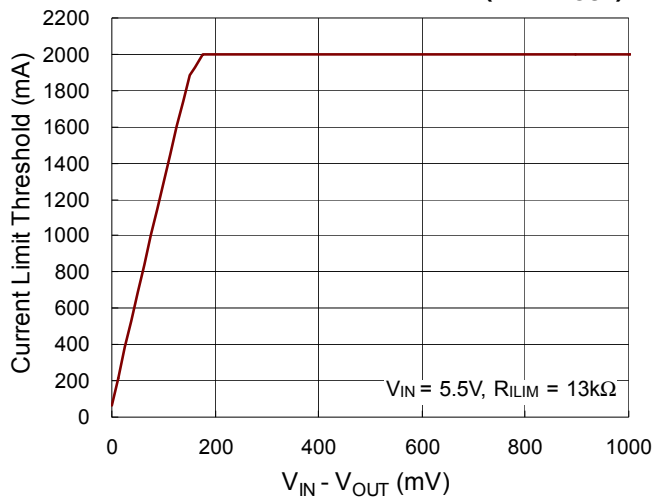
Short Circuit Protection



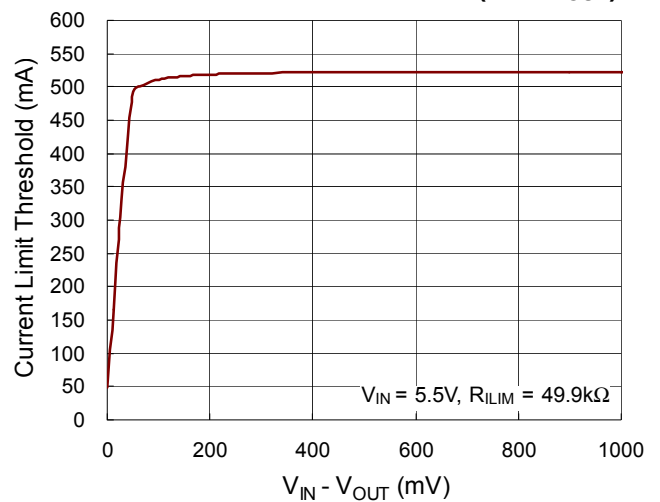
Short Circuit Protection



Current Limit Threshold vs. ($V_{IN} - V_{OUT}$)



Current Limit Threshold vs. ($V_{IN} - V_{OUT}$)



Application Information

The RT2528A is a single P-MOSFET high-side power switch with active high enable input, optimized for self powered and bus powered Universal Serial Bus (USB) applications. The switch's low $R_{DS(ON)}$ meets USB voltage drop requirements and a flag output is available to indicate fault conditions to the local USB controller.

Current Limiting and Short Circuit Protection

When a heavy load or short circuit situation occurs while the switch is enabled, large transient current may flow through the device. The RT2528A includes a current limit circuitry to prevent these large currents from damaging the MOSFET switch and the hub downstream ports. The RT2528A provides an adjustable current limit threshold between 0.5A and 2.5A (typ.) via an external resistor, R_{ILIM} , between 10k Ω and 49.9k Ω . The maximum –100mA fault flag assertion offset needs cautions, especially for low ILIM applications. Once the current limit threshold is exceeded and output voltage doesn't drop over 1/2 input voltage, the device enters constant current mode.

If output voltage drops under around 1/2 input voltage, the device enters re-soft start current fold-back mode until either thermal shutdown occurs or the fault is removed. The Table1 shows a recommended current limit value vs. R_{ILIM} resistor.

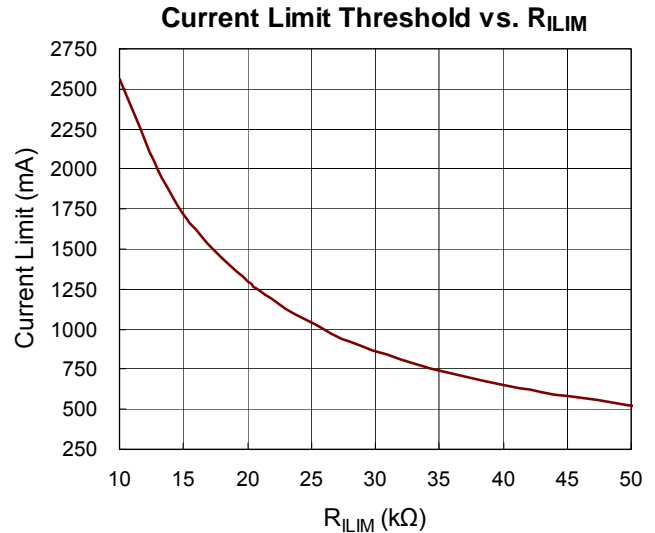


Figure 1. Current Limit Threshold vs. R_{ILIM}

Table 1. Recommended R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)	Ideal Resistor (k Ω)	Closest 1% Resistor (k Ω)	Actual Limits (Include R Tolerance)		
			IOS min (mA)	IOS nom (mA)	IOS max (mA)
500	52.5	52.3	443.9	501.6	562.4
600	43.5	43.2	535.1	604.6	674.1
700	37.2	37.4	616.0	696.0	776.0
800	32.4	32.4	708.7	800.8	892.9
900	28.7	28.7	797.8	901.5	1005.2
1000	25.8	26.1	875.4	989.1	1102.8
1100	23.4	23.2	982.1	1109.7	1237.3
1200	21.4	21.5	1057.9	1195.4	1332.9
1300	19.7	19.6	1158.0	1308.5	1459.0
1400	18.5	18.7	1225.7	1385.0	1544.3
1500	17.3	17.4	1317.3	1488.5	1659.7
1600	16.2	16.2	1414.8	1598.7	1782.6
1700	15.2	15.0	1528.1	1726.7	1925.3
1800	14.4	14.3	1602.9	1811.2	2019.5
1900	13.6	13.7	1673.1	1890.5	2107.9
2000	12.9	13.0	1763.2	1992.3	2221.4
2100	12.3	12.4	1848.5	2088.7	2328.9
2200	11.8	11.8	1942.6	2195.0	2447.4
2300	11.3	11.3	2028.4	2292.0	2555.6
2400	10.8	10.7	2141.7	2420.0	2698.3
2500	10.3	10.0	2292.2	2590.0	2887.9

Fault Flag

The RT2528A provides a $\overline{\text{FAULT}}$ signal pin which is an N-Channel open drain MOSFET output. This open drain output goes low when current exceeds current limit threshold. The $\overline{\text{FAULT}}$ output is capable of sinking a 1mA load to typically 180mV above ground. The $\overline{\text{FAULT}}$ pin requires a pull-up resistor; this resistor should be large in value to reduce energy drain. A 100k Ω pull-up resistor works well for most applications. In case of an over-current condition, $\overline{\text{FAULT}}$ will be asserted only after the flag response delay time, t_D , has elapsed. This ensures that $\overline{\text{FAULT}}$ is asserted upon valid over-current conditions and that erroneous error reporting is eliminated. For example, false over-current conditions may occur during hot-plug events when extremely large capacitive loads are connected, which induces a high transient inrush current that exceeds the current limit threshold. The $\overline{\text{FAULT}}$ response delay time, t_D , is typically 7.5ms.

Supply Filter/Bypass Capacitor

A 10 μ F low-ESR ceramic capacitor connected from VIN to GND and located close to the device is strongly recommended to prevent input voltage drooping during hot plug events. However, higher capacitor values may be used to further reduce the voltage droop on the input. Without this bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. Note that the input transient voltage must never exceed 6V as stated in the Absolute Maximum Ratings.

Output Filter Capacitor

Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused by hot-insertion transients in downstream cables. Ferrite beads in series with VBUS, the ground line and the bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies.

For commercial applications where the ambient temperature is 0°C to 70°C (such as a PC or USB hub), RT2528A supports an output capacitor range of up to

120 μ F. For industrial applications with an ambient temperature of -40°C to 125°C, please limit the output capacitance to less than 50 μ F to ensure normal startup.

Chip Enable Input

The RT2528A doesn't have auto discharge function. During shutdown condition, the supply current is 1 μ A typical. The maximum guaranteed voltage for a logic-low at the EN pin is 0.4V. A minimum guaranteed voltage of 1.2V at the EN pin will turn on the RT2528A. Floating the input may cause unpredictable operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 2.2V. If input voltage drops below approximately 2V, UVLO turns off the MOSFET switch.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(\text{MAX})}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(\text{MAX})} = (T_{J(\text{MAX})} - T_A) / \theta_{JA}$$

where $T_{J(\text{MAX})}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA} , is 49°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.041\text{W for a SOP-8 (Exposed Pad) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

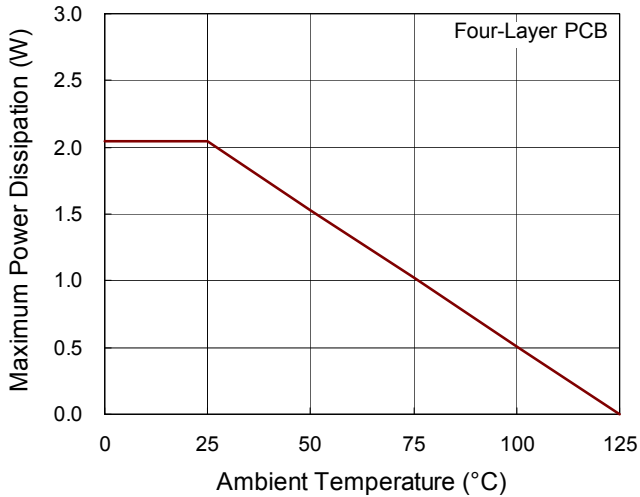
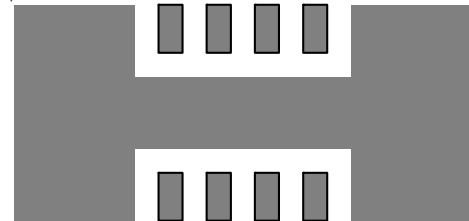


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Consideration

- ▶ Ounce copper on top layer will improve thermal performance. 4-layer PCB will be better.
- ▶ Place the shape with minimum 70mm² as Figure 3 around the SOP-8 (Exposed Pad) footprint to achieve best thermal performance.



Copper Area = 70mm², $\theta_{JA} = 49^{\circ}\text{C/W}$

Figure 3. PCB Copper Area

- ▶ Utilize standard PTH (Plated Through Hole, 25mil diameter, as Figure 4) to via down from exposed pad on top layer to GND plane on other layers.

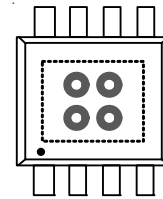
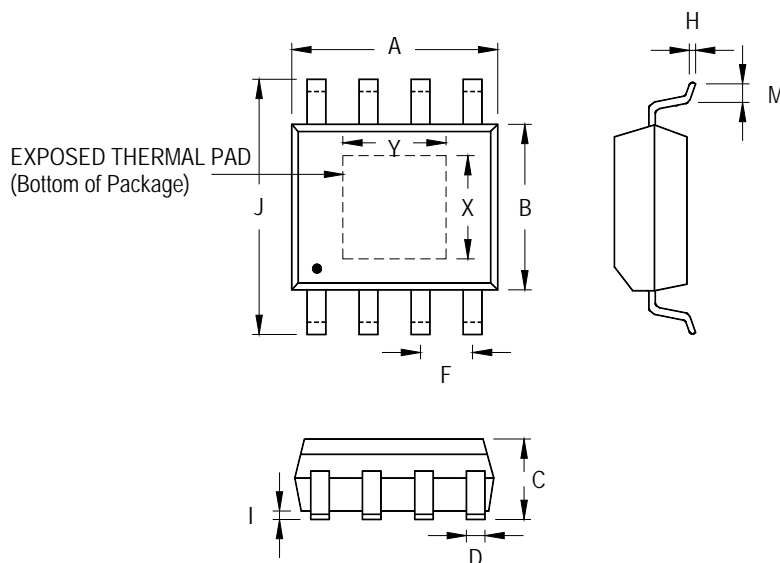


Figure 4. Standard PTH to GND Plane

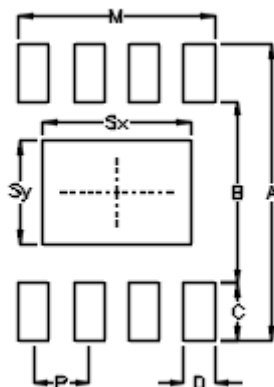
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)							Tolerance	
			P	A	B	C	D	Sx	Sy		M
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

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