60V, 300W Hybrid Step-Down µModule Bus Converter

FEATURES

- **Input Voltage Range: 30V to 60V (65V Abs. Max.)**
- **Wide Output Voltage: 4.5V to 18V ($V_{OUT} < V_{IN}/2$)**
- **97.3% Peak Efficiency ($12V_{OUT}$ at 15A, $48V_{IN}$)**
- **±1.5% Maximum Total DC Output Error**
- **Up to 300W Output Power**
- **Scalable: Parallel LTM4660s for Higher Power**
- Fixed Frequency Current Mode Control
- Phase-Lockable External Synchronization from 200kHz to 1MHz
- Low Start-Up Inrush Current with Flying Capacitor Voltage-Balancing Prior to DC/DC Switching Action
- Output Voltage Tracking with Soft-Start
- Short-Circuit Protection with Adjustable Retry-Timer
- Overcurrent and Overtemperature Protection
- Onboard Diode Temperature Monitor
- Optional External Reference Input
- Power Good and $\overline{FAULT}$ Indicators
- 16mm × 16mm × 10.34mm BGA Package

APPLICATIONS

- Telecom, Data Centers and Networking Equipment
- Industrial and Test Equipment

DESCRIPTION

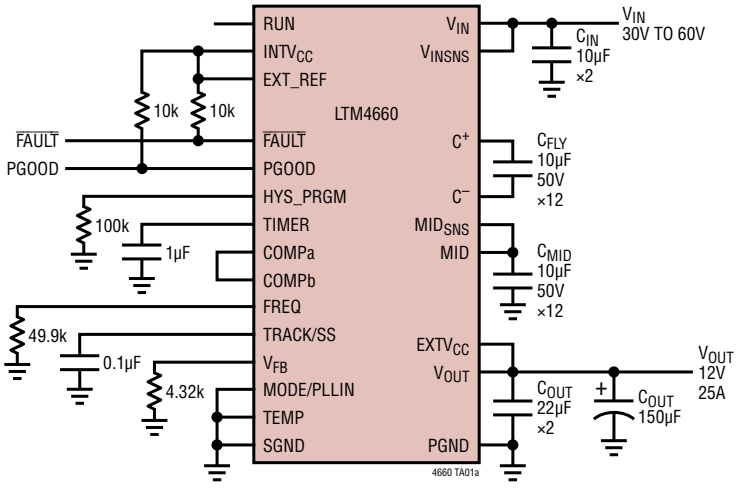
The LTM®4660 is a complete 300W output switching mode hybrid-topology step-down DC/DC µModule® (micromodule) nonisolated bus converter. Its exposed power inductor resides on the top of the package, providing an intrinsic path for heat to dissipate up and out of the module—away from one's printed circuit board. Included in the package are the switching controller IC, power MOSFETs and supporting components. Only flying (charge-pump) capacitors, bulk input and output bypass capacitors, and a few configuration passives are needed.

The LTM4660 features frequency synchronization, Burst Mode® operation and output voltage soft-start and tracking. An onboard temperature diode is available for temperature monitoring. The LTM4660 protects against short-circuit, overcurrent, and overtemperature faults. For higher power applications, multiple LTM4660 modules can be easily paralleled.

The LTM4660 is offered in a 16mm × 16mm × 10.34mm BGA package with RoHS compliant terminal finish.

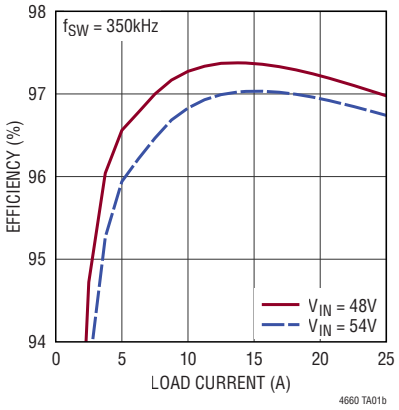
TYPICAL APPLICATION

12V, 25A DC/DC µModule Nonisolated Bus Converter



PINS NOT USED IN THIS CIRCUIT: CLKOUT, TEMP+, TEMP–

Efficiency vs Load Current
V_{OUT} = 12V



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages

V_{IN}, V_{INSNS} ..... –0.3V to 65V

V_{OUT}, $EXTV_{CC}$, PGOOD, $\overline{FAULT}$ ..... –0.3V to 20V

MID, MID_{SNS} ..... –0.3V to 32.5V

RUN, FREQ, HYS_PRGM, TEMP, V_{FB}, TRACK/SS, TIMER, MODE/PLLIN, EXT_REF ..... –0.3V to $INTV_{CC}$

Terminal Currents

$TEMP^+$ ..... –1mA to 1mA

$TEMP^-$ ..... –1mA to 1mA

Temperatures

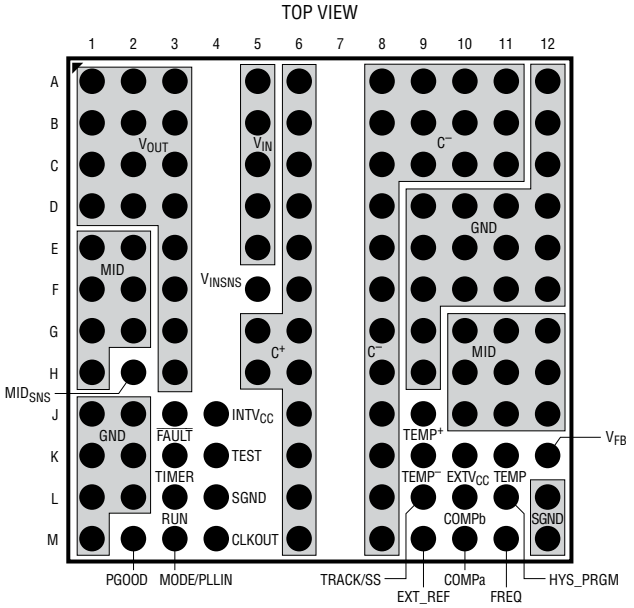
Internal Operating Temperature Range (Note 2) ..... –40°C to 125°C

Storage Temperature Range ..... –55°C to 125°C

Peak Package Body Temperature During Reflow ..... 245°C

(All Voltages Relative to GND Unless Otherwise Indicated)

PIN CONFIGURATION



BGA PACKAGE

120-LEAD (16mm × 16mm × 10.34mm)

T_{JMAX} = 125°C, θ_{JCtop} = 3.92°C/W, $\theta_{JCbottom}$ = 1.98°C/W, θ_{JA} = 7.3°C/W

θ VALUES DETERMINED PER JESD51-12 (SEE NOTE 9), WEIGHT = 9.3g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4660EY#PBF	SAC305 (RoHS)	LTM4660Y	e1	BGA	4	–40°C to 125°C
LTM4660IY#PBF						

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INSNS} = 54V, V_{OUT} = 12V and $EXTV_{CC}$ = 12V (see Note 4). Configured per Block Diagram circuit with no output load unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	30		60	V
$V_{OUT(RANGE)}$	Output Voltage, Supported Range of Regulation	V_{IN} = 54V	●	4.5		18	V
$V_{OUT(DC)}$	Output Voltage Variation	V_{OUT} = 12V, I_{OUT} = 15A (Notes 3, 5)	●	11.8	12	12.2	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	V_{IN} Rising Hysteresis	●		8.8 0.38	9.4	V V
$I_{S(VIN, FCM)}$	Input Supply Power Current, in Forced Continuous Mode	MODE/PLLIN = 0V, I_{OUT} = 0A (Note 6) MODE/PLLIN = 0V, I_{OUT} = 0.5A			38 150		mA mA
$I_{S(VIN, PS)}$	Input Supply Power Current, in Pulse-Skipping Mode	MODE/PLLIN = $INTV_{CC}$, I_{OUT} = 0.5A			135		mA
$I_{S(VIN, BM)}$	Input Supply Power Current, in Burst Mode	MODE/PLLIN = Open Circuit, I_{OUT} = 0.5A			120		mA
$I_{S(VIN, SHUTDOWN)}$	Input Supply Power Current in Shutdown	Shutdown, V_{RUN} = 0V			300		µA
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	(Note 3)		0		25	A
$\Delta V_{OUT}/V_{OUT}$	Line Regulation Accuracy	30 ≤ V_{IN} ≤ 60V, I_{OUT} = 0A			0.003	0.2	%/V
	Load Regulation Accuracy	I_{OUT} =15A 30 ≤V_{IN} ≤ 60V, 0A ≤ I_{OUT} ≤ 25A (Note 7)	●		 0.5	1.5	% %
$\Delta V_{OUT(AC)}$	Output Voltage Ripple				150		mV_{P-P}
f_s	V_{OUT} Ripple Frequency	R_{FREQ} = 61.9kΩ, I_{OUT} = 0A			450		kHz
$t_{Start-Up}$	Turn-On Start-Up Time	Capacitor Balancing – Delay Measured from Toggling RUN on to MID Reaching V_{IN}/2, C_{TIMER} = 1.47µF, C_{MID} and C_{FLY} = 10µF ×12 Delay Measured from MID Reaching V_{IN}/2 to PGOOD Exceeding 3V, $C_{TRACK/SS}$ = 0.1µF			300 5		ms ms
$\Delta V_{OUT(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0W to 150W in 1µs and 150W to 0W in 1µs C_{OUT} =150µF ×2, 10µF ×3 (Note 7)			0.3		V
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0W to 150W in 1µs and 150W to 0W in 1µs C_{OUT} =150µF ×2, 10µF ×3 (Note 7)			300		µs
Control Section							
V_{VFB}	Regulated V_{FB} Pin Feedback Voltage	I_{OUT} = 0A, V_{OUT} = 12V	●	0.792	0.8	0.808	V
I_{VFB}	V_{FB} Pin Leakage Current	(Note 8)			±10		nA
$I_{TRACK/SS}$	Soft-Start Charge Current	$V_{TRACK/SS}$ = 0V		–9	–10	–11	µA
Monitors							
I_{VINSNS}	V_{INSNS} Bias Current	V_{RUN} = 5V, Normal Mode V_{RUN} = 0V, Shutdown			1 45		mA µA
RUN Enable Pins							
V_{RUN}	RUN Turn-On Threshold	V_{RUN} Rising	●	1.1	1.3	1.6	V
$V_{RUN, HYS}$	RUN Hysteresis				100		mV
I_{RUN}	RUN Pull-Up Current	V_{RUN} = 0V			1		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INSNS} = 54V, V_{OUT} = 12V and $EXTV_{CC}$ = 12V (see Note 4). Configured per Block Diagram circuit with no output load unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Capacitor Voltage-Balancing							
V_{TIMER_LOW}	Voltage at TIMER Pin to Start Capacitor Balancing				0.5		V
V_{TIMER_HIGH}	Voltage at TIMER Pin to Stop Capacitor Balancing				1.25		V
I_{TIMER}	TIMER Pin Charge Current	V_{TIMER} = 0.9V V_{TIMER} = 2.8V	●	–6 –3	–7 –3.5	–8 –4	µA µA
V_{HYS_PRGM}	Capacitor Balancing Window Comparator Threshold	V_{HYS_PRGM} = 0V V_{HYS_PRGM} = 1.2V V_{HYS_PRGM} = $INTV_{CC}$			±0.3 ±1.2 ±0.8		V V V
I_{HYS_PRGM}	HYS_PRGM Pin Current	V_{HYS_PRGM} = 0V	●	–9	–10	–11	µA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Pin Voltage Low	$I_{\overline{FAULT}}$ = 0.6mA			0.2	0.4	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 20V				1	µA
$I_{C^+(SOURCE)}$	Current Out of C^+ During Capacitor Balancing	V_{C^+} to V_{C^-} < V_{IN}/2, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			40		mA
$I_{C^+(SINK)}$	Current Into C^+ During Capacitor Balancing	V_{C^+} to V_{C^-} > V_{IN}/2, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			6		mA
$I_{C^-(SINK)}$	Current Into C^- During Capacitor Balancing	V_{C^+} to V_{C^-} < V_{IN}/2, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			40		mA
$I_{C^-(SOURCE)}$	Current Out of C^- During Capacitor Balancing	V_{C^+} to V_{C^-} > V_{IN}/2, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			6		mA
$I_{MID(SOURCE)}$	Current Out of MID During Capacitor Balancing	V_{MID} < V_{IN}/2, V_{MID} = V_{MID_SNS} = 23V, V_{C^+} to V_{C^-} ≥ 27V, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			60		mA
$I_{MID(SINK)}$	Current Into MID During Capacitor Balancing	V_{MID} > V_{IN}/2, V_{MID} = V_{MID_SNS} = 31V, V_{C^+} to V_{C^-} ≥ 27V, V_{C^-} = 12V, V_{IN} = 48V (Note 8)			40		mA
Oscillator and Timer Circuits							
$f_{SYNC(RANGE)}$	External Frequency Synchronization Range			200		1000	kHz
f_{SW}	Nominal Switching Frequency	R_{FREQ} = 61.9kΩ			450		kHz
I_{FREQ}	FREQ Setting Current	V_{FREQ} = 0V (Note 8)		–9.5	–10	–10.5	µA
Power Good							
R_{PGOOD}	PGOOD Pull-Down Resistance	I_{PGOOD} = 0.6mA			650		Ω
I_{PGOOD_LEAK}	PGOOD Leakage Current	V_{PGOOD} = 20V				±1	µA
$INTV_{CC}$ Regulator and $EXTV_{CC}$ Circuits							
V_{INTVCC_INT}	$INTV_{CC}$ Voltage No Load	10V ≤ V_{IN} ≤ 60V, V_{EXTVCC} = 0V	●	5.65		5.95	V
	$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0 to 50mA, V_{EXTVCC} = 0V			0.8	±2	%
V_{INTVCC_EXT}	$INTV_{CC}$ Voltage No Load with $EXTV_{CC}$ Bias	12V < V_{EXTVCC} < 18V		5.65	5.8	5.95	V
	$INTV_{CC}$ Load Regulation with $EXTV_{CC}$ Bias	I_{INTVCC} = 0 to 50mA, V_{EXTVCC} = 12V			0.5	±2	%
	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive			7		V
	$EXTV_{CC}$ Hysteresis				200		mV
Temperature Sensor							
ΔV_{TEMP}	Temperature Sensor Forward Voltage, V_{TEMP^+} to V_{TEMP^-}	I_{TEMP^+} = 100µA and I_{TEMP^-} = –100 µA at T_A = 25°C			0.6		V
$TC_{\Delta V(TEMP)}$	ΔV_{TEMP} Temperature Coefficient				–2.0		mV/°C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4660 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4660E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4660I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 4: To reduce internal module temperature rise, it is recommended to bias $EXTV_{CC}$. For applications where $V_{OUT} > 8V$, tie V_{OUT} to $EXTV_{CC}$. For applications where $V_{OUT} < 8V$, it is strongly recommended to drive $EXTV_{CC}$ with an auxiliary supply.

Note 5: Total DC output voltage error includes all errors over temperature: line and load regulation as well as the tolerance of the 60.4kΩ feedback resistor internally connecting V_{OUT} to V_{FB}.

Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency in forced continuous mode operation. See Applications Information.

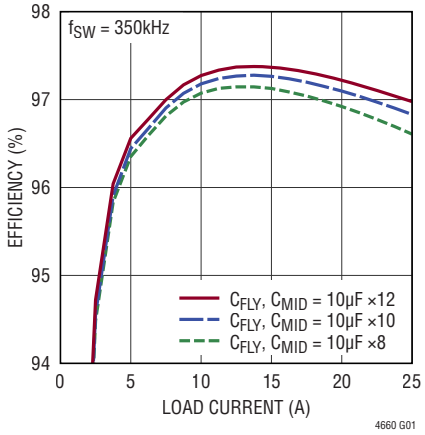
Note 7: Guaranteed by design. Validated from bench measurements.

Note 8: ATE-tested at wafer sort only.

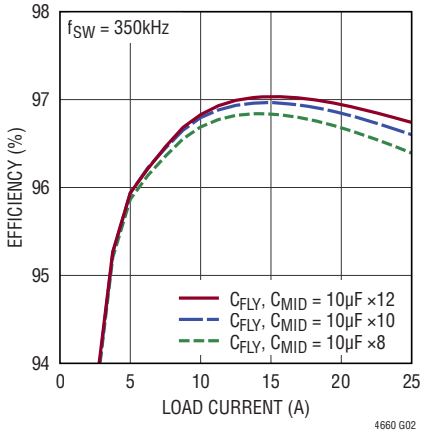
Note 9: θ_{JA} value obtained from demo board DC2879A. Refer to Thermal Considerations in Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

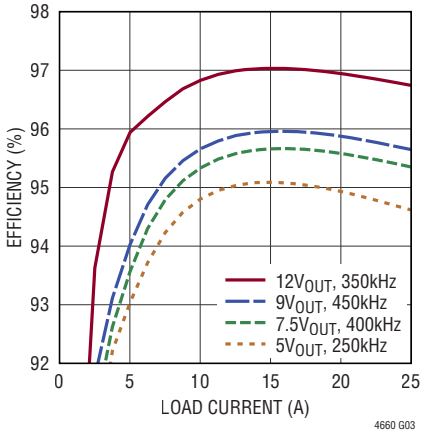
Efficiency vs Output Current
V_{IN} = 48V, V_{OUT} = 12V



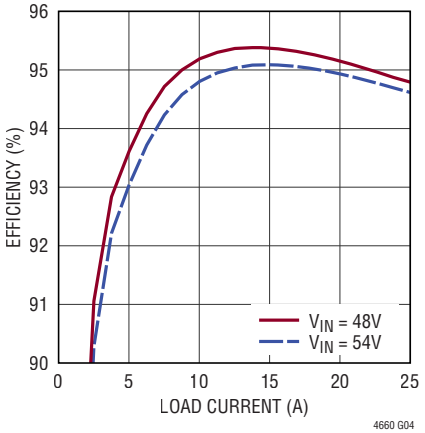
Efficiency vs Output Current
V_{IN} = 54V, V_{OUT} = 12V



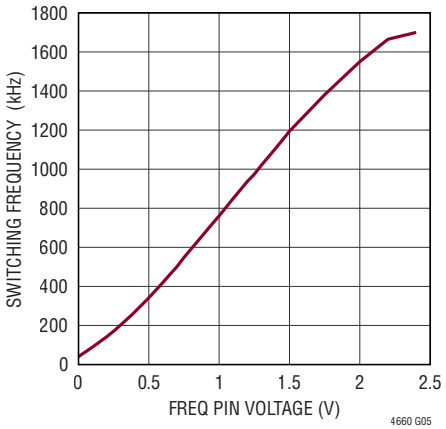
Efficiency for
$54V_{IN}$, C_{MID} = C_{FLY} = 10µF ×12



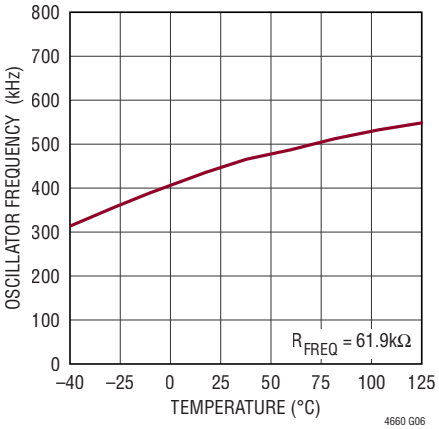
Efficiency for
V_{OUT} = 5V, f_{SW} = 250kHz



Switching Frequency
vs FREQ

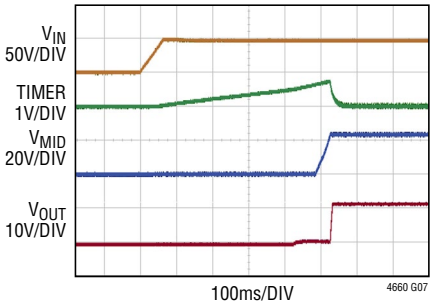


Oscillator Frequency
vs Temperature

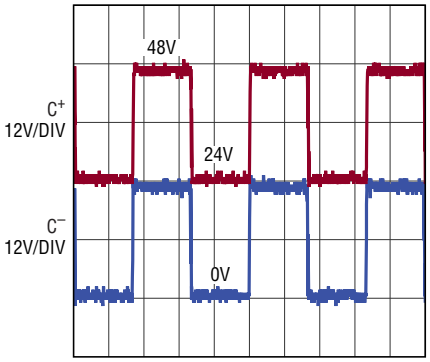


TYPICAL PERFORMANCE CHARACTERISTICS

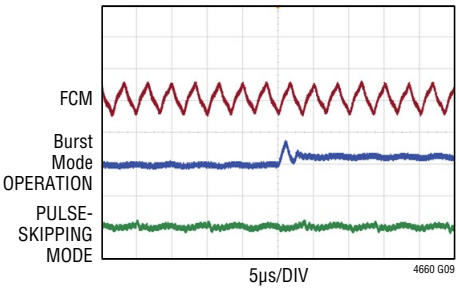
Start-Up Characteristics



Steady State Waveforms
V_{IN} = 48V, V_{OUT} = 12V, FCM

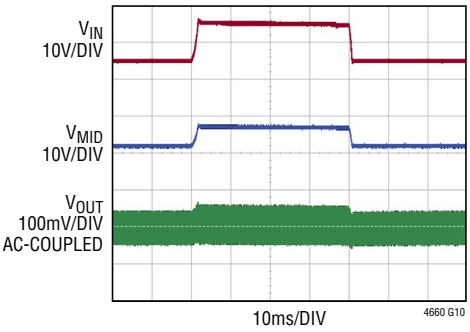


V_{OUT} Ripple



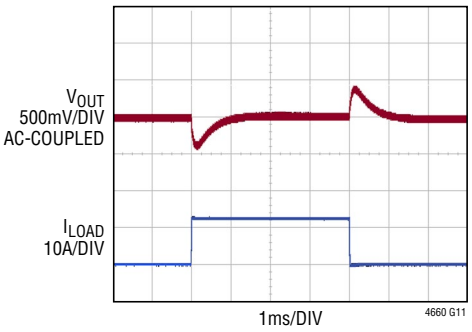
V_{IN} = 48V
V_{OUT} = 12V
C_{OUT} = 150µF ×2 + 10µF ×3
COMPa TIED TO COMPb

Line Transient
V_{IN} Slew Rate 10V/ms



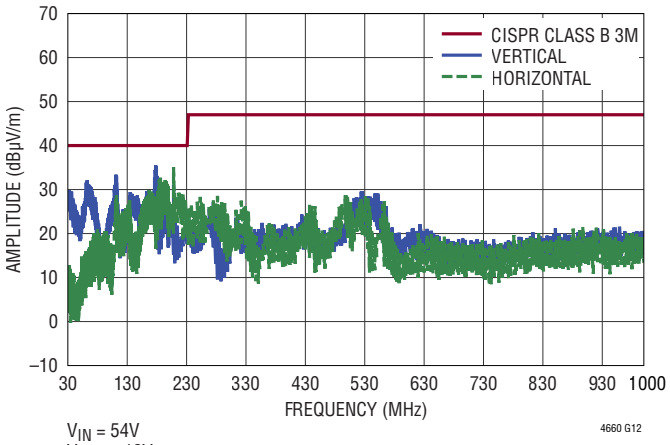
V_{OUT} = 12V
P_{OUT} = 300W
C_{MID} AND C_{FLY} = 10µF ×12

Load Transient
12.5A to 25A to 12.5A



V_{IN} = 48V
V_{OUT} = 12V
C_{OUT} = 150µF ×2 + 10µF ×3
COMPa TIED TO COMPb

Radiated EMI Performance (CISPR22 Radiated Emission Test with Class B 3m Limits)



V_{IN} = 54V
V_{OUT} = 12V
P_{OUT} = 300W, f_{SW} = 350kHz
DC2879A, MEASURED IN A 3m CHAMBER, PEAK DETECT METHOD

PIN FUNCTIONS

V_{OUT} (A1-3, B1-3, C1-3, D1-3, E3, F3, G3, H3): Output Voltage. Bypass to ground with capacitors appropriate for the application. See Decoupling Requirements.

V_{IN} (A5, B5, C5, D5, E5): Main Input Supply. Bypass this pin to GND with at least 2 × 4.7µF X7R- or X7S-type capacitors with appropriate voltage rating.

C^+ (A6, B6, C6, D6, E6, F6, G5-6, H5-6, J6, K6, L6, M6): Switch Node Connection to One Terminal of Flying Capacitor. Voltage at this pin swings between $V_{IN}/2$ and V_{IN}.

C^- (A8-11, B8-11, C8-11, D8, E8, F8, G8, H8, J8, K8, L8, M8): Switch Node Connection to Internal Power Inductor and One Terminal of Flying Capacitor. Voltage at this pin swings between ground and $V_{IN}/2$.

GND (A12, B12, C12, D9-D12, E9-12, F9-12, G9, H9, J1-2, K1-2, L1-2, M1): Power Ground. Connect all module GND pins to the application's power ground plane.

MID (E1-2, F1-2, G1-2, G10-12, H1, H10-12, J10-12): Half Supply from V_{IN}. Do not use this to source current. Connect MLCC bypass capacitors from this node to GND. A minimum of 8 × 10µF X7R or X7S MLCC capacitors is recommended. Higher efficiency can be achieved with 12 × 10µF X7R or X7S MLCC capacitors. All MID pins are internally connected within the module, but in order for the LTM4660 to achieve the best possible efficiency, it is necessary to connect all MID pins together with large copper plane(s) external to the module. See the Applications Information section.

V_{INSNS} (F5): V_{IN} Kelvin Sensing Input. Used to accurately sense input voltage. Connect to V_{IN}, under the module.

MID_{SNS} (H2): MID Kelvin Sensing Input. Used to accurately sense MID voltage. Connect to MID under the module.

$\overline{FAULT}$ (J3): Open Drain Output pin. When the signal goes low, it indicates one of the following conditions:

a. In the capacitor balancing phase, capacitors C_{FLY} or C_{MID} (see Typical Applications) are not charged to $V_{IN}/2$. A low $\overline{FAULT}$ indicates an abnormal condition that is preventing C_{FLY} or C_{MID} from being be charged up to $V_{IN}/2$.

b. During normal operation, the voltage deviates from $V_{IN}/2$ by a window amount set by the voltage on the HYS_PRGM pin.

c. The die temperature exceeds its internally set limit or the PTC resistor connected as the lower leg of a resistor divider (if used) trips the TEMP pin threshold.

During any of the aforementioned conditions, the TRACK/SS pin will also be pulled low.

$INTV_{CC}$ (J4): Internal Regulator Output. Powers control circuits and gate drivers internal to the module. Leave this pin floating.

$TEMP^+$ (J9): Temperature Sensor, Positive Input. Emitter of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC®2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open.

$TEMP^-$ (K9): Temperature Sensor, Negative Input. Collector-base of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open.

TIMER (K3): Charge Balancing Timer Input. A capacitor connected from this pin to SGND sets the amount of time allocated to charge C_{FLY} and C_{MID} to $V_{IN}/2$ during the capacitor balancing phase. It also sets the auto-retry timeout, should the capacitors fail to reach this voltage within the set time. Capacitors C_{FLY} and C_{MID} begin and end charging when the TIMER voltage is between 0.5V and 1.2V, respectively. If the capacitor is balanced before the TIMER voltage reaches 1.2V, this voltage is reset to ground and normal operation begins. However, if the balance is not reached when the voltage reaches 1.2V, then the charging of the capacitors stops and the auto-retry timeout period begins. The TIMER capacitor will now slew at half the rate until it reaches 4V and then resets to zero and begins to slew at 1× rate. Once it reaches 0.5V, the C_{FLY} and C_{MID} begin to charge again and the process repeats.

TEST (K4): Test Pin. Used in ATE test, only. Leave open circuit.

PIN FUNCTIONS

$EXTV_{CC}$ (K10): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 8V. Do not float or exceed 20V on this pin. Connect $EXTV_{CC}$ to GND, if the features is unused.

To reduce internal module temperature rise, it is strongly recommended to bias $EXTV_{CC}$ with $8V_{DC}$ or higher. For applications where $V_{OUT} \geq 8V$, there is an easy way: connect V_{OUT} to $EXTV_{CC}$. For applications where $V_{OUT} < 8V$, it is strongly recommended to drive $EXTV_{CC}$ to 8V (or higher) with an external bias supply. When driving $EXTV_{CC}$ externally, take precautions to ensure $EXTV_{CC} \leq V_{IN}$ at all times.

TEMP (K11): Temperature Sensing Input. Using a PTC resistor as the lower leg of a resistor divider, connect the TEMP pin to the common point of the divider. The PTC resistor is used to monitor a hot spot on the PCB. Once it reaches the TEMP threshold of 1.22V, the LTM4660 stops switching for 100ms before retrying. Ground this pin if not used.

V_{FB} (K12): Error Amplifier Feedback Input. Connect resistor R_{VFB} from this pin to SGND in order to configure the V_{OUT} output voltage setting. R_{VFB} is given by Equation 1.

$$R_{VFB}\ (k\Omega) = \frac{60.4}{\left(\frac{V_{OUT}}{V_{VFB}} - 1\right)} \quad (1)$$

When EXT_REF is connected to $INTV_{CC}$, the module regulates the V_{FB} pin at 0.8V, nominal. If EXT_REF is used or TRACK/SS is externally driven to influence the V_{FB} target servo voltage, the value of R_{VFB} must be computed accordingly. (See the Applications Information section.)

RUN (L3): Run Control Input. A voltage above 1.3V turns the LTM4660 ON. A voltage below 1.1V causes the module to shutdown. There is a 1µA pull-up current on this pin when its voltage is below 1.3V.

SGND (L4, L12, M12): Signal Ground. All small-signal components and compensation components (if used) should connect to this signal SGND, which connects to GND internal to the module. It is not necessary to connect SGND to GND externally.

TRACK/SS (L9): Output Voltage Tracking and Soft-Start Input. The LTM4660 regulates the V_{FB} voltage to the lowest of three voltages: 0.8V, the voltage on the EXT_REF pin or the voltage on the TRACK/SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to SGND at this pin sets the ramp time to the final regulated output voltage. Alternatively, a resistor divider from another voltage supply connected to this pin allows the LTM4660 output voltage to track the other supply during start-up.

HYS_PRGM (L11): There is a 10µA current flowing out of this pin. A voltage created by connecting a resistor from this pin to SGND sets an equal amount of window threshold around $V_{IN}/2$ to a window comparator. When the voltage at MID_{SNS} is not within this window threshold, $\overline{FAULT}$ will be pulled low and switching will stop. C_{FLY} and C_{MID} will be rebalanced to half of V_{IN} before resuming normal operation.

PGOOD (M2): Power Good Pin. This is an open drain output. PGOOD is pulled to ground when voltage at V_{FB} pin falls below 7.5% or rises above 8.5% of its set point. It will also be pulled low when $\overline{FAULT}$ is tripped.

MODE/PLLIN (M3): Mode Selection or External Synchronization Input to Phase Detector. When external synchronization is not used, this pin selects the operating modes and can be tied to SGND, to $INTV_{CC}$ or left open circuit. If the pin is connected to SGND, it enables forced continuous mode while a connection to $INTV_{CC}$ enables pulse-skipping mode. Floating the pin enables Burst Mode operation. For external sync, apply a clock signal to this pin. The integrated PLL along with its internal compensation network will synchronize the internal oscillator to external clock. Forced continuous mode will be enabled when an external clock is applied.

CLKOUT (M4): Clock Output Pin. This pin outputs a clock 180° out of phase with the main operating clock of the LTM4660.

EXT_REF (M9): External Reference Input. A voltage applied to this pin forces the V_{FB} to regulate to this voltage. Internal clamps set at 0.45V and 0.9V limit the lower and upper bounds of V_{FB} regulation that EXT_REF can

PIN FUNCTIONS

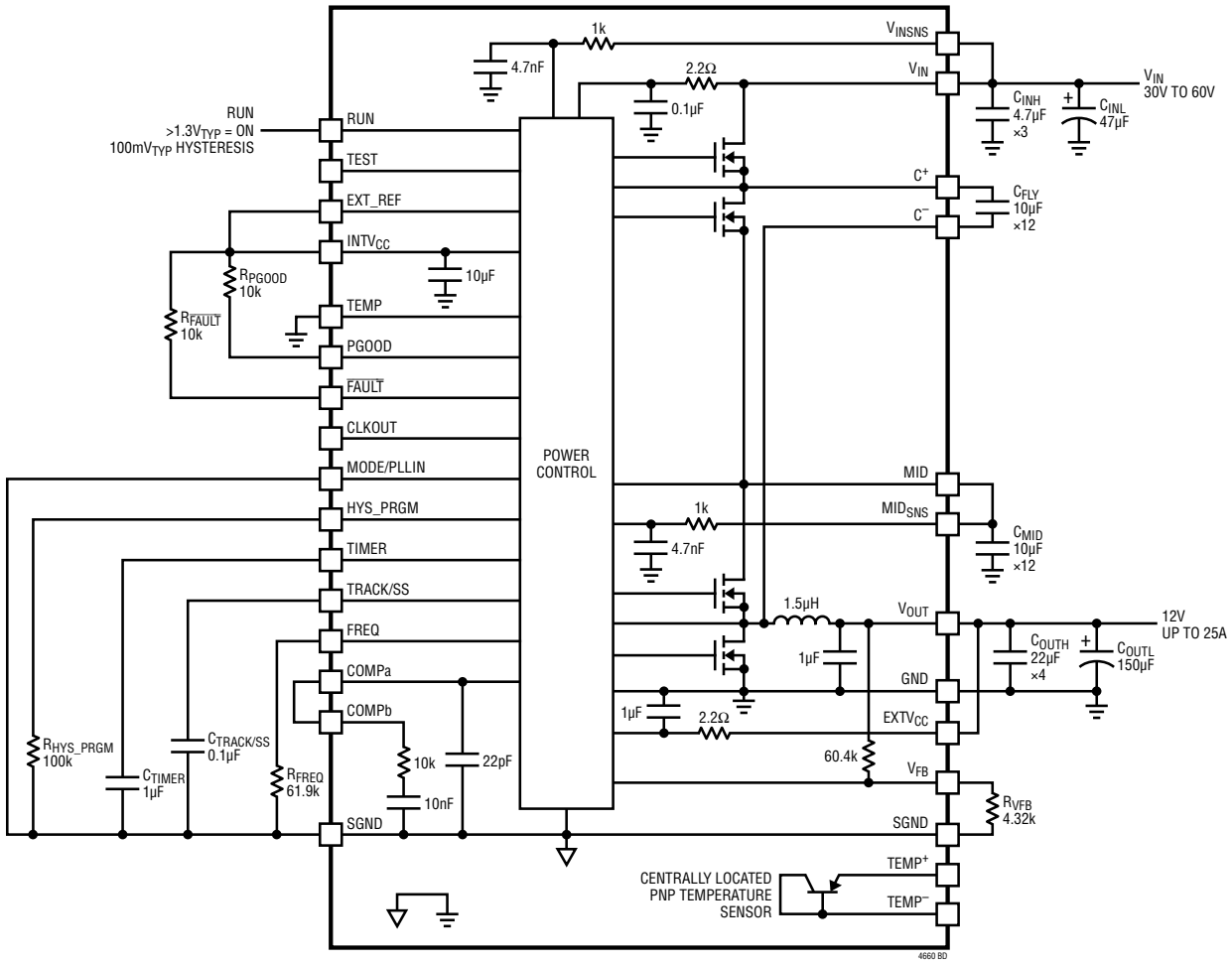
command. Connecting this pin to $INTV_{CC}$ will cause the internal reference to be used for output voltage regulation.

COMPb (L10): Default Loop Compensation Network. Connect COMPa to COMPb for default loop compensation—or otherwise, leave open circuit.

COMPa (M10): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with its COMPa control voltage. Connect COMPa to COMPb for default loop compensation—or alternatively, connect a series R-C network from COMPa to SGND, to apply application-specific loop compensation.

FREQ (M11): Frequency Set Pin. There is a 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the switching frequency of the module.

BLOCK DIAGRAM



DECOUPLING REQUIREMENTS

T_A = 25°C. Refer to Block Diagram.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{FLY}	External Flying Capacitor Requirement, 30V ≤ V_{IN} ≤ 60V, V_{OUT} = 12V	P_{OUT} = 300W (Note 3)	80	100	120	µF
C_{MID}	External Midpoint Capacitor Requirement, 30V ≤ V_{IN} ≤ 60V, V_{OUT} = 12V	P_{OUT} = 300W (Note 3)	80	100	120	µF
C_{OUT}	External Output Capacitor Requirement, 30V ≤ V_{IN} ≤ 60V, V_{OUT} = 12V	P_{OUT} = 300W		100		µF

OPERATION

Module Description

LTM4660 is a high efficient Intermediate Bus Converter (IBC) utilizing a hybrid switched capacitor topology. Four power switches along with capacitor bank C_{FLY} and C_{MID} form a switched capacitor stage, dividing the input voltage by two at MID. Voltage at MID is further stepped down through a power inductor and output capacitor, similar to a step down switching converter. LTM4660 employs peak current mode control of the inductor current for pulse width modulation of the switches and to maintain accurate output regulation. Soft switching of the power switches results in excellent efficiency and EMI performance.

Current mode control enables fast cycle-by-cycle current limiting of the inductor current and hence protects the internal components of LTM4660 during short-circuit conditions. With current mode control, LTM4660 exhibits good transient performance and stability margins for wide range of output capacitors. An internal compensation network included inside LTM4660 is sufficient for most typical applications. The V_{FB} pin is used to program the output voltage with a single resistor to ground.

Switching frequency can be programmed by a single resistor connected between FREQ pin and SGND. Typical switching frequency for IBC applications with LTM4660 is 300kHz to 500kHz. A phase-locked loop inside the module enables synchronizing the switching frequency to an external clock.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state by turning off all switching and internal circuits. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. Internal bandgap reference of 0.8V can be overridden by applying a suitable voltage at EXT_REF pin. See the Applications Information section.

A general purpose temperature diode is included to monitor internal temperature of the module. In addition, TEMP pin of the module is used to program the OTP trip point. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits the regulation window.

Capacitor banks C_{FLY} and C_{MID} connected external to the µModule, are also part of the energy transfer elements. LTM4660 utilizes these capacitor-banks to efficiently deliver energy from input to output. These capacitors are initially precharged in the Capacitor Balancing phase using proprietary control techniques. This balancing eliminates large transient currents seen in similar switched capacitor based topologies. Voltages of capacitor banks are continuously monitored and balanced by LTM4660. Dedicated pins TIMER and HYS_PRGM are provided to set the balancing time interval and voltage window and can be adjusted for each application of LTM4660. Following balancing phase, regular switching action begins. During each switching cycle, capacitor C_{FLY} is connected either in series with or in parallel to C_{MID}. See Operation and Applications Information section.

Capacitor Balancing Phase

During initial power up, voltage across the flying capacitor (C_{FLY}) and C_{MID} are measured. If either of these voltages are not at $V_{IN}/2$, the TIMER's capacitor will be allowed to charge up. When the TIMER capacitor's voltage reaches 0.5V, internal current sources to bring C_{FLY} voltage to $V_{IN}/2$ are turned ON. After the C_{FLY} voltage has reached $V_{IN}/2$, C_{MID} will then be charged to $V_{IN}/2$. The TRACK/SS pin is pulled low during this duration. The $\overline{FAULT}$ pin will

OPERATION

not be pulled low during this initial power up. If the voltages across C_{FLY} and C_{MID} reach $V_{IN}/2$ before the TIMER capacitor's voltage reaches 1.2V, the TRACK/SS will be released and allowed to charge up. The TIMER pin will reset to ground and remain there. Normal operation will begin (see Figure 1a).

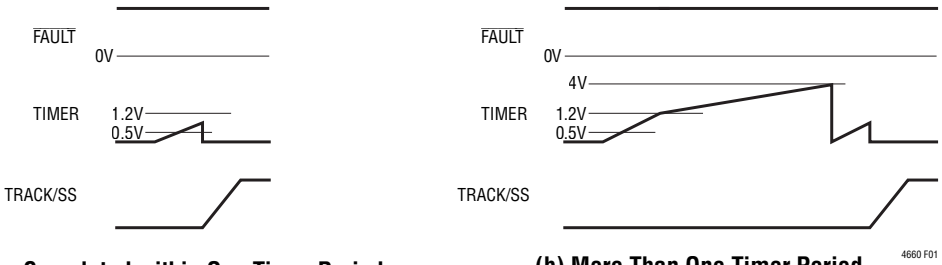
If, however, the C_{FLY} or C_{MID} voltage is not at $V_{IN}/2$ when V_{TIMER} reaches 1.2V, the internal current sources will be turned OFF and the TIMER capacitor will be charged at half the initial rate until it reaches 4V. Timer will then be reset to zero, and the LTM4660 will repeat the above process again until C_{FLY} and C_{MID} are at $V_{IN}/2$. (See Figure 1b).

During normal operation, only C_{MID} is monitored for deviation away from $V_{IN}/2$ by a window amount set by a resistor connected from HYS_PRGM to ground. The voltage across this resistor sets the same amount of window threshold above and below $V_{IN}/2$. If V_{CMID} leaves this voltage window, all switching will stop, and the TRACK/SS pin will be pulled low. Corresponding internal current sources will be turned on to bring C_{FLY} and C_{MID} voltages back to $V_{IN}/2$. $\overline{FAULT}$ will be pulled low and released once the balancing is complete. During this balancing period, PGOOD will also be pulled low. The TRACK/SS pin is also allowed to charge up upon the completion of balancing (see Figure 2). Connecting HYS_PRGM to $INTV_{CC}$ sets the window threshold to ±0.8V around $V_{IN}/2$.

Main Control Loop

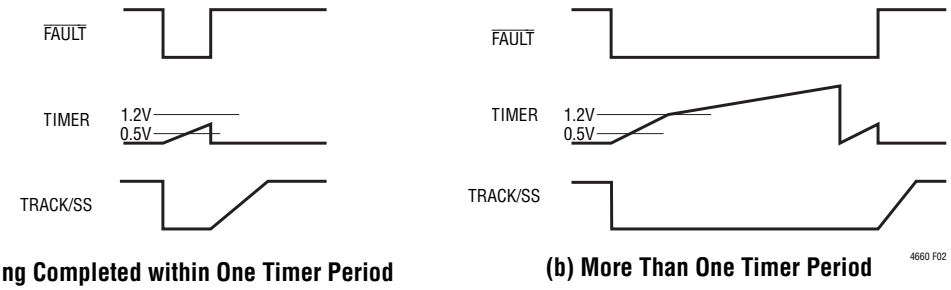
Once the capacitor balancing phase is complete, normal operation begins. Power switches are turned ON/OFF based on peak current in the power inductor. Peak inductor current is controlled by voltage on COMPa pin, which is the output of a transconductance error amplifier. The V_{FB} pin receives the voltage feedback signal from V_{OUT}, which is compared to the internal reference voltage by the error amplifier. When load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference voltage, which in turn causes the COMPa voltage to increase until average inductor current matches the new load current.

During each switching cycle, capacitor C_{FLY} is connected in series with or parallel to C_{MID}. Voltage at C^+ alternates between V_{IN} and $V_{IN}/2$ whereas voltage at C^- alternates between $V_{IN}/2$ and ground. The voltage at MID and across C_{FLY} will each be approximately at $V_{IN}/2$.



(a) Balancing Completed within One Timer Period **(b) More Than One Timer Period**

Figure 1. Charge Balancing During Power-Up



(a) Balancing Completed within One Timer Period **(b) More Than One Timer Period**

Figure 2. Charge Balancing During Normal Operation

APPLICATIONS INFORMATION

The Typical Applications on the first page is a basic LTM4660 application circuit.

$INTV_{CC}/EXTV_{CC}$ Power

Power for power switch drivers and most internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is grounded or tied to a voltage less than 7V, an internal 5.8V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 8V, this linear regulator is turned OFF and another 5.8V linear regulator turns ON to provide the $INTV_{CC}$ power from $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source, resulting in an overall increase in LTM4660 efficiency. For LTM4660 applications where V_{OUT} is greater than 8V, $EXTV_{CC}$ can be directly tied to V_{OUT}.

Shutdown and Start-Up

When RUN pin is below 1.1V, $INTV_{CC}$ linear regulator along with all the internal circuitry including the main control loop enters shutdown mode. Releasing the RUN pin will allow a internal 1µA current source to pull this pin up, thus enabling LTM4660. RUN pin can also be driven directly by logic if this voltage does not exceed the absolute maximum rating of 6V.

The slew rate of the output voltage V_{OUT} can be controlled by the voltage on the TRACK/SS pin. When voltage on TRACK/SS is less than internal reference voltage of 0.8V (or EXT_REF if this feature is utilized), the LTM4660 regulates the V_{FB} voltage to the TRACK/SS voltage instead of to the reference voltage. This allows TRACK/SS pin to be used to program the soft-start period by connecting an external capacitor from the TRACK/SS pin to SGND. After capacitor balancing phase of LTM4660 is completed, an internal 10µA pull-up current charges the soft-start capacitor, creating a voltage ramp. As the voltage on this pin rises linearly from 0V to the reference voltage (and beyond), output voltage V_{OUT} rises smoothly from zero to the final set value. Note that soft-start is achieved not by limiting the maximum output current of LTM4660 but by controlling the output ramp voltage according to the ramp rate at the TRACK/SS pin. The total soft-start time can be calculated with Equation 2.

$$t_{SOFT\text{-}START} = 0.8V \text{ or } V_{EXT\_REF} \bullet \frac{Css}{10\mu A} \quad (2)$$

A 0.1µF capacitor connected between TRACK/SS pin and SGND would be sufficient for most typical IBC applications with LTM4660.

Output Voltage Tracking

Alternatively, TRACK/SS pin allows start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground. Tracking can be configured to be either coincident or ratiometric as shown in Figure 3. In the following discussions, V_{OUT1} refers to another supply's output while V_{OUT2} refers to the LTM4660 output that tracks V_{OUT1}. To implement the coincident tracking in Figure 3a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACK/SS pin of the LTM4660. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 4a. In this tracking mode, V_{OUT1} must be higher than V_{OUT2}. This ensures the final voltage on TRACK/SS pin is greater than 0.8V.

To implement ratiometric tracking shown in Figure 3b, connect a resistor divider R1 and R2 from external supply to TRACK/SS pin of LTM4660. Select R1 and R2 such that when external supply reaches steady state, final voltage on TRACK/SS is less than 0.8V. Use this final voltage to select FB resistor R4 (see Figure 4b). Output voltage V_{OUT2} of LTM4660 which ratiometrically tracks external supply voltage V_{OUT1} is given by Equation 3.

$$V_{OUT2} = \frac{V_{OUT1}\left(1+\frac{60.4k}{R4}\right)}{1+\frac{R1}{R2}} \quad (3)$$

In order to track down another supply after the soft-start has successfully reached 82.5% of 0.8V or V_{EXT_REF}, it is recommended to set the LTM4660 into forced continuous mode operation by setting the MODE/PLLIN = 0V. By selecting different resistors, the LTM4660 can achieve different modes of tracking including the two in Figure 3. The ratio-metric mode has lesser output accuracy on V_{OUT2} but is fully coupled to any variations in V_{OUT1}. In both modes, there is an error in output voltage setting caused by the pin current of TRACK/SS. To minimize this error, use smaller resistor values in the divider.

APPLICATIONS INFORMATION

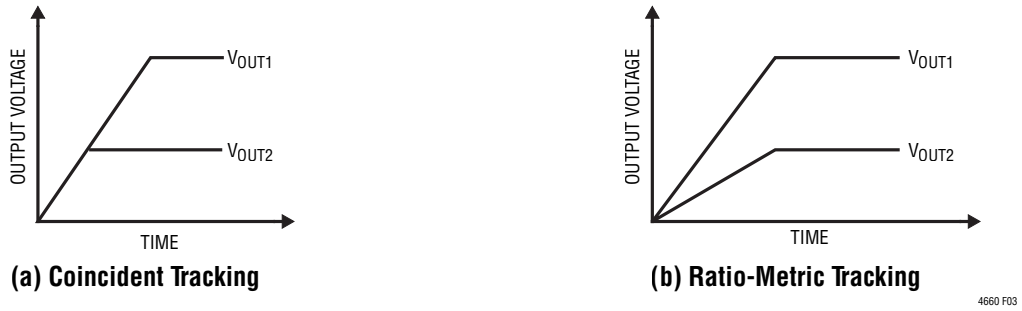


Figure 3. Two Different Methods of Output Voltage Tracking

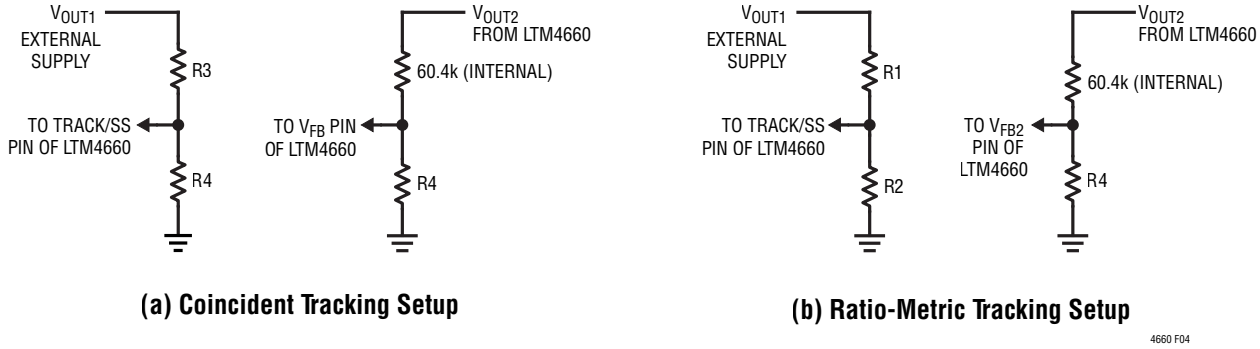


Figure 4. Setup for Coincident and Ratio-Metric Tracking

Burst Mode Operation, Pulse-Skipping Mode, or Forced Continuous Mode

The LTM4660 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous mode. To select forced continuous operation, tie the MODE/PLLIN pin to SGND. To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin. When the controller is enabled for Burst Mode operation, if the average inductor current is higher than the load current, the error amplifier will decrease the voltage on the COMPa pin. When the COMPa voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode) and switching is turned off. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the voltage on COMPa pin begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the power switches on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the controller operates in discontinuous operation. In forced continuous operation, the peak inductor current is determined by the voltage on the COMPa pin. Switching frequency is constant as set by R_{FREQ} resistor and inductor current remains continuous through the switching period. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of faster response to load transients and less interference with audio circuitry. When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTM4660 operates in PWM pulse-skipping mode at light loads. At very light loads, switching is off for few numbers of cycles (i.e., skipping pulses) and the part operates in discontinuous mode. This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. At light loads, pulse-skipping mode provides higher efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Regardless of the

APPLICATIONS INFORMATION

mode selected by MODE/PLLIN pin, LTM4660 will always operate in pulse-skipping mode during start-up.

Frequency Selection and Phase-Locked Loop

The switching frequency of the LTM4660 can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 200kHz to 1MHz. There is a 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. Figure 5 shows variation of switching frequency versus resistor connected from FREQ pin to SGND. For typical datacenter IBC applications of LTM4660 with V_{IN} = 48V or 54V bus voltage and with V_{OUT} = 12V, choose FREQ resistor to be 40k to 60k for maximum efficiency.

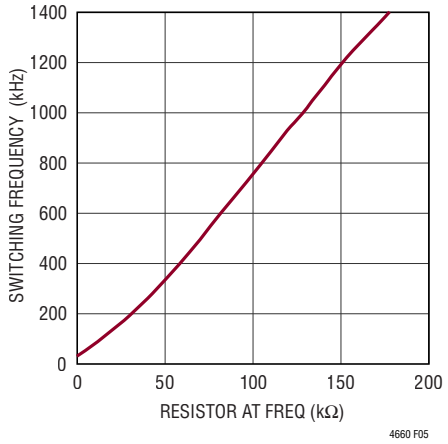


Figure 5. Variation of Switching Frequency vs Resistor Connected from FREQ Pin to SGND

A phase-locked loop (PLL) is integrated on the LTM4660 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. Rising edge of C^- pin synchronizes to the rising edge of the external clock source. The controller operates in forced continuous mode when it is synchronized. The phase-locked loop is capable of locking any frequency within the range of 200kHz to 1MHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Temperature Monitoring

The LTM4660 can provide hotspot monitoring via the TEMP pin. By using a PTC thermistor as the lower leg of a resistor divider and connecting the common point of this divider to the TEMP pin, the voltage increases drastically when the temperature reaches beyond the Curie point of the PTC thermistor as shown in Figure 6. The characteristic of the PTC thermistor is shown in Figure 7. When the TEMP pin reaches 1.22V, all switching stops for 100ms.

The voltage on the TRACK/SS pin and $\overline{FAULT}$ is pulled low and is released after 100ms (Figure 8) if the voltage on the TEMP pin goes below 1.1V during this 100ms timeout. If the TEMP pin voltage remains above 1.1V, the timeout period will be extended until the voltage drops below 1.1V. The temperature that is used to trigger the hotspot protection will determine the thermistor selection. This temperature will be the Curie point of the thermistor, which is often defined as having two times its resistance at 25°C. With the Curie point resistance of the thermistor known, $R2_{CURIE}$, the upper resistance, R1, can be selected by Equation 4.

$$R1 = \frac{R2_{CURIE}\,(V_{EXT} - 1.22)}{1.22} \qquad (4)$$

A diode-connected PNP transistor is connected internally between pins $TEMP^+$ and $TEMP^-$. The transistor is centrally located inside LTM4660, in close proximity to the hotspot. Voltage derived from the $TEMP^+$ and $TEMP^-$ pins provides a close estimate of the internal temperature of LTM4660.

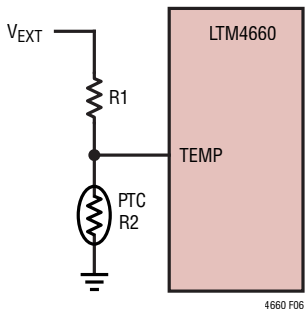


Figure 6. Temperature Monitoring Setup

APPLICATIONS INFORMATION

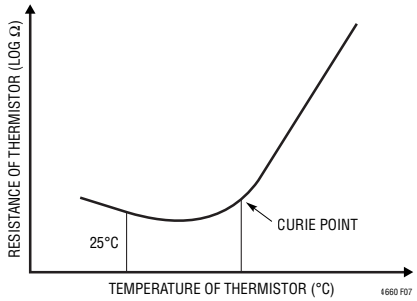


Figure 7. Characteristic of a Thermistor

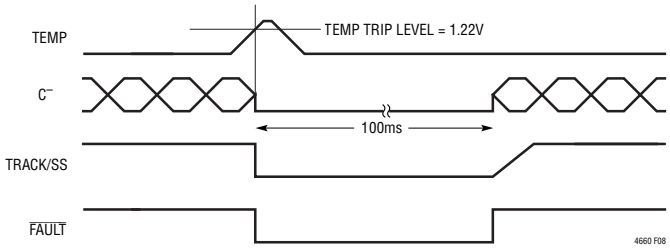


Figure 8. Temperature Trip Characteristic

Power Good

When V_{FB} pin voltage falls below 7.5% or rises above 8.5% of the internal 0.8V reference or the reference set by EXT_REF, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.1V or when the LTM4660 is in the soft-start or tracking phase. The PGOOD pin will flag power good immediately when the V_{FB} pin is within the reference window. However, there is an internal 50µs power bad mask when V_{FB} goes out this window. The PGOOD pin can be pulled up by an external resistor to sources of up to 20V.

$\overline{\text{FAULT}}$

During initial power up of the LTM4660 or when enabling the part via the RUN pin, the $\overline{\text{FAULT}}$ pin will not be pulled low even when C_{FLY} and/or C_{MID} need to be rebalanced to $V_{IN}/2$. But during normal operation, when rebalancing is needed, the $\overline{\text{FAULT}}$ will be pulled low. Another condition that causes the $\overline{\text{FAULT}}$ to go low is thermal shutdown, either caused by the internal temperature reaching 150°C or the voltage at TEMP pin reaching 1.22V. The $\overline{\text{FAULT}}$ pin is allowed to be pulled up by an external resistor to sources of up to 20V.

Frequency Compensation

The LTM4660 µModule employs peak current mode control for pulse width modulation of the power switches. This method of control simplifies the compensation design by eliminating the dynamics of the power inductor contributing to the closed loop response. A Type-II network is sufficient to compensate the LTM4660 feedback loop. Such a network comprises of a resistor in series with capacitor connected at COMPa pin—the output of a transconductance error amplifier inside LTM4660, to SGND. A high frequency roll-off capacitor of 22pF, as part of the Type-II network is already connected at the COMPa pin internal to LTM4660.

Choose the components of the Type-II network dependent on the desired output response for line and load variations as well as loop stability parameters phase margin and gain margin of the feedback loop. In general, selecting a low capacitance and a high resistance for the Type-II network at COMPa pin leads to fast transient response but may adversely affect the loop stability parameters.

A resistor capacitor network of 10k in series with 10nF is connected from COMPb pin to SGND internal to LTM4660. For most LTM4660 applications, it is sufficient to tie COMPa and COMPb pins together to ensure closed loop stability across line and load variations. Refer to LTM4660 model in LTspice® to fine tune and optimize the Type-II network for each application circuit with LTM4660.

Input Capacitor Selection

The LTM4660 module should be connected to a low AC-impedance DC source. For the regulator input, two 10µF input ceramic capacitors are required for RMS ripple current. A 33µF or 47µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitance is only needed if the input source impedance is compromised by long inductive leads. If low impedance power planes are used, then this bulk capacitor is not needed. For IBC applications with 48V or 54V bus, choose input capacitors rated to at least 100V.

APPLICATIONS INFORMATION

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated by Equation 5.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2 \bullet \eta\%} \bullet \sqrt{(D \bullet D')} \quad (5)$$

where D is $2 \bullet V_{OUT}/V_{IN}$ and D' = 1 – D

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or Polymer capacitor.

Output Capacitor Selection

The LTM4660 is designed to achieve good transient response and low output voltage ripple. Choose C_{OUT} with low ESR to meet the output ripple and transient performance requirements. Place at least two 10µF output ceramic capacitors close to V_{OUT} and GND pins. This lowers the output ripple by lowering the total ESR of C_{OUT}. Aluminum electrolytic capacitors of 100µF or 150µF can be placed further away as bulk output capacitors. Choose enough bulk capacitance to meet the transient specification demanded by downstream loads. When choosing C_{OUT}, be aware of the impact of its ESR on loop stability. Refer to LTM4660 model in LTspice to optimize and fine tune the combination of C_{OUT} for each LTM4660 application.

C_{FLY} and C_{MID} Selection

For the LTM4660 µModule, capacitor banks C_{FLY} and C_{MID} connected external to the µModule, are part of the energy transfer elements. Therefore, ceramic capacitors are attractive since they have the lowest ESR. However, care should be taken when choosing this type of capacitors. During operation the DC voltage across C_{FLY} and C_{MID} is approximately half the V_{IN} supply, therefore the voltage rating of the capacitors should be greater than that. As a general rule, select the voltage rating of the capacitor to be twice the operating voltage of the capacitor. For the same voltage rating and capacitance, a larger case size will have a lower failure rate.

In addition, the operating temperature of the capacitors needs to be considered. For operating temperature above 85°C, capacitors with the X7R dielectric need to be used while X5R dielectric is adequate for operation below 85°C. For long term reliability of the capacitor, keep the temperature rise of the capacitor to be below 20°C, preferably 10°C. The temperature rise of the capacitor is dependent on the amount of RMS current through the capacitor and the operating frequency.

Ceramic capacitors also have a large voltage coefficient, losing close to half their capacitance when the DC bias across a given capacitor is half its rated voltage. The DC bias effect on a capacitor is greater when the case size is smaller. Factor in these effects when deciding on the capacitance.

The ripple voltage on C_{FLY} and C_{MID} is given by Equation 6.

$$V_{RIPPLE} = \frac{I_{OUT}}{C_{BANK} \bullet f_{SW}} \frac{2V_{OUT}}{V_{IN}} \quad (6)$$

where C_{BANK} is either C_{FLY} or C_{MID}, I_{OUT} is output current and f_{SW} is the switching frequency.

Ripple voltage on C_{FLY} and C_{MID} contributes significantly to the power dissipated in LTM4660 (see Efficiency figures in Typical Performance Characteristics section). As a good starting point, select enough capacitance such that the ripple on each capacitor is less than 1% of the DC bias voltage of the capacitor. For example, if the DC bias voltage of the capacitor is 24V, keep the ripple to be less than 240mV. To achieve lowest loss in LTM4660, select the capacitance of C_{MID} to be same as that of C_{FLY}.

LTM4660 is designed to deliver 300W of output power at $12V_{OUT}$. For maximum efficiency at 300W, use eight to twelve 10µF ceramic capacitors each for C_{MID} and C_{FLY}. Considering the voltage derating of ceramic capacitors, for bus voltages in range of $48V_{IN}$ to $54V_{IN}$, choose ceramic capacitors rated to at least 50V.

Timer and Hysteresis

The LTM4660 µModule uses a switched capacitor hybrid topology where the switched capacitor stage consists of C_{FLY} and C_{MID} capacitor banks connected alternately in series or in parallel through the power switches inside LTM4660. During start-up, C_{FLY} and C_{MID} capacitors are completely discharged. Starting switching with the capacitors discharged may lead to undesirably high currents through the power switches. To circumvent this phenomenon, LTM4660 uses a patented technology to balance the charge across the C_{FLY} and C_{MID} to half of V_{IN} during start-up.

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Capacitor connected at TIMER pin to SGND defines the time-period during which LTM4660 enters capacitor balancing phase. An internal current source at the pin charges the TIMER capacitor generating a voltage ramp. Capacitor balancing is initiated when the voltage at this pin is between 0.5V and 1.2V. Choose this capacitor based on the maximum input voltage and the capacitance of capacitor banks C_{FLY} and C_{MID}. Higher input voltage and higher capacitance indicates more time necessary for LTM4660 to complete capacitor balancing, hence requiring a larger TIMER capacitor. Choosing a smaller TIMER capacitor leads to LTM4660 using multiple TIMER cycles to complete capacitor charge balancing leading to longer start-up times.

A TIMER capacitor of 1µF is sufficient for V_{IN} of up to 60V and $C_{MID} = C_{FLY} = 10µF \bullet 12$.

HYS_PRGM Voltage

The voltage on the HYS_PRGM pin sets a window centered on $V_{IN}/2$ for fault protection purposes. During operation, if the voltage at MID_SNS deviates beyond this window, a fault is indicated, and capacitor balancing begins. Therefore, setting the correct window is important as it adds another layer to of protection to LTM4660 application circuit.

During normal operation, voltage at MID may settle to a voltage less than $V_{IN}/2$ depending on the impedance looking into MID and output current. In general, higher the I_{OUT}, higher would be the deviation of MID from $V_{IN}/2$. Similarly, lower the C_{MID} and switching frequency, higher the impedance looking into MID. In addition to the DC offset of MID relative to $V_{IN}/2$, the AC ripple on C_{MID} is also to be considered (Refer to Equation 6 in C_{FLY} and C_{MID} Selection section) when choosing the HYS_PRGM window.

For most LTM4660 applications, a hysteresis window of 1V is sufficient to ensure proper operation. To set the window to 1V, connect a 100k resistor from HYS_PRGM to SGND.

Output Voltage Setting

The LTM4660 uses its internal reference of 0.8V when EXT_REF is tied to $INTV_{CC}$. The output voltage is given by Equation 7. Always set V_{OUT} to be less than half of the minimum expected input voltage.

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{60.4k}{R1}\right) \quad (7)$$

Applying a voltage on EXT_REF pin between 0.45V and 0.9V allows LTM4660's output to track the EXT_REF voltage, indicated by the characteristic in Figure 9.

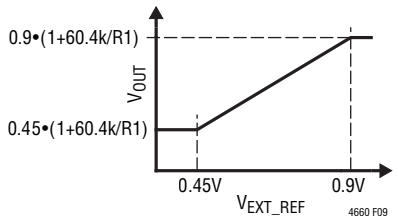

Figure 9. Output Voltage Set by EXT_REF Pin

Due to its unique architecture, the optimal efficiency for the LTM4660 is when $V_{OUT} = V_{IN}/4$. Efficiency for step-down ratios higher or lower than 4:1 may be lower. For applications that demand optimal efficiency within a range of V_{IN}, EXT_REF could be used to track this V_{IN} variation while maintaining a 4:1 step down ratio at the output. In this type of setup, the output voltage will also change with the input. Figure 10 shows a 48V to 12V setup that accounts for V_{IN} variation between 36V to 60V.

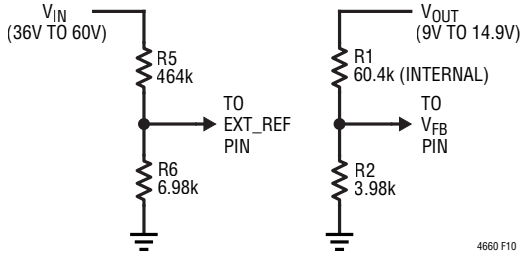

Figure 10. Output Voltage to Track V_{IN} in 4:1 Ratio

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that LTM4660 is able to turn on its power switches. Low duty cycle applications may approach minimum on-time limit and care should be taken to ensure Equation 8.

$$\frac{2V_{OUT}}{V_{IN}} \bullet \frac{1}{f_{SW}} > t_{ON(MIN)} \quad (8)$$

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If duty cycle falls below what can be accommodated by the minimum on-time, the LTM4660 will begin to skip cycles. Output voltage will continue to be regulated but ripple voltage and current will increase. $t_{ON(MIN)}$ for LTM4660 is 210ns for 4:1 step-down ratios and it linearly increases for higher step-down ratios. To avoid running into minimum on-time of LTM4660 switching, it is recommended that switching frequency be reduced to 200kHz to 400kHz for input output step down ratios greater than 6:1.

Dual Phase Operation

For higher output power applications, two LTM4660s can be easily paralleled to create a dual phase single output configuration. Figure 23 shows the key signal connections between the two LTM4660s.

Thermal Considerations

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD 51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD 51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board.

A graphical representation of the aforementioned thermal resistances is given in Figure 11; blue resistances are

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contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-9 to predict power loss heat flow.

The LTM4660 package has been designed such that inductor on top also doubles as a heat sink, removing heat from the power switches below. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 12 shows a thermal capture of LTM4660 with 48V input, 12V output at 25A without heat sink and 200LFM airflow condition.

Recommended PCB footprint

The high integration of LTM4660 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, MID, GND and V_{OUT} pins to minimize high frequency noise.
- Use short loops to route C_{FLY} capacitors from C^+ to C^-. Reduce the parasitic trace inductance and resistance in this loop.

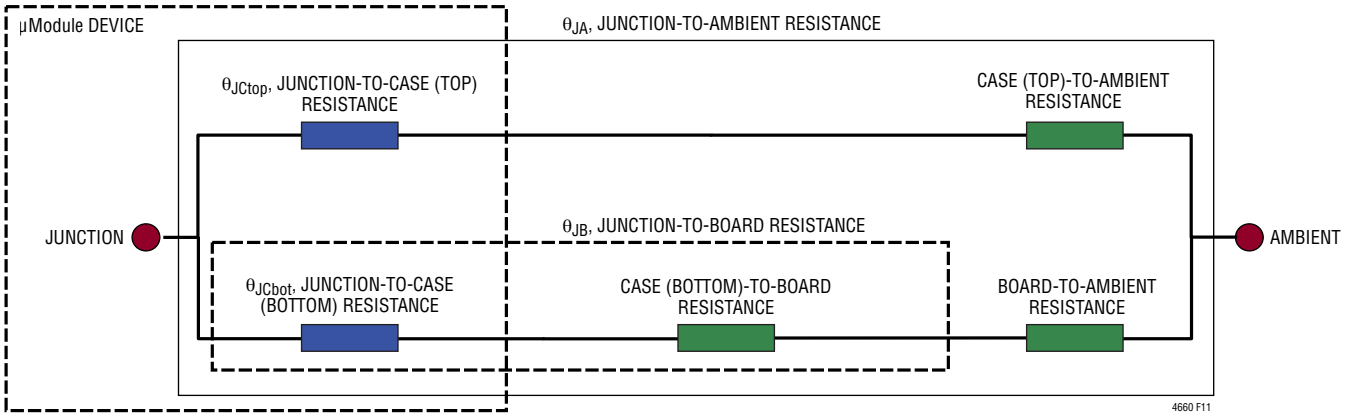


Figure 11. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

APPLICATIONS INFORMATION

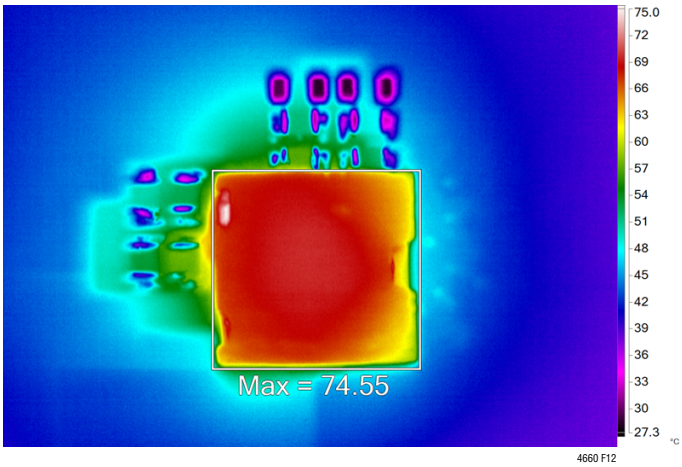


Figure 12. Thermal Image 48V to 12V, 25A; 200LFM Airflow; No Heat Sink (Based on 6-Layer PCB with 2oz Copper on All Layers)

- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. SGND is connected to GND internal to the module.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 13 gives a good example of the recommended layout for input, output, C_{FLY} and C_{MID} capacitors on the top layer. Pinout of LTM4660 is designed such that C_{FLY} capacitors can be conveniently placed on the bottom layer right underneath the module, with minimal impact to total PCB area. (See Figure 14 for example of bottom layer layout).

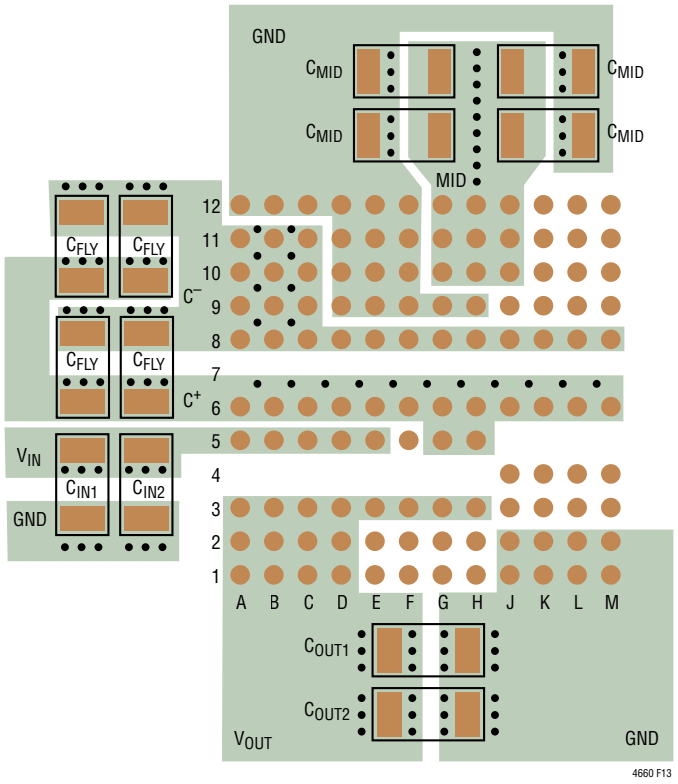


Figure 13. Recommended Layout for Top Layer

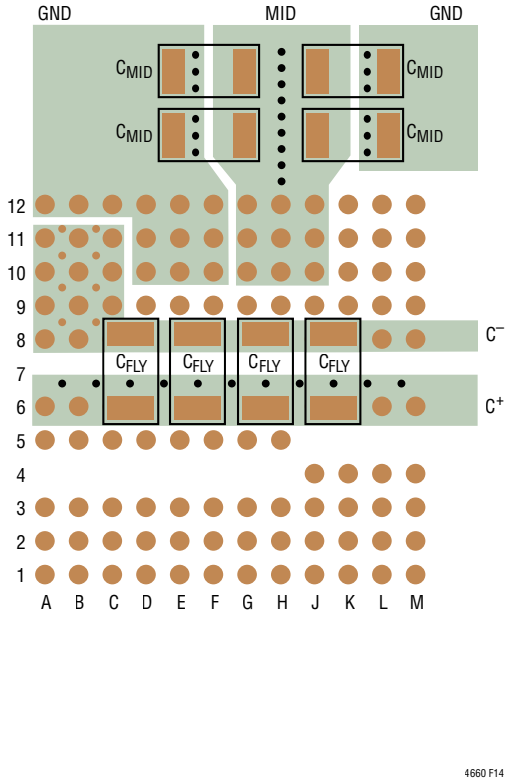


Figure 14. Recommended Layout for Bottom Layer

APPLICATIONS INFORMATION

Table 1. Bulk and Ceramic Capacitor Manufacturers

C_{IN} (BULK)			C_{OUT} (BULK)		
VENDORS	**VALUE**	**PART NUMBER**	**VENDORS**	**VALUE**	**PART NUMBER**
Panasonic	33µF, 80V	EEHZA1K330	Panasonic	150µF, 16V	16SVPC150
C_{IN} (CERAMIC)			C_{FLY}, C_{MID}		
VENDORS	**VALUE**	**PART NUMBER**	**VENDORS**	**VALUE**	**PART NUMBER**
Murata	2.2µF, 100V, 1210, X7R	GRM32DR72A225KA12	Murata	10µF, 100V, 1210, X7S	GRM32EC72A106KE05
TDK	2.2µF, 100V, 1210, X7R	C3225X7R2A225K230AB	TDK	10µF, 100V, 1210, X7R	C3225X7R2A106K250AC
C_{OUT} (CERAMIC)			Murata	10µF, 50V, 1210, X7S	GCM32EC71H106KA03
VENDORS	**VALUE**	**PART NUMBER**	TDK	10µF, 50V, 1210, X7R	C3225X5R1H106K250AB
Murata	10µF, 25V, 1210, X7S	GCM32EC7YA106KA03			
TDK	10µF, 25V, 1210, X7R	C3225X7R1E106K250AC			

Table 2. Component Selection Table for Typical LTM4660 Applications

V_{IN} (V)	V_{OUT} (V) I_{OUT} = 25A	C_{IN} (BULK) (µF)	C_{IN} (CERAMIC) (µF)	C_{OUT} (BULK) (µF)	C_{OUT} (CERAMIC) (µF)	C_{FLY} (µF)	C_{MID} (µF)	R_{VFB} (kΩ)	R_{FREQ} (kΩ)	R_{HYS_PRGM} (kΩ)	TIMER (µF)
48	12	33	10	150 ×2	10 ×3	10 ×10	10 ×10	4.32	49.9	100	1
54	12	22	10	150 ×2	10 ×3	10 ×12	10 ×12	4.32	49.9	100	1
48	5	33	10	100 ×2	10 ×2	10 ×12	10 ×12	11.49	39.9	100	1
54	9	22	10	100 ×2	10 ×2	10 ×10	10 ×10	5.92	43.2	100	1

Safety Considerations

The LTM4660 does not provide galvanic isolation between the input and output. There is no internal fuse. If required, a slow blow fuse with a rating of twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. The temperature diode along with TEMP pin can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

BGA pinout of LTM4660 is such that high voltage pins (V_{IN} and C+) have a clearance of one BGA ball from adjacent lower voltage pins.

Power Derating

Derating curves in Figure 15 to Figure 20 can be used to calculate approximate values of θ_{JA} thermal resistance with various airflow conditions.

Radiated EMI Noise

Potential for EM interference (EMI) is inherent to all switching regulators. Fast switching turn-on and turn-off of the power MOSFETs—necessary for achieving high efficiency—create high frequency (~30MHz +) di/dt changes within DC/DC converters. This activity tends to be the dominant source of high frequency EMI radiation in such systems. The high level of device integration within LTM4660 along with soft switching of power MOSFETs delivers low radiated EMI noise performance. EMI graph in the Typical Performance Characteristics section shows an example of LTM4660 meeting radiation emission limits established by CISPR22 Class B.

APPLICATIONS INFORMATION (C_{MID} and C_{FLY} = 10µF × 12, unless otherwise specified)

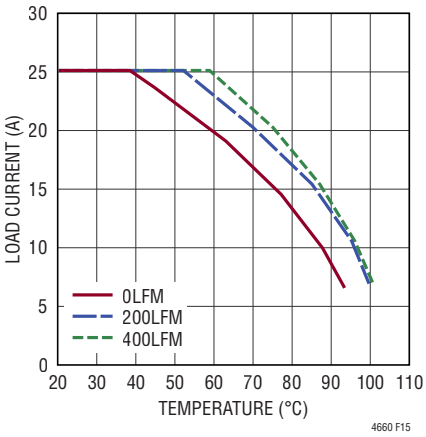


Figure 15. 48V to 12V Derating Curve, No Heat Sink

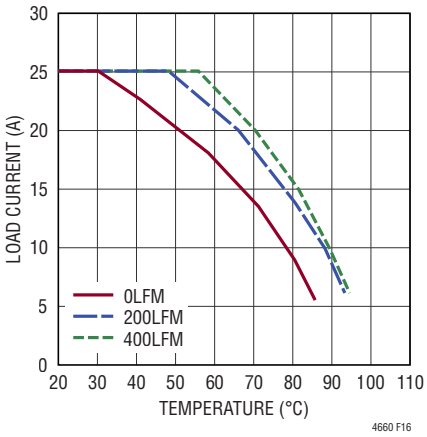


Figure 16. 54V to 12V Derating Curve, No Heat Sink

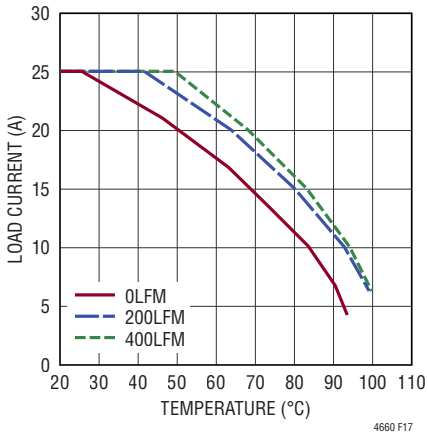


Figure 17. 48V to 15V Derating Curve, No Heat Sink

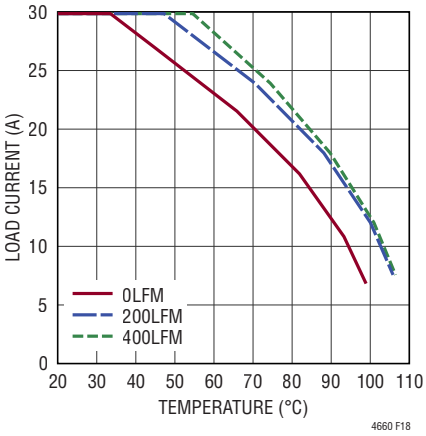


Figure 18. 48V to 5V Derating Curve, No Heat Sink

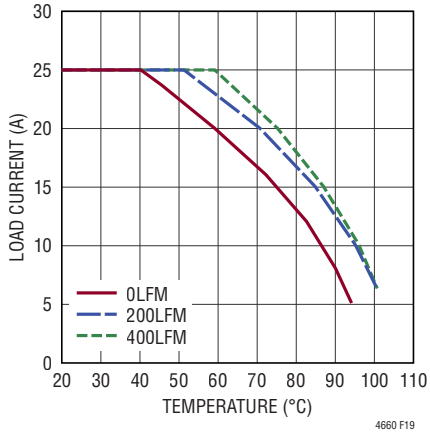


Figure 19. 48V to 12V Derating Curve, No Heat Sink, C_{FLY} and C_{MID} = 10µF × 10

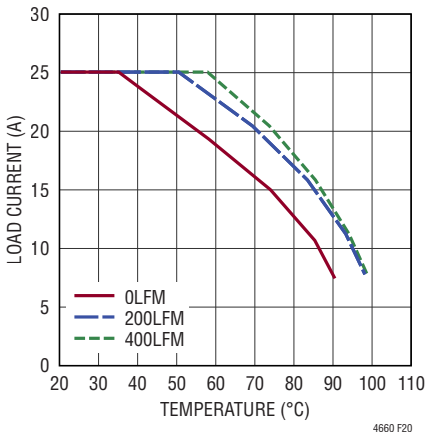


Figure 20. 48V to 12V Derating Curve, No Heat Sink, C_{FLY} and C_{MID} = 10µF × 8

TYPICAL APPLICATIONS

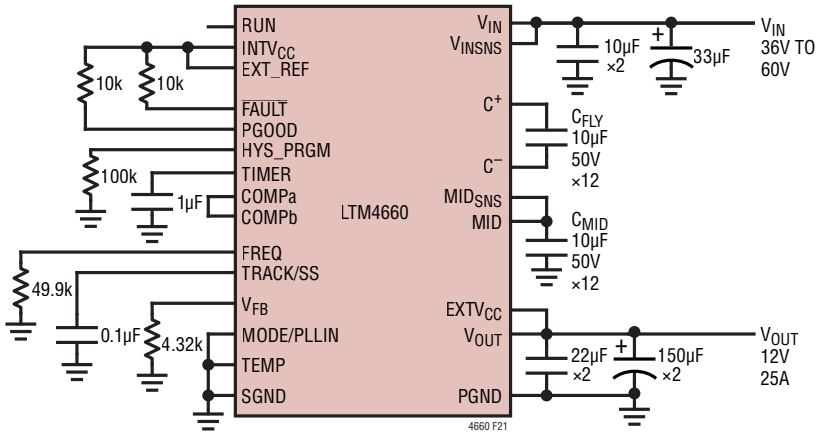
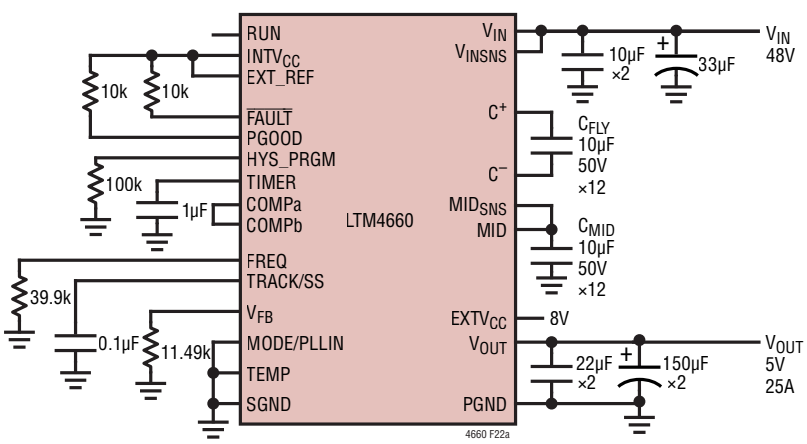


Figure 21. 12V_{OUT} 25A Intermediate Bus Converter



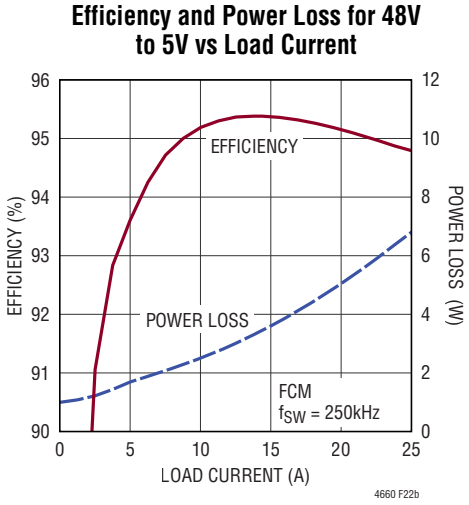
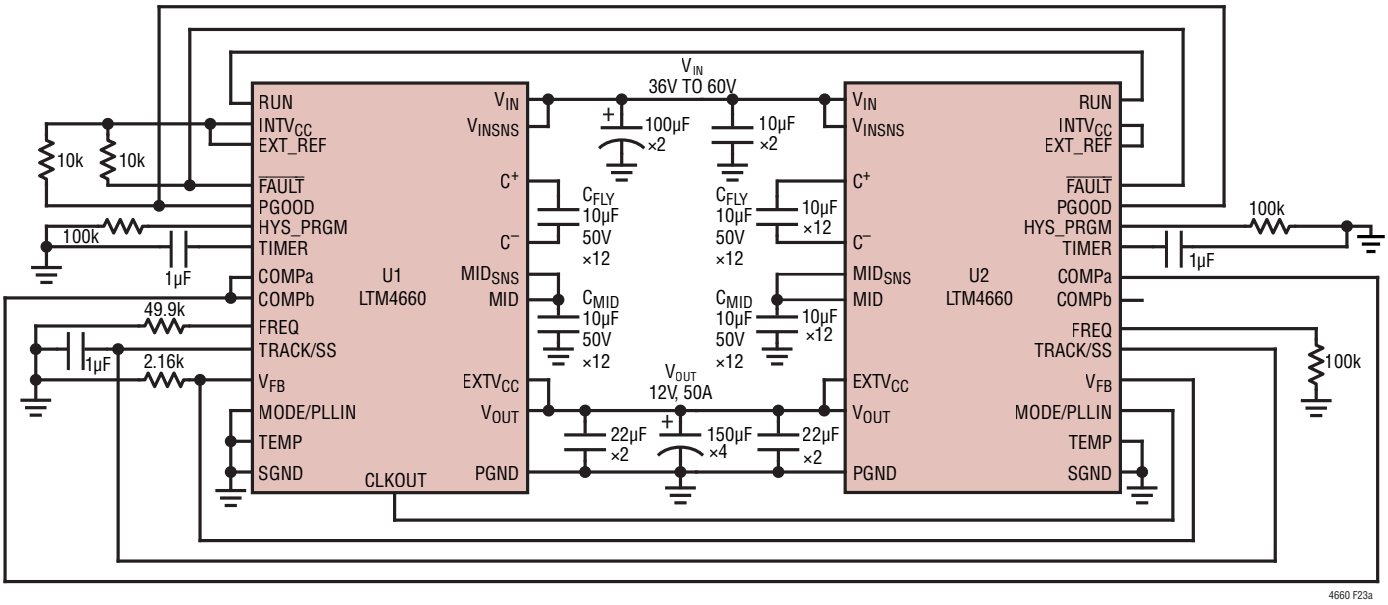


Figure 22. A 48V to 5V Step-Down Converter

TYPICAL APPLICATIONS



Current Sharing

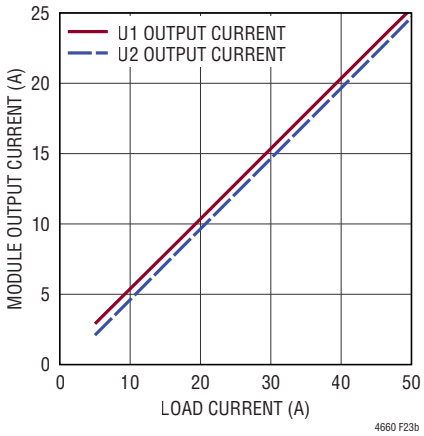


Figure 23. LTM4660 Configured for Dual Phase Operation: 48V to 12V at 50A Step-Down Converter

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

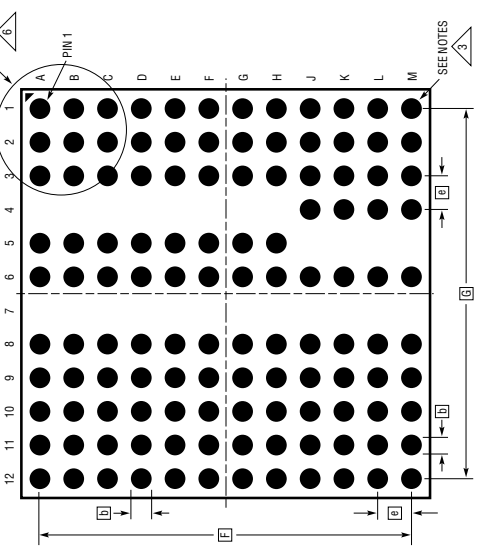
LTM4660 BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}	D1	V_{OUT}	E1	MID	F1	MID
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}	D2	V_{OUT}	E2	MID	F2	MID
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}	D3	V_{OUT}	E3	V_{OUT}	F3	V_{OUT}
A4	(NO PIN)	B4	(NO PIN)	C4	(NO PIN)	D4	(NO PIN)	E4	(NO PIN)	F4	(NO PIN)
A5	V_{IN}	B5	V_{IN}	C5	V_{IN}	D5	V_{IN}	E5	V_{IN}	F5	V_{INSNS}
A6	C^+	B6	C^+	C6	C^+	D6	C^+	E6	C^+	F6	C^+
A7	(NO PIN)	B7	(NO PIN)	C7	(NO PIN)	D7	(NO PIN)	E7	(NO PIN)	F7	(NO PIN)
A8	C^-	B8	C^-	C8	C^-	D8	C^-	E8	C^-	F8	C^-
A9	C^-	B9	C^-	C9	C^-	D9	GND	E9	GND	F9	GND
A10	C^-	B10	C^-	C10	C^-	D10	GND	E10	GND	F10	GND
A11	C^-	B11	C^-	C11	C^-	D11	GND	E11	GND	F11	GND
A12	GND	B12	GND	C12	GND	D12	GND	E12	GND	F12	GND

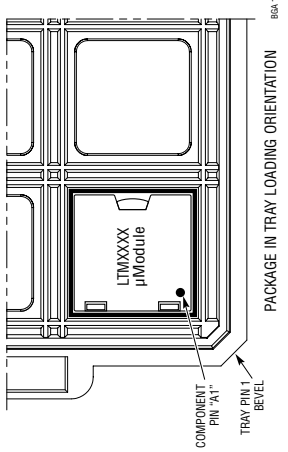
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	MID	H1	MID	J1	GND	K1	GND	L1	GND	M1	GND
G2	MID	H2	MID_{SNS}	J2	GND	K2	GND	L2	GND	M2	PGOOD
G3	V_{OUT}	H3	V_{OUT}	J3	$\overline{FAULT}$	K3	TIMER	L3	RUN	M3	MODE/PLLIN
G4	(NO PIN)	H4	(NO PIN)	J4	$INTV_{CC}$	K4	TEST	L4	SGND	M4	CLKOUT
G5	C^+	H5	C^+	J5	(NO PIN)	K5	(NO PIN)	L5	(NO PIN)	M5	(NO PIN)
G6	C^+	H6	C^+	J6	C^+	K6	C^+	L6	C^+	M6	C^+
G7	(NO PIN)	H7	(NO PIN)	J7	(NO PIN)	K7	(NO PIN)	L7	(NO PIN)	M7	(NO PIN)
G8	C^-	H8	C^-	J8	C^-	K8	C^-	L8	C^-	M8	C^-
G9	GND	H9	GND	J9	$TEMP^+$	K9	$TEMP^-$	L9	TRACK/SS	M9	EXT_REF
G10	MID	H10	MID	J10	MID	K10	$EXTV_{CC}$	L10	COMPb	M10	COMPa
G11	MID	H11	MID	J11	MID	K11	TEMP	L11	HYS_PRGM	M11	FREQ
G12	MID	H12	MID	J12	MID	K12	V_{FB}	L12	SGND	M12	SGND

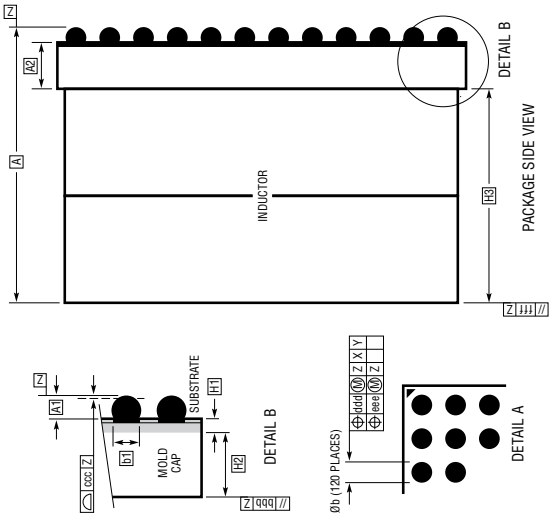
PACKAGE DESCRIPTION

BGA Package
120-Lead (16mm × 16mm × 10.34mm)
(Reference LTC DWG # 05-08-1623 Rev Ø)

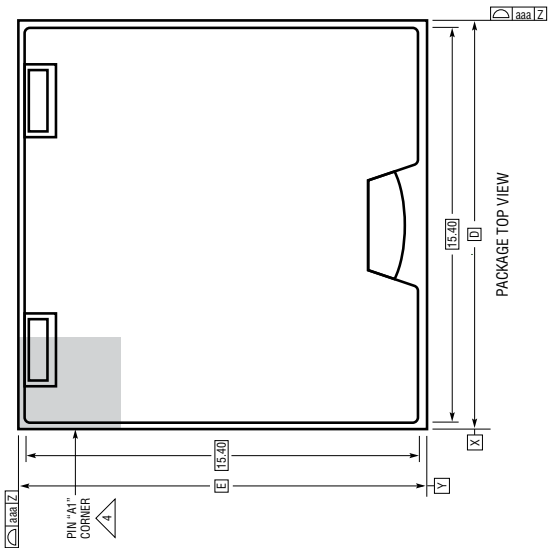


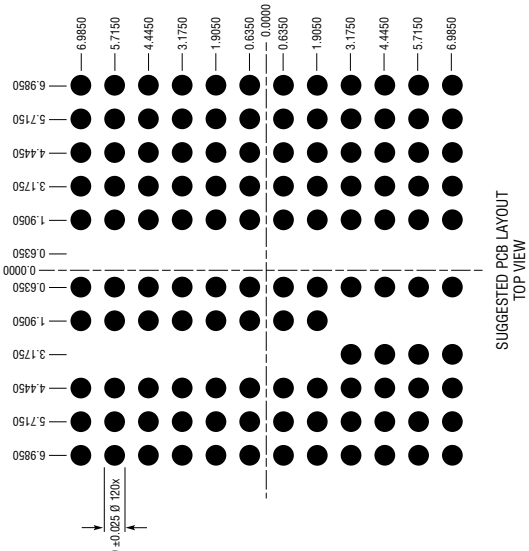
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





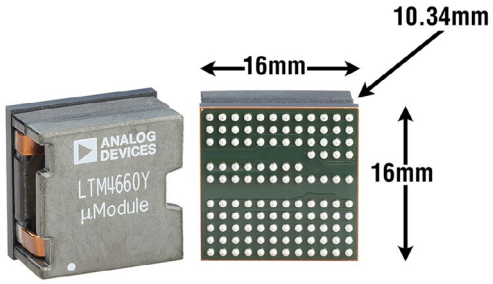
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	9.94	10.34	10.74	
A1	0.50	0.60	0.70	BALL HT
A2	1.72	1.82	1.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
H3	7.72	7.92	8.12	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
fff			0.35	
TOTAL NUMBER OF BALLS: 120				



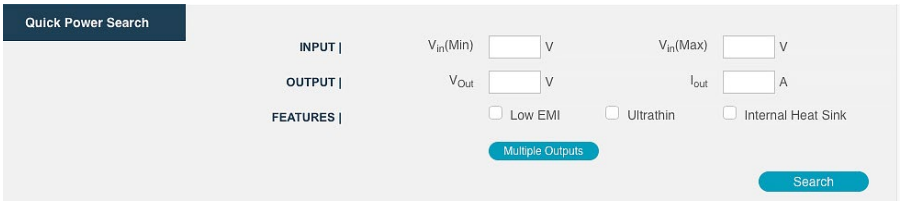


PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4664	54V_{IN} Dual 25A or Single 30A µModule Regulator with PMBus Interface	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA
LTM4664A	54V_{IN} Dual 30A or Single 60A µModule Regulator with PMBus Interface	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA
LTM4681	Quad 31.25A or Single 125A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 15mm × 22mm × 8.17mm BGA
LTM4700	Dual 50A or Single 100A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V, 15mm × 22mm × 7.87mm BGA
LTM4680	Dual 30A or Single 60A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.82mm BGA
LTM4678	Dual 25A or Single 50A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 5.86mm BGA
LTM4650	Dual 25A or Single 50A µModule Regulator	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4650A	Dual 25A or Single 50A µModule Regulator with High V_{OUT} Range	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V, 16mm × 16mm × 5.01mm BGA, 16mm × 16mm × 4.41mm LGA