

TPS7B82EVM-024 Evaluation module

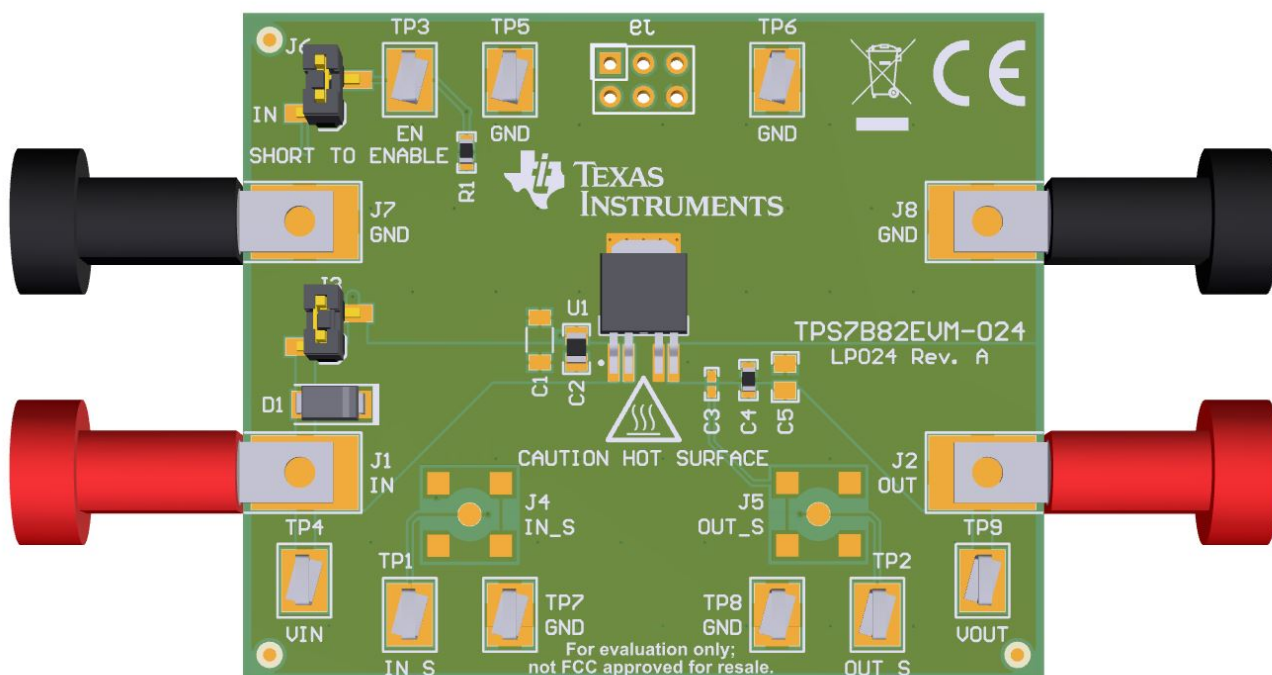


Figure 1. TPS7B82EVM-024 Evaluation Module

This user's guide describes the operational use of the TPS7B82EVM-024 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7B8233QKVURQ1, low-dropout linear regulator (LDO). Included in this user's guide are setup and operating instructions, layout guidelines, a printed circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM).

Throughout this document, the terms *demonstration kit*, *evaluation board*, and *evaluation module* are synonymous with the TPS7B82EVM-024.

Table 1 lists the related documentation available through the Texas Instruments web site at www.ti.com.

Table 1. Related Documentation

Device	Literature Number
TPS7B82-Q1	SLVSDQ0

Contents

1	Introduction	3
1.1	Before You Begin	3
2	EVM Setup.....	4
2.1	Input/Output Connectors and Jumper Descriptions	4
2.2	Soldering Guidelines	5
2.3	Equipment Connection	5
3	Operation	5
4	PCB Layout.....	6
5	Schematic.....	7
6	Bill of Materials	8

List of Figures

1	TPS7B82EVM-024 Evaluation Module	1
2	Assembly Layer	6
3	Top Layer Routing	6
4	Bottom Layer Routing	6
5	TPS7B82EVM-024 Schematic	7

List of Tables

1	Related Documentation	1
2	TPS7B82EVM-024 BOM.....	8

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

Texas Instruments' TPS7B82EVM-024 EVM helps design engineers evaluate the operation and performance of the TPS7B82-Q1 linear regulator for possible use in their own circuit application. This particular EVM configuration contains a single 300-mA, high-voltage, ultra-low- I_O , low-dropout regulator for automotive systems. The regulator is capable of delivering up to 300 mA to the load with a wide V_{IN} range of up to 40 V (45 V transient). For stability, use a 2.2- μ F (or larger) output capacitor for the TPS7B82-Q1.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS7B82EVM-024. Observe all safety precautions.



Warning

Warning Hot surface. Contact may cause burns. Do not touch.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The circuit module is not a finished product or electrical appliance. The module does not contain current or voltage thresholds for circuit protection. It must be used by qualified personnel with additional equipment for evaluation only.

2 EVM Setup

This section describes how to properly connect and setup the TPS7B82EVM-024, including the jumpers and connectors on the EVM board.

2.1 Input/Output Connectors and Jumper Descriptions

2.1.1 J1: IN

Input power-supply voltage connector. Twist together the positive input lead and ground return lead from the input power supply, and keep them as short as possible to minimize input inductance.

2.1.2 J2: OUT

Regulated output voltage connector.

2.1.3 J3: Diode Bypass

Diode D1 bypass. To bypass diode D1, connect a jumper to short the two terminals of J3.

2.1.4 J4: IN_S

Input sense.

2.1.5 J5: OUT_S

Output sense.

2.1.6 J6: Short to Enable

Output enable. To enable the output, connect a jumper to short V_{IN} to EN.

There is a pulldown resistor, R1, between EN and GND so that the output is disabled when EN is not driven to a higher voltage. If making I_{GND} measurements, be sure to remove R1.

2.1.7 J7: GND

Input ground return connector.

2.1.8 J8: GND

Output ground return connector.

2.1.9 J9: Unpopulated Through-Hole Test Points

Through-hole test points that are unpopulated for debugging purposes.

2.1.10 TP1: IN_S

Input sense test point.

2.1.11 TP2: OUT_S

Output sense test point.

2.1.12 TP3: EN

Enable test point.

2.1.13 TP4: VIN

V_{IN} test point.

2.1.14 TP5: GND

Ground test point.

2.1.15 TP6: GND

Ground test point.

2.1.16 TP7: GND

Ground test point.

2.1.17 TP8: GND

Ground test point.

2.1.18 TP9: VOUT

V_{OUT} test point.

2.2 Soldering Guidelines

To avoid damaging the integrated circuit (IC), use a hot-air system for any solder rework to modify the EVM for the purpose of repair or other application reasons.

2.3 Equipment Connection

Connect the equipment as described in the following steps:

1. Set the input power supply up to 40 V (max) and turn the power supply off.
2. Connect the positive voltage lead from the input power supply to IN at the J1 connector of the EVM.
3. Connect the ground lead from the input power supply to GND at the J7 connector of the EVM.
4. Connect a 0-A to 300-mA load between OUT at the J2 and GND at the J8 connector of the EVM.
5. Disable the output by floating J6.

3 Operation

Operate the equipment using the following steps:

1. Turn on the power supplies.
2. Enable the output by jumping J6 (the EN pin) to VIN.
3. Vary the respective load and input voltage, as necessary, for test purposes.

4 PCB Layout

Figure 2 to Figure 4 show the PCB layout for this EVM.

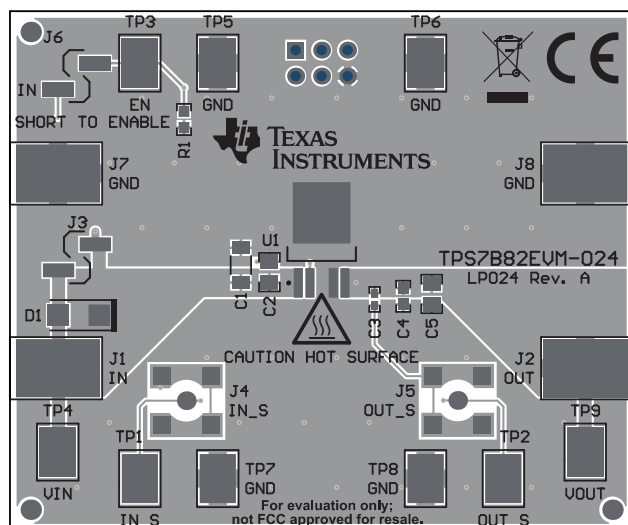


Figure 2. Assembly Layer

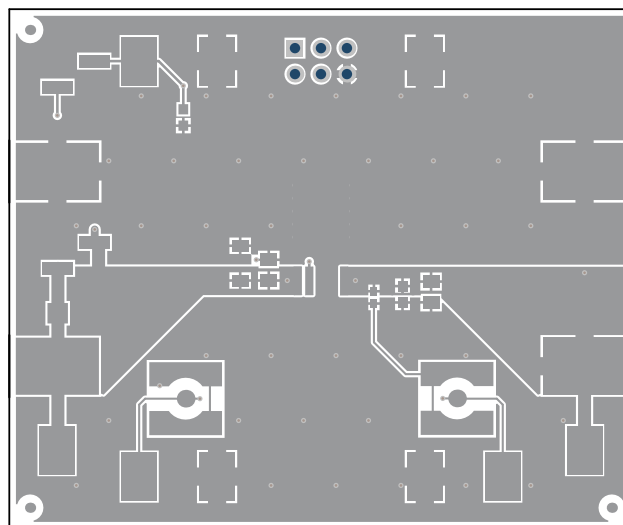


Figure 3. Top Layer Routing

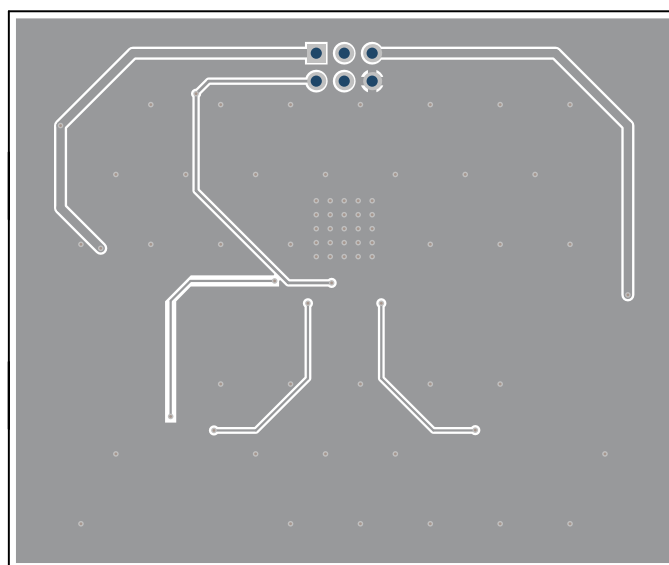


Figure 4. Bottom Layer Routing

5 Schematic

Figure 5 is the schematic for this EVM.

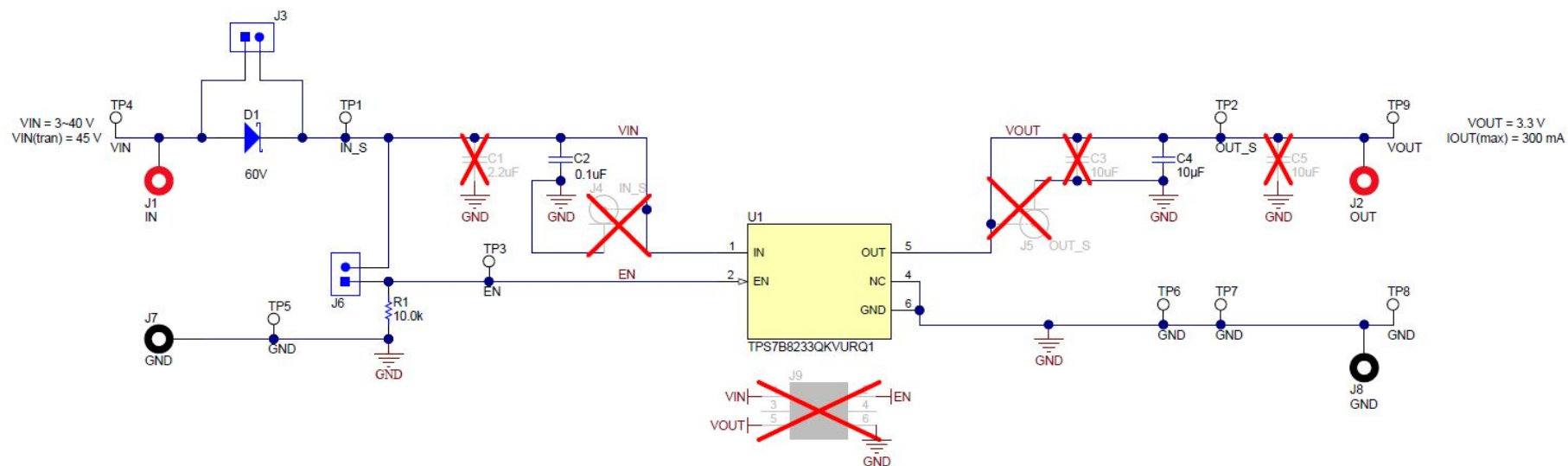


Figure 5. TPS7B82EVM-024 Schematic

6 Bill of Materials

Table 2 lists the BOM for this EVM.

Table 2. TPS7B82EVM-024 BOM⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP024	Any		
C2	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805	0805	GRM21BR71H104KA01L	MuRata	GRM21BC71E106ME11L	MuRata
C4	1	10uF	CAP, CERM, 10 uF, 10 V, +/- 10%, X5R, 0603	0603	GRM188R61A106KE69D	MuRata		
D1	1	60V	Diode, Schottky, 60 V, 2 A, SMA	SMA	B260A-13-F	Diodes Inc.		
J1, J2	2		Standard Banana Jack, Insulated, Red	6091	6091	Keystone		
J3, J6	2		Header, 2.54 mm, 2x1, Gold, R/A, SMT	Header, 2.54 mm, 2x1, R/A, SMT	878980204	Molex		
J7, J8	2		Standard Banana Jack, Insulated, Black	6092	6092	Keystone		
R1	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RCG060310K0FKEA	Vishay Draloric		
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		Automotive 300-mA high-voltage ultra-low-Iq low-dropout (LDO) regulator, KVVU0005A (TO-252-5)	KVVU0005A	TPS7B8233QKVURQ1	Texas Instruments		
C1	0	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, 1206	1206	GRM31CR71H225KA88L	MuRata		
C3	0	10uF	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0402	0402	GRM155R60J106ME15D	MuRata		
C5	0	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	0805	GRM21BR61E106KA73L	MuRata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J4, J5	0		Connector, SMA Jack, Vertical, Gold, SMD	SMA	142-0711-201	Cinch Connectivity		
J9	0		Header, 100mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions		

⁽¹⁾ These assemblies are ESD sensitive, observe ESD precautions.

⁽²⁾ These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.

⁽³⁾ These assemblies must comply with workmanship standards IPC-A-610 Class 2.

⁽⁴⁾ Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts may be substituted with equivalents.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated