NHD-2.23-12832UMY3

OLED Display Module

NHD-	Newhaven Display
2.23-	2.23” Diagonal Size
12832-	128 x 32 Pixel Resolution
UM-	Model – Includes Multi-Font Chip
Y-	Emitting Color: Yellow
3-	+3V Power Supply

Functions and Features

- **128 x 32 pixel resolution**
- **Built-in SSD1305 controller**
- **Parallel or serial MPU interface**
- **Single, low voltage power supply**
- **RoHS compliant**
- **Multi-Language Fonts built-in**

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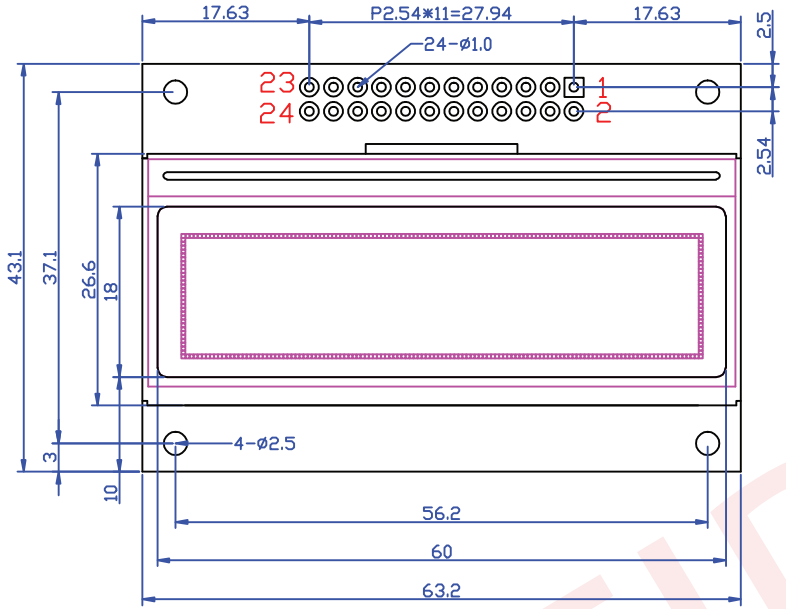
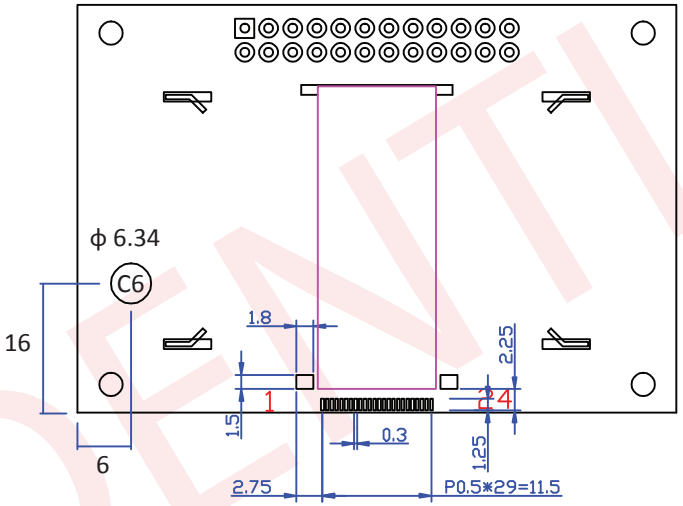
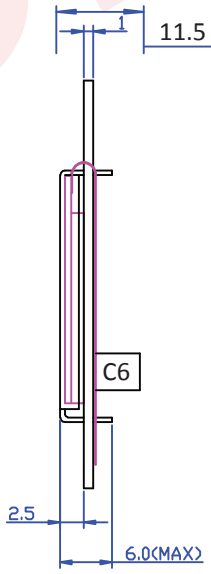
1. Document Revision History

Revision	Date	Description	Changed by
0	10/15/2012	Preliminary Release	-
1	11/5/2012	Initial Product Release	-
2	9/10/2014	Electrical Characteristics updated	ML

2. Mechanical Drawing







PIN ASSIGNMENT	
1	VSS
2	VDD
3	NC
4	D/C
5	R/W (/WR)
6	E (/RD)
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	/RES
16	/CS
17	BS2
18	BS1
19	MF_SCLK
20	MF_SI
21	/MF_CS2
22	MF_SO
23	NC
24	NC

Notes:

1. Color: Yellow
2. Controller IC: SSD1305
3. Interface: 8-bit 68xx/80xx Parallel, 4-wire SPI
4. RoHS Compliant

Rev	Description	Date

	Date	
	11/21/12	NEWHAVEN DISPLAY INTERNATIONAL
Gen. Tolerance ±0.3mm	Unit mm	Model: NHD-2.23-12832UMY3

3. Interface Description

3.1. Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	**6800-interface:** Read/Write select signal, R/W=1: Read R/W: =0: Write **8080-interface:** Active LOW Write signal.
6	E or /RD	MPU	**6800-interface:** Operation enable signal. Falling edge triggered. **8080-interface:** Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	/RES	MPU	Active LOW Reset signal.
16	/CS	MPU	Active LOW Chip Enable signal.
17	BS2	MPU	MPU Interface Select signal.
18	BS1	MPU	MPU Interface Select signal.
19	MF_SCLK	MPU	Multi-font IC Serial Clock Input
20	MF_SI	MPU	Multi-font IC Serial Data Input
21	/MF_CS2	MPU	Multi-font IC Active LOW Chip Enable signal.
22	MF_SO	MPU	Multi-font IC Serial Data Output
23	NC	-	No Connect
24	NC	-	No Connect

3.2. Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	VSS	Power Supply	Ground
15	/RES	MPU	Active LOW Reset signal.
16	/CS	MPU	Active LOW Chip Enable signal.
17	BS2	MPU	MPU Interface Select signal.
18	BS1	MPU	MPU Interface Select signal.
19	MF_SCLK	MPU	Multi-font IC Serial Clock Input
20	MF_SI	MPU	Multi-font IC Serial Data Input
21	/MF_CS2	MPU	Multi-font IC Active LOW Chip Enable signal.
22	MF_SO	MPU	Multi-font IC Serial Data Output
23	NC	-	No Connect
24	NC	-	No Connect

3.3. I^2C Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	SA0	MPU	Slave Address Selection signal.
5-6	VSS	Power Supply	Ground
7	SCL	MPU	Serial Clock signal.
8	SDA_{IN}	MPU	Serial Data input signal (pins 8 and 9 can be tied together).
9	SDA_{OUT}	MPU	Serial Data output signal (pin9 can be no connect).
10-14	VSS	Power Supply	Ground
15	/RES	MPU	Active LOW Reset signal.
16	/CS	MPU	Active LOW Chip Enable signal.
17	BS2	MPU	MPU Interface Select signal.
18	BS1	MPU	MPU Interface Select signal.
19	MF_SI	MPU	Multi-font IC Serial Data Input
20	MF_SCLK	MPU	Multi-font IC Serial Clock Input
21	/MF_CS2	MPU	Multi-font IC Active LOW Chip Enable signal.
22	MF_SO	MPU	Multi-font IC Serial Data Output
23	NC	-	No Connect
24	NC	-	No Connect

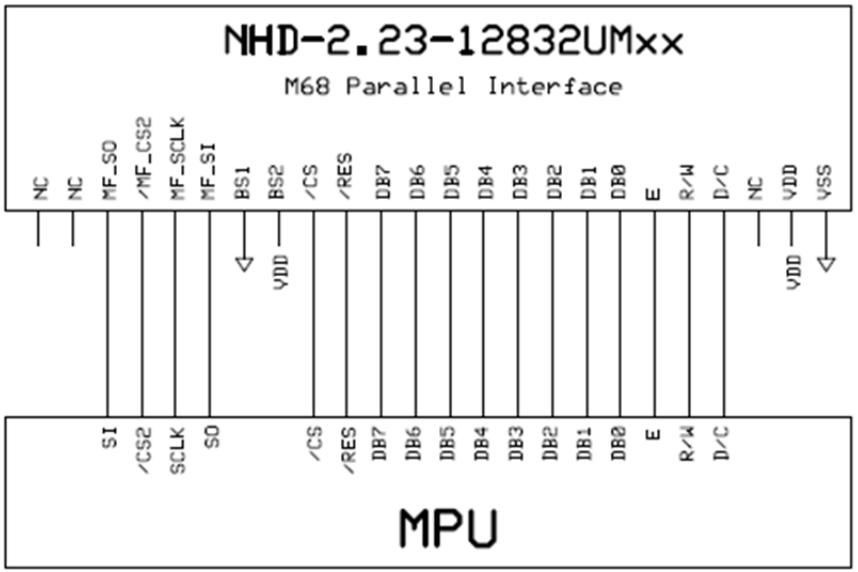
3.4. MPU Interface Pin Selections

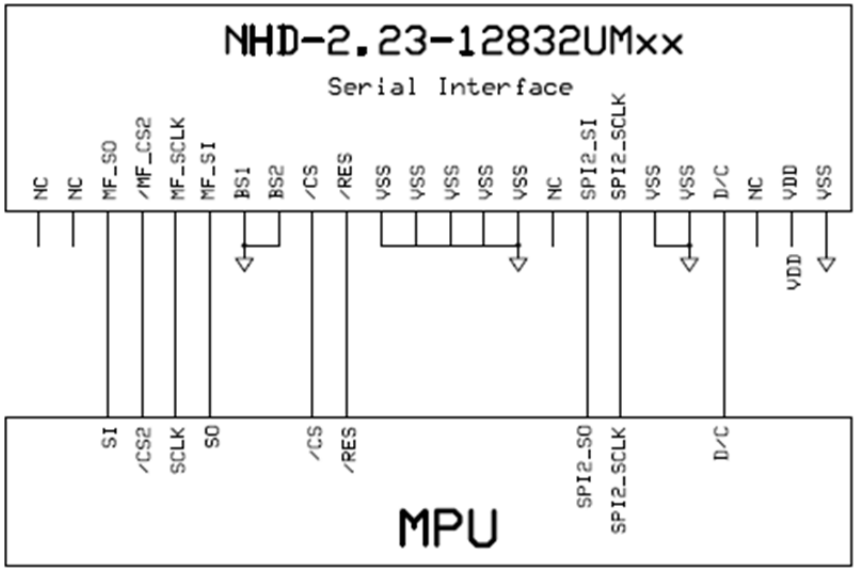
Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	Serial Interface	I2C Interface
BS2	1	1	0	0
BS1	0	1	0	1

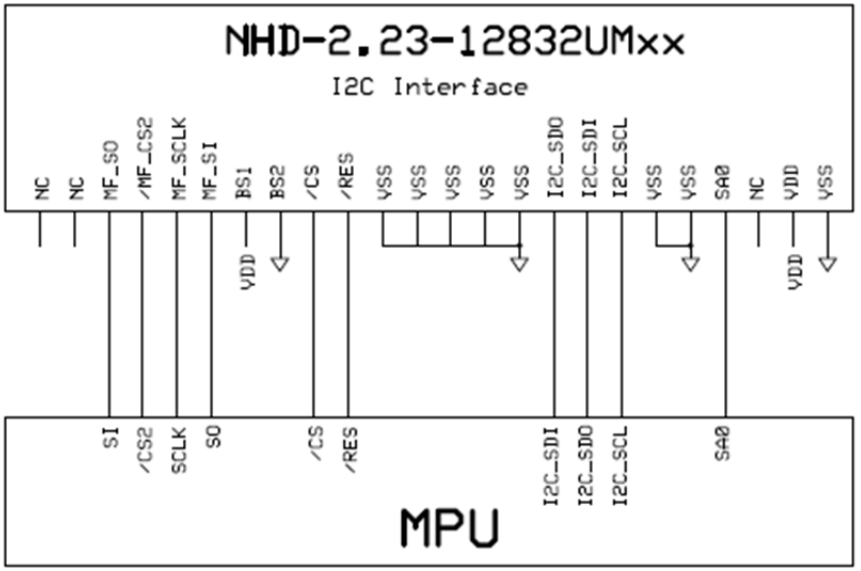
3.5. MPU Interface Pin Assignment Summary

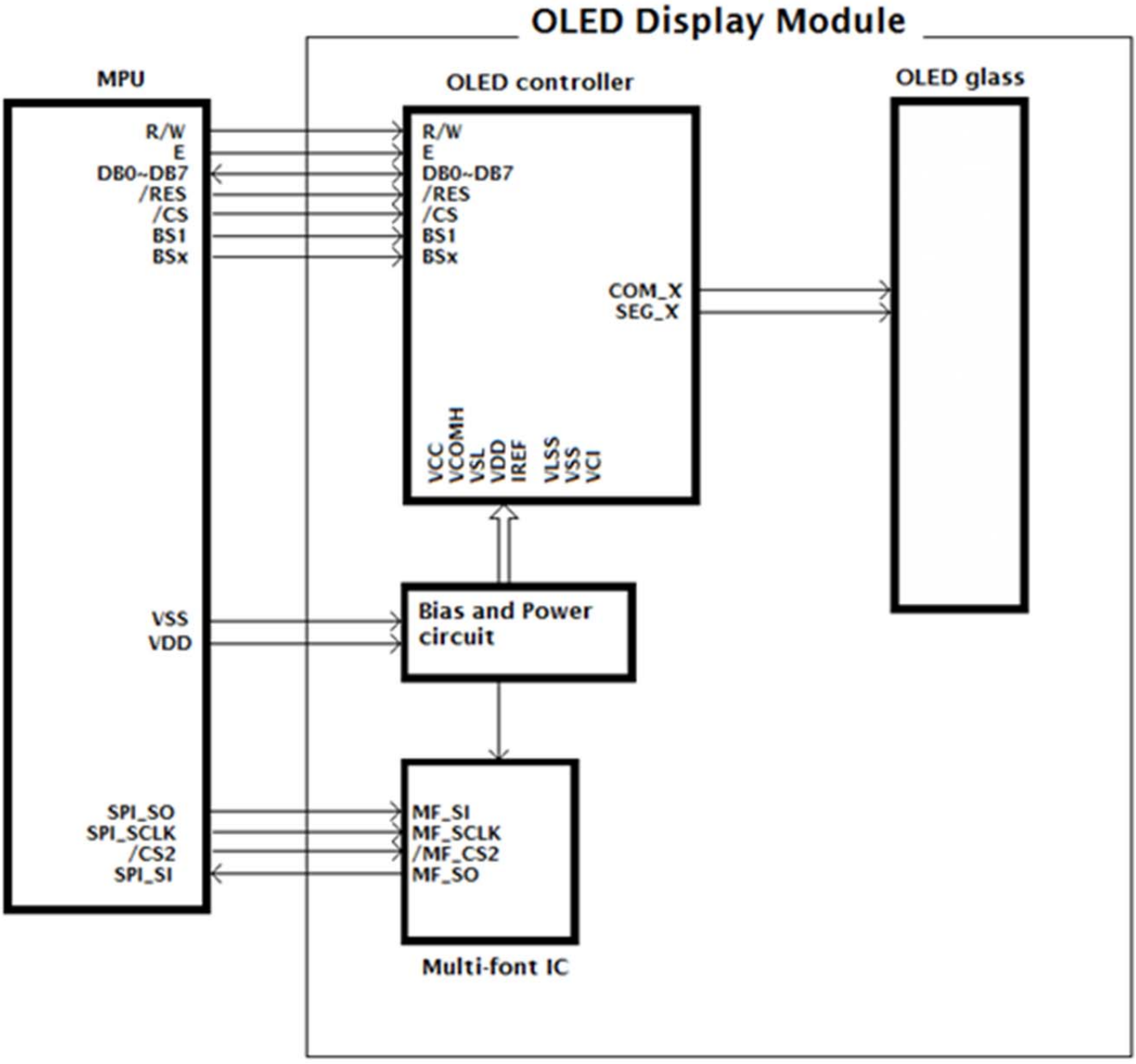
Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES
I2C	Tie LOW					SDA_{IN}	SDA_{OUT}	SCL	Tie LOW			SA0	/RES

4. Wiring Diagrams








OLED Display Module
MPU
OLED controller
OLED glass
R/W
E
DB0~DB7
/RES
/CS
BS1
BSx
R/W
E
DB0~DB7
/RES
/CS
BS1
BSx
COM_X
SEG_X
VCC
VCOMH
VSL
VDD
IREF
VLSS
VSS
VCI
VSS
VDD
Bias and Power circuit
SPI_SO
SPI_SCLK
/CS2
SPI_SI
MF_SI
MF_SCLK
/MF_CS2
MF_SO
Multi-font IC

5. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-40	-	+90	°C
Supply Voltage	VDD		-	3.3	3.5	V
Supply Current	IDD	VDD=3.3V, 50% ON	-	75	90	mA
		VDD=3.3V, 100% ON	-	123	140	mA
Sleep Mode Current	IDD_{SLEEP}		-	4	17	µA
"H" Level input	Vih		0.8*VDD	-	VDD	V
"L" Level input	Vil		VSS	-	0.2*VDD	V
"H" Level output	Voh		0.9*VDD	-	VDD	V
"L" Level output	Vol		VSS	-	0.1*VDD	V

6. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Vertical (top)	AV		80	-	-	º
Viewing Angle – Vertical (bottom)	AV		80	-	-	º
Viewing Angle – Horizontal (left)	AH		80	-	-	º
Viewing Angle – Horizontal (right)	AH		80	-	-	º
Contrast Ratio	Cr		2000:1	-	-	-
Response Time (rise)	Tr	-	-	10	-	us
Response Time (fall)	Tf	-	-	10	-	us
Brightness		50% checkerboard	100	120	-	cd/m^2
Lifetime		Ta=25°C, 50% checkerboard	40,000	-	-	Hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

7. Font Content Address Table

#	Type	Font Content	Character Set	Number of Characters	Base Address (decimal)	Base Address (hex)
1	ASCII	5x7 ASCII	ASCII	96	0	000000
2		7x8 ASCII	ASCII	96	768	000300
3		8x16 **BOLD** ASCII	ASCII	96	1,536	000600
4		Width-adjusted Arial ASCII	ASCII	96	3,072	000C00
5		8x16 Latin	Basic	96	6,336	0018C0
6		8x16 Latin	Supplement	96	7,872	001EC0
7		8x16 Latin	Extended A	128	9,408	0024C0
8		8x16 Latin	Extended B	80	11,456	002CC0
9		8x16 Latin	Extended Additional	96	12,736	0031C0
10		8x16 Greek	Basic	96	14,272	0037C0
11	UNICODE	8x16 Cyrillic	Basic	208	15,808	003DC0
12		8x16 Hebrew	Basic	112	19,136	004AC0
13		8x16 Thai	Basic	128	20,928	0051C0
14		Width-adjusted Latin	Basic	96	22,976	0059C0
15		Width-adjusted Latin	Supplement	96	26,240	006680
16		Width-adjusted Latin	Extended A	128	29,504	007340
17		Width-adjusted Latin	Extended B	80	33,856	008440
18		Width-adjusted Latin	Extended Additional	96	36,576	008EE0
19		Width-adjusted Greek	Basic	96	39,840	009BA0
20		Width-adjusted Cyrillic	Basic	208	43,104	00A860
21		Width-adjusted Arabic	Basic	576	50,176	00C400
22	CJK	GB2312		7,614	69,760	011080
23		KSC5605		6,500	379,744	05CB60
24		JIS0208		7,999	490,624	077C80
25	LCM	5x7 ISO8859		1,792	946,992	0E7330
26		LCM 5x10		1,792	961,328	0EAB30

8. Supported Languages

Language Family	Area	Country	Language
Latin (English)	Europe	United Kingdom	English
		Ireland	
	North America	USA	English
		Canada	English, French
		Belize	English
		Jamaica	
		Trinidad and Tobago	
		Bahamas	
		Antigua and Barbuda	
		Dominica	
		St. Vincent	
		St. Lucia	
		Grenada	
		St. Kitts-Nevis	
	South Africa	Guyana	English
	Australia	Australia	English
		New Zealand	
		Tonga	
		Fiji	
		Palau	
		Solomon	
		Vanuatu	
		Kiribati	
		Nauru	
		Marshall Islands	
	Africa	South Africa	English, Dutch
		Zimbabwe	English
		Gambia	
		Sierra Leone	
		Liberia	
		Ghana	
		Nigeria	
		Uganda	
		Zambia	
		Malawi	
		Seychelles	
		Mauritius	
		Botswana	
		Namibia	
		Lesotho	
Latin (Portuguese)	Europe	Portugal	Portuguese
	South America	Brazil	
	Africa	Cape Verde	
		Guinea-Bissau	
		Sao Tome and Principe	
		Angola	
		Mozambique	
Latin (German)	Europe	Germany	German
		Switzerland	German, French
		Austria	German
		Luxembourg	German, French
		Liechtenstein	German
Latin (Dutch)	Europe	Holland	Dutch
	South	Surinam	

Language Family	Area	Country	Language
Latin (French)	Europe	France	French
		Belgium	French, Dutch
		Monaco	French, Italian
	North America	Haiti	French
	Africa	Senegal	French
		Mali	
		Burkina Faso	
		Guinea	
		Cote d'Ivoire	
		Togo	
		Benin	
		Niger	
		Cameroon	
		Chad	
		Central African Republic	
		Djibouti	
		Burundi	
		Republic of Democratic Congo	
		Congo	
		Gabon	
		Comoros	
		Madagascar	
Latin (Spanish)	Europe	Spain	Spanish, Catalan
		Andorra	Spanish
	North America	Mexico	Spanish
		Guatemala	
		Costa Rica	
		Panama	
		Dominican Republic	
		El Salvador	
		Honduras	
		Nicaragua	
		Puerto Rico	
		Cuba	
	South America	Venezuela	Spanish
		Colombia	
		Peru	
		Argentina	
		Ecuador	
		Chile	
		Uruguay	
		Paraguay	
		Bolivia	
	Africa	New Guinea	Spanish
		Ceuta and Melilla	
Latin (Nordic Europe)	Europe	Denmark	Danish
		Norway	Norwegian
		Sweden	Swedish
		Faroes	Faroese
		Greenland	Greenlandic
		Iceland	Icelandic
		Finland	Finnish, Swedish
		Estonia	Estonian
		Latvia	Latvian

	America		
Latin (Central Europe)	Europe	Czech	Czech
		Slovakia	Slovak
		Poland	Polish
		Hungary	Hungarian
		Romania	Romanian
		Slovenia	Slovenian
		Croatia	Crotian
Latin (Southern Europe)	Europe	Italy	Italian
		San Marino	
		Vatican	
		Turkey	Turkish
		Malta	Maltese
		Albania	Albanian
Latin (Southeast Asia)	Asia	Vietnam	Vietnamese
		Malaysia	Malaysian
		Brunei	
		Indonesia	Indonesian
		East Timor	
		Philippines	English, Tagalog
Arabic (Africa)	Africa	Egypt	Arabic
		Tunisia	
		Libya	
		Morocco	
		Algeria	
		Sudan	
		Somalia	
		Djibouti	
		Mauritania	
Arabic (Asia)	Asia	Syria	Arabic
		United Arab Emirates	
		Lebanon	
		Yemen	
		Kuwait	
		Qatar	
		Bahrain	
		Oman	
		Jordan	
		Iraq	
		Saudi Arabia	
		Palestine	
		Iran	Farsi
		Pakistan	Urdu, Arabic
		Afghanistan	Pashto
		Lithuania	Lithuanian
Cyrillic (Eastern Europe)	Europe	Russia	Russian
		Belarus	
		Ukraine	Russian Ukrainian
		Bulgaria	Bulgarian
		Moldova	Russian
		Yugoslavia	Serbian
		Barbados	
		Macedonia	Macedonian
Cyrillic (Asia)	Asia	Azerbaijan	Azeri
		Kirghizstan	Kyrgyz
		Tajikistan	Tajik
		Turkmenistan	Turkmen
		Uzbekistan	Uzbek
		Kazakhstan	Kazakh
		Mongolia	Mongolian
Greek	Europe	Greece	Greek
		Cyprus	
Latin (Africa)	Africa	Kenya	Kiswahili
		Tanzania	
Hebrew	Asia	Israel	Hebrew
Thai	Asia	Thailand	Thai
Japan	Asia	Japan	Japanese
Korea	Asia	Korea	Korean
China	Asia	China	Chinese
		Singapore	

9. OLED controller Instruction Table (Built-In SSD1305 Controller/Driver)

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set Lower Column Start Address	0	**00~ 0F**	**0**	**0**	**0**	**0**	**X3**	**X2**	**X1**	**X0**	Set the lower nibble of the column start address register for Page Addressing Mode.	0
Set Higher Column Start Address	0	**10~1F**	**0**	**0**	**0**	**1**	**X3**	**X2**	**X1**	**X0**	Set the higher nibble of the column start address register for Page Addressing Mode.	0
Set Memory Addressing Mode	0	**20** **A[1:0]**	**0** *	**0** *	**1** *	**0** *	**0** *	**0** *	**0** **A1**	**0** **A0**	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode A[1:0] = 11b, Invalid	10b
Set Column Address	0	**21** **A[7:0]** **B[7:0]**	**0** **A7** **B7**	**0** **A6** **B6**	**1** **A5** **B5**	**0** **A4** **B4**	**0** **A3** **B3**	**0** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Setup column start and end address A[7:0]: Column start address. Range: 0-131d B[7:0]: Column end address. Range: 0-131d	 0 131d
Set Page Address	0	**22** **A[2:0]** **B[2:0]**	**0** * *	**0** * *	**1** * *	**0** * *	**0** * *	**0** **A2** **B2**	**1** **A1** **B1**	**0** **A0** **B0**	Setup page start and end address A[2:0]: Page start address. Range: 0-7d B[2:0]: Page end address. Range: 0-7d	 0 7d
Set Display Start Line	0	**40~7F**	**0**	**1**	**X5**	**X4**	**X3**	**X2**	**X1**	**X0**	Set display RAM display start line register from 0-63d.	0
Set Contrast Control	0	**81** **A[7:0]**	**1** **A7**	**0** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	 0x80
Set Brightness	0	**82** **A[7:0]**	**1** **A7**	**0** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases.	 0x80
Set Look-Up Table	0	**91** **X[5:0]** **A[5:0]** **B[5:0]** **C[5:0]**	**1** * * * *	**0** * * * *	**0** **X5** **A5** **B5** **C5**	**1** **X4** **A4** **B4** **C4**	**0** **X3** **A3** **B3** **C3**	**0** **X2** **A2** **B2** **C2**	**0** **X1** **A1** **B1** **C1**	**1** **X0** **A0** **B0** **C0**	Set current drive pulse width of Bank 0, Color A, B and C. Bank 0: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color A: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color B: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color C: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Note: Color D pulse width is fixed at 64 clocks.	 0x31 0x3F 0x3F 0x3F
Set Bank Color of Bank1 to Bank16 (Page 0)	0	**92** **A[7:0]** **B[7:0]** **C[7:0]** **D[7:0]**	**1** **A7** **B7** **C7** **D7**	**0** **A6** **B6** **C6** **D6**	**0** **A5** **B5** **C5** **D5**	**1** **A4** **B4** **C4** **D4**	**0** **A3** **B3** **C3** **D3**	**0** **A2** **B2** **C2** **D2**	**1** **A1** **B1** **C1** **D1**	**0** **A0** **B0** **C0** **D0**	Sets the bank color of Bank1~Bank16 to any one of the 4 colors A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK1. A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK2. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK15. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK16.	
Set Bank Color of Bank17 to Bank32	0	**93** **A[7:0]**	**1** **A7**	**0** **A6**	**0** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Sets the bank color of Bank17~Bank32 to any one of the 4 colors A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK17.	

(Page 1)		**B[7:0]** **C[7:0]** **D[7:0]**	**B7** **C7** **D7**	**B6** **C6** **D6**	**B5** **C5** **D5**	**B4** **C4** **D4**	**B3** **C3** **D3**	**B2** **C2** **D2**	**B1** **C1** **D1**	**B0** **C0** **D0**	A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK18. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK31. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK32.	
Set Segment Remap	0	**A0/A1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**X0**	X[0] = 0; Column address 0 is mapped to SEG0 X[0] = 1; Column address 131 is mapped to SEG0	0
Entire Display ON	0	**A4/A5**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**X0**	X[0] = 0; Resume RAM content display. Output follows RAM content. X[0] = 1; Entire display ON. Output ignores RAM content.	0
Set Normal/ Inverse Display	0	**A6/A7**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**X0**	X[0] = 0; Normal display. X[0] = 1; Inverse display.	0
Set Multiplex Ratio	0	**A8** **A[5:0]**	**1** *****	**0** *****	**1** **A5**	**0** **A4**	**1** **A3**	**0** **A2**	**0** **A1**	**0** **A0**	Set MUX ratio to N+1 MUX N=A[5:0]; from 16MUX to 64MUX (0 to 14 are invalid)	64
Dim mode setting	0	**AB** **A[3:0]** **B[7:0]** **C[7:0]**	**1** ***** **B7** **C7**	**0** ***** **B6** **C6**	**1** ***** **B5** **C5**	**0** ***** **B4** **C4**	**1** **A3** **B3** **C3**	**0** **A2** **B2** **C2**	**1** **A1** **B1** **C1**	**1** **A0** **B0** **C0**	A[3:0] = reserved. Set as 0000b B[7:0] = Set contrast for BANK0. Range 0-255d. Refer to command 81h. C[7:0] = Set brightness for color bank. Range 0-255d. Refer to command 82h.	
Master configuration	0	**AD** **AE**	**1** **1**	**0** **0**	**1** **0**	**0** **0**	**1** **1**	**1** **1**	**0** **1**	**1** **0**	Selects external VCC supply	AEh
Set Display ON/ OFF	0	**AC/** **AE/** **AF**	**1**	**0**	**1**	**0**	**1**	**1**	**A1**	**A0**	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) AFh = Display ON in normal mode	AEh
Set Page Start Address	0	**B0~B7**	**1**	**0**	**1**	**1**	**0**	**X2**	**X1**	**X0**	Set GDRAM Page Start Address for Page Addressing Mode using X[2:0]. PAGE0~PAGE7	
Set COM Output Scan Direction	0	**C0/C8**	**1**	**1**	**0**	**0**	**X3**	**0**	**0**	**0**	X[3] = 0; Normal mode. Scan from COM0 to COM[N-1] X[3] = 1; Remapped mode. Scan from COM[N-1] to COM0	0
Set Display Offset	0	**D3** **A[5:0]**	**1** *****	**1** *****	**0** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Set vertical shift by COM from 0~63.	0
Set Display Clock Divide Ratio / Oscillator Frequency	0	**D5** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**1** **A4**	**0** **A3**	**1** **A2**	**0** **A1**	**1** **A0**	A[3:0] = Define the divide ratio of the display clocks. Divide ratio = A[3:0] +1 A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0000b 0111b
Set Area Color Mode ON/OFF & Low Power Display Mode	0	**D8** **X[5:0]**	**1** **0**	**1** **0**	**0** **X5**	**1** **X4**	**1** **0**	**0** **X2**	**0** **0**	**0** **X0**	X[5:4] = 00b; Monochrome mode X[5:4] = 11b; Area Color mode X[2] = 0 and X[0] = 0; Normal power mode X[2] = 1 and X[0] = 1; Set low power display mode	00 00
Set Pre-charge Period	0	**D9** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**1** **A4**	**1** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	A[3:0] = Phase 1 period of up to 15 DCLK clocks. 0 is invalid. A[7:4] = Phase 2 period of up to 15 DCLK clocks. 0 is invalid.	2h 2h
Set COM pins	0	**DA**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	X[4] = 0; Sequential COM pin configuration	

Hardware configuration		**X[5:4]**	**0**	**0**	**X5**	**X4**	**0**	**0**	**1**	**0**	X[4] = 1; Alternative COM pin configuration X[5] = 0; Disable COM Left/Right remap X[5] = 1; Enable COM Left/Right remap	1 1
Set VCOMH Deselect Level	0	**DB** **A[5:2]**	**1** **0**	**1** **0**	**0** **A5**	**1** **A4**	**1** **A3**	**0** **A2**	**1** **0**	**1** **0**	A[5:2] = 0000b; VCOMH = ~0.43*VCC A[5:2] = 1101b; VCOMH = ~0.77*VCC A[5:2] = 1111b; VCOMH = ~0.83*VCC	 1101
Enter Read Modify Write mode	0	**E0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	Enter the Read/Modify/Write mode.	
NOP	0	**E3**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	Command for No Operation	
Exit Read Modify Write mode	0	**EE**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	Exit the Read/Modify/Write mode.	

For detailed instruction information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

10. OLED Controller -> MPU Interface

For detailed timing information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

10.1. 6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.
A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

10.2. 8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.
A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

10.3. Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.
D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	0	0	0	0	↑
Write Data	0	0	0	1	↑

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,…D0.
D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.
Note: Read is not available in serial mode.

10.4. I^2C Interface

The I2C interface consists of a slave address bit SA0, I2C-bus data signal SDA, and I2C-bus clock signal SCL. D1 and D2 can be tied together, and act as SDA. D0 acts as SCL. Both the data and clock signals must be connected to pull-up resistors. /RES is used to initialize the device.
Note: SA0 bit allows the device to have a slave address of either “0111100” or “0111101”.
Note: Data and acknowledgement are sent through the SDA. The ITO track resistance and the pull-up resistance at SDA becomes a voltage potential divider. As a result, it may not be possible to attain a valid logic “0” level on SDA for the ACK signal. SDA_{IN} must be connected, but SDA_{OUT} may be disconnected and the ACK signal will be ignored on the I2C bus.

For detailed protocol information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

11. Example Initialization Sequence:

```
Set_Display_On_Off(0x00);          // Display Off (0x00/0x01)
Set_Display_Clock(0x10);           // Set Clock as 160 Frames/Sec
Set_Multiplex_Ratio(0x1F);         // 1/32 Duty (0x0F~0x3F)
Set_Display_Offset(0x00);          // Shift Mapping RAM Counter (0x00~0x3F)
Set_Start_Line(0x00);              // Set Mapping RAM Display Start Line (0x00~0x3F)
Set_Master_Config(0x00);           // Disable Embedded DC/DC Converter (0x00/0x01)
Set_Area_Color(0x05);              // Set Monochrome & Low Power Save Mode
Set_Addressing_Mode(0x02);         // Set Page Addressing Mode (0x00/0x01/0x02)
Set_Segment_Remap(0x01);           // Set SEG/Column Mapping (0x00/0x01)
Set_Common_Remap(0x08);            // Set COM/Row Scan Direction (0x00/0x08)
Set_Common_Config(0x10);           // Set Alternative Configuration (0x00/0x10)
Set_LUT(0x3F,0x3F,0x3F,0x3F);      // Define All Banks Pulse Width as 64 Clocks
Set_Contrast_Control(Brightness);  // Set SEG Output Current
Set_Area_Brightness(Brightness);   // Set Brightness for Area Color Banks
Set_Precharge_Period(0xD2);        // Set Pre-Charge as 13 Clocks & Discharge as 2 Clock
Set_VCOMH(0x08);                   // Set VCOM Deselect Level
Set_Entire_Display(0x00);          // Disable Entire Display On (0x00/0x01)
Set_Inverse_Display(0x00);         // Disable Inverse Display On (0x00/0x01)
Fill_RAM(0x00);                    // Clear Screen
Set_Display_On_Off(0x01);          // Display On (0x00/0x01)
```

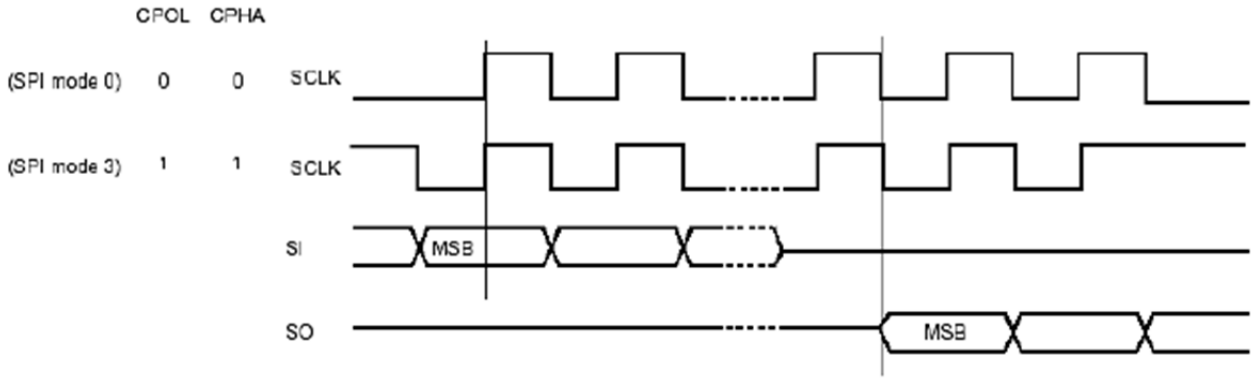
12. Multi-Font IC -> MPU Interface

12.1. Serial Interface

The serial interface consists of serial clock MF_SCLK, serial data in MF_SI, serial data out MF_SO, chip enable /MF_CS2.

Function	MF_SCLK	MF_SI	MF_SO	/MF_CS2
Send Font Address	↑	DATA	X	0
Read Font Data	↓	X	DATA	0

The Multi-Font device is enabled by a high-to-low transition on /MF_CS2. /MF_CS2 must remain LOW for the duration of any command-in or data-out sequence.
The Font Address is shifted in on the MF_SI line on the rising edge of MF_SCLK.
The Font Data is shifted out on the MF_SO line on the falling edge of MF_SCLK.

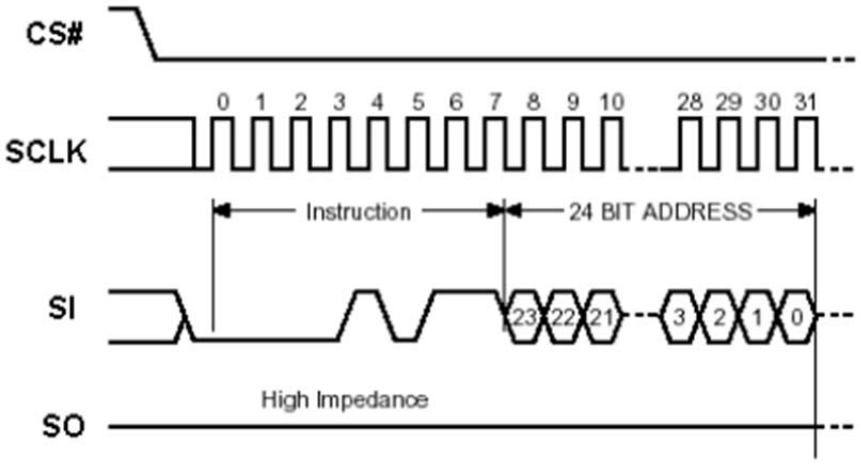


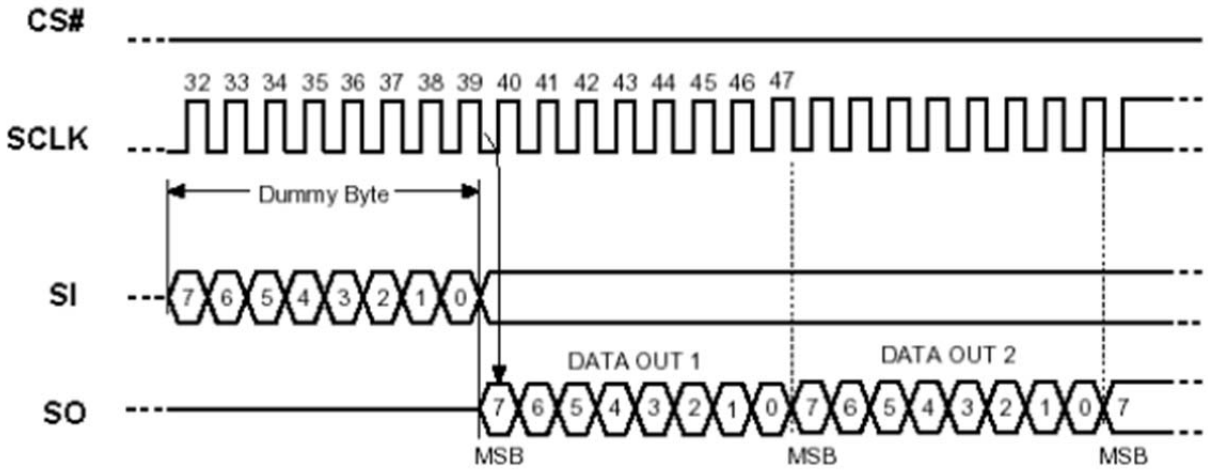
12.2. Communication Protocol

Font data can be accessed and read by using the READ command instruction.

Instruction	Description	Instruction Code	Address Bytes	Dummy Bytes	Data Bytes
READ	Read Data (30MHz MAX)	0Bh	3	1	1 ~ ∞

READ mode supports up to 30MHz frequency on MF_SCLK.
READ mode outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on /MF_CS2. The internal address pointer will automatically increment after each byte is read.
READ instruction is initiated by executing an 8-bit command [0x0B] on the MF_SI line, followed by the desired font address bits [A23-A0], and followed by an 8-bit dummy write [0x00]. The font data will then be output on MF_SO line, MSB first.
/MF_CS2 must remain active LOW for the duration of the read cycle.





12.3. Timing Characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
Fc	Clock Frequency		-	30	MHz
tCH	Clock High Time		15	-	ns
tCL	Clock Low Time		15	-	ns
tCLCH	Clock Rise Time	peak to peak	0.1	-	V/ns
tCHCL	Clock Fall Time	peak to peak	0.1	-	V/ns
tSLCH	/MF_CS2 Active Setup Time	relative to MF_SCLK	5	-	ns
tCHSL	/MF_CS2 Not Active Hold Time	relative to MF_SCLK	5	-	ns
tDVCH	Data IN Setup Time		2	-	ns
tCHDX	Data IN Hold Time		5	-	ns
tCHSH	/MF_CS2 Active Hold Time	relative to MF_SCLK	5	-	ns
tSHCH	/MF_CS2 Not Active Setup Time	relative to MF_SCLK	5	-	ns
tSHSL	/MF_CS2 Deselect Time		100	-	ns
tSHQZ	Output Disable Time		-	9	ns
tCLQV	Clock Low to Output Valid		-	9	ns
tCLQX	Output Hold Time		0	-	ns

13. Font Tables

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

14. Font Data Arrangement

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

15. Calculation of Font Addresses

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

16. Multi-Font program code example

17. Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C , 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+70°C 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-20°C , 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value

Precautions for using OLEDs/LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms