

3.3V CMOS 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

FEATURES:

- Typical tsk(o) (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µ W typ. static)
- · All inputs, outputs, and I/O are 5V tolerant
- Available in TSSOP package

DRIVE FEATURES:

- Balanced Output Drivers: ±12mA
- · Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- · Data communication and telecommunication systems

DESCRIPTION:

The LVCH162373A 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The LVCH162373A can be used for implementing memory address latches, I/O ports, and bus drivers. The output enable and latch enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

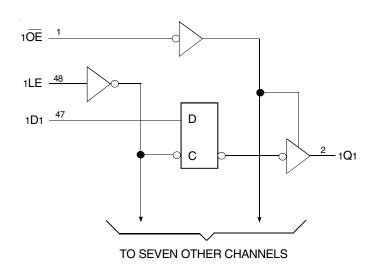
IDT74LVCH162373A

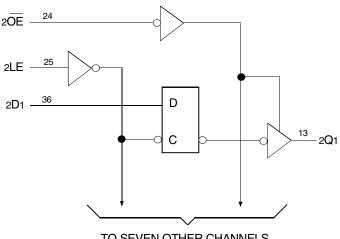
All pins of the LVCH162373A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH162373A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been developed to drive ±12mA at the designated threshold levels.

The LVCH162373A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



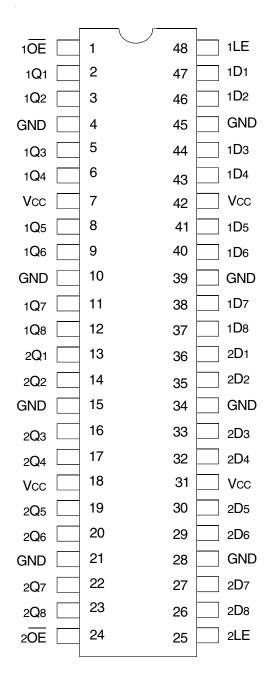


TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

OCTOBER 2015

PIN CONFIGURATION



TSSOP TOP VIEW

INDUSTRIAL TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
Tstg	Storage Temperature	–65 to +150	°C
Ιουτ	DC Output Current	–50 to +50	mA
Ік Іок	Continuous Clamp Current, Vı < 0 or Vo < 0	-50	mA
lcc Iss	Continuous Current through each Vcc or GND	±100	mA

NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
Соит	Output Capacitance	Vout = 0V	6.5	8	pF
CI/O	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs ⁽¹⁾
xLE	Latch Enable Inputs (Active HIGH)
xQx	3-State Outputs
xŌĒ	Output Enable Inputs (Active LOW)

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH 8-BIT SECTION)(1)

Inputs			Outputs
xOE	xLE	xDx	xQx
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ⁽²⁾
Н	Х	Х	Z

NOTES:

1. H = HIGH Voltage Level

X = Don't Care

L = LOW Voltage Level

Z = High-Impedance

2. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: Operating Condition: TA = -40 °C to +85 °C

Symbol	Parameter	Test Co	nditions	Min.	Typ. ⁽¹⁾	Max.	Unit
Vih	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	_	_	V
		Vcc = 2.7V to 3.6V		2	-	_	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		_	_	0.7	V
		Vcc = 2.7V to 3.6V		_	_	0.8	
Ін	Input Leakage Current	Vcc = 3.6V	VI = 0 to 5.5V		-	±5	μA
lı∟							
lozн	High Impedance Output Current	Vcc = 3.6V	Vo = 0 to 5.5V	-	-	±10	μA
Iozl	(3-State Output pins)						
loff	Input/Output Power Off Leakage	Vcc = 0V, VIN or Vo ≤ 5.5 V		_	-	±50	μA
Vik	Clamp Diode Voltage	Vcc = 2.3V, IIN = -18mA		-	-0.7	-1.2	V
Vн	Input Hysteresis	Vcc = 3.3V		_	100	_	mV
ICCL	Quiescent Power Supply Current	Vcc = 3.6V	VIN = GND or VCC	-	-	10	μA
Іссн Іссz			$3.6 \le VIN \le 5.5V^{(2)}$			10	
Δlcc	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other i	nputs at Vcc or GND	-	-	500	μA

NOTES:

1. Typical values are at Vcc = 3.3V, +25°C ambient.

2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
Івнн	Bus-Hold Input Sustain Current	Vcc = 3V	VI = 2V	-75	—	_	μA
IBHL			VI = 0.8V	75	_	—	
Івнн	Bus-Hold Input Sustain Current	Vcc = 2.3V	VI = 1.7V	_	_	_	μA
IBHL			VI = 0.7V	_	_	_	
Івнно	Bus-Hold Input Overdrive Current	Vcc = 3.6V	Vi = 0 to 3.6V	_	_	±500	μA
Ibhlo							

NOTES:

1. Pins with Bus-Hold are identified in the pin description.

2. Typical values are at Vcc = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	TestCon	ditions ⁽¹⁾	Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = 2.3V to 3.6V	Іон = - 0.1mA	Vcc-0.2	_	V
		Vcc = 2.3V	Iон = - 4mA	1.9	_	
			Iон = - 6mA	1.7	_	
		Vcc = 2.7V	Iон = - 4mA	2.2	_	
			Iон = - 8mA	2	_	
		Vcc = 3V	Iон = – 6mA	2.4	_	
			Iон = – 12mA	2	_	
Vol	Output LOW Voltage	Vcc = 2.3V to 3.6V	IOL = 0.1mA	_	0.2	V
		Vcc = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	_	0.55	
		Vcc = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	_	0.6	
		Vcc = 3V	IOL = 6mA	_	0.55	
			IOL = 12mA	_	0.8	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. TA = − 40°C to + 85°C.

OPERATING CHARACTERISTICS, Vcc = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
Cpd	Power Dissipation Capacitance per Latch Outputs enabled	CL = 0pF, f = 10Mhz	_	pF
Cpd	Power Dissipation Capacitance per Latch Outputs disabled		—	

SWITCHING CHARACTERISTICS⁽¹⁾

		Vcc =	2.7V	Vcc = 3.3	V ± 0.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tPLH	Propagation Delay	-	6	1.6	5.3	ns
t PHL	xDx to xQx					
tPLH	Propagation Delay	_	6.4	2.1	5.7	ns
t PHL	xLE to xQx					
tрzн	Output Enable Time	-	7.1	1.3	6.1	ns
tPZL	xOE to xQx					
tPHZ	Output Disable Time	-	7.7	2.5	7.3	ns
tPLZ	xOE to xQx					
ts∪	Set-up Time HIGH or LOW, xDx to xLE	2.3	_	2.3	_	ns
ťH	Hold Time HIGH or LOW, xDx after xLE	1.6	_	1.6	_	ns
tw	xLE Pulse Width HIGH	3.3	_	3.3	_	ns
tsk(o)	Output Skew ⁽²⁾	-	—	—	500	ps

NOTES:

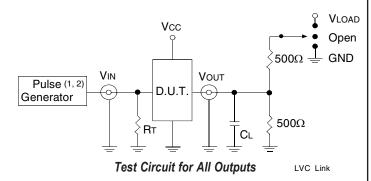
1. See TEST CIRCUITS AND WAVEFORMS. TA = -40° C to + 85° C.

2. Skew between any two outputs of the same package and switching in the same direction.

IDT74LVCH162373A 3.3VCMOS16-BITTRANSPARENTD-TYPE LATCH

TEST CIRCUITS AND WAVEFORMS TEST CONDITIONS

Symbol	Vcc ⁽¹⁾ =3.3V±0.3V	Vcc ⁽¹⁾ =2.7V	Vcc ⁽²⁾ =2.5V±0.2V	Unit
VLOAD	6	6	2 x Vcc	V
Vih	2.7	2.7	Vcc	V
Vτ	1.5	1.5	Vcc/2	V
Vlz	300	300	150	mV
VHZ	300	300	150	mV
CL	50	50	30	pF



DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

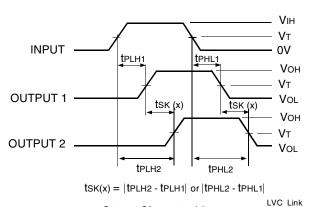
 $\mathsf{R} \tau$ = Termination resistance: should be equal to $\mathsf{Z} \mathsf{O} \mathsf{U} \tau$ of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate \leq 10MHz; tF \leq 2.5ns; tR \leq 2.5ns. 2. Pulse Generator for All Pulses: Rate \leq 10MHz; tF \leq 2ns; tR \leq 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Vload
Disable High Enable High	GND
All Other Tests	Open

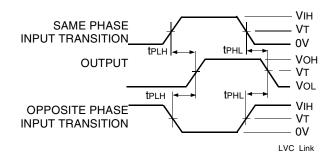


Output Skew - tsk(x)

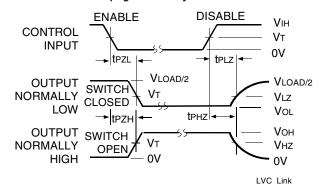
NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.

2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



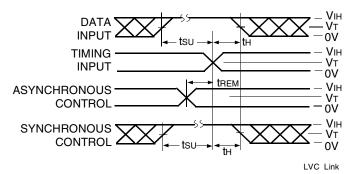
Propagation Delay

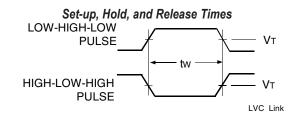


Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



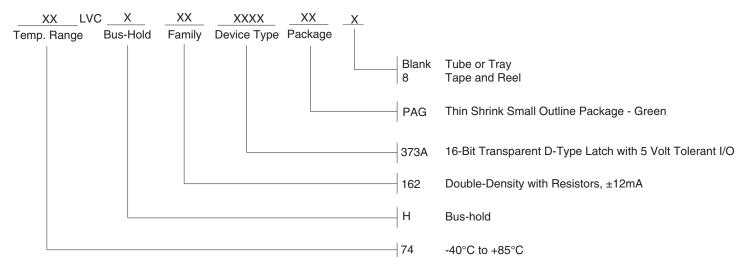


Pulse Width

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INDUSTRIAL TEMPERATURE RANGE

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

10/06/2015 Pg. 1, 2, 6 Updated the ordering information by removing non RoHS parts and adding Tape and Reel information.

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