

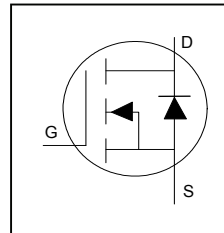
Application

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters

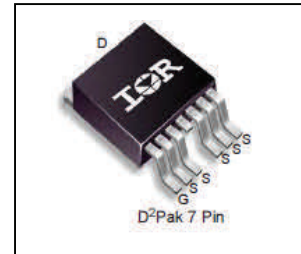
Benefits

- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche SOA
- Enhanced body diode dV/dt and dI/dt capability
- Lead-free, RoHS compliant

HEXFET® Power MOSFET



V_{DS}	75V
$R_{DS(on)}$ typ.	1.70mΩ
max	2.00mΩ
I_D (Silicon Limited)	269A①
I_D (Package Limited)	240A



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRFS7730-7PPbF	D2Pak-7PIN	Tube	50	IRFS7730-7PPbF
		Tape and Reel Left	800	IRFS7730TRL7PP

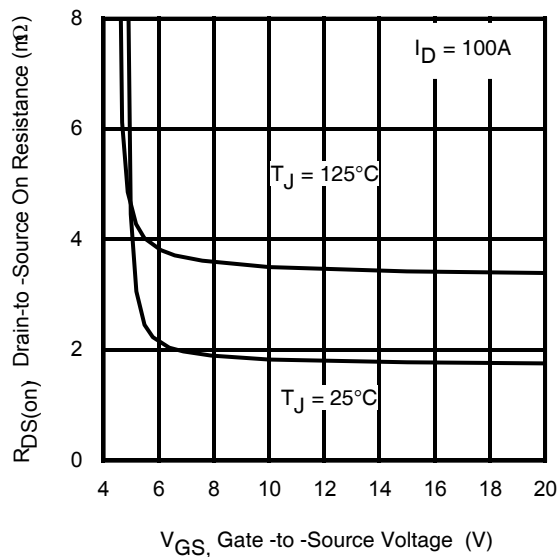


Fig 1. Typical On-Resistance vs. Gate Voltage

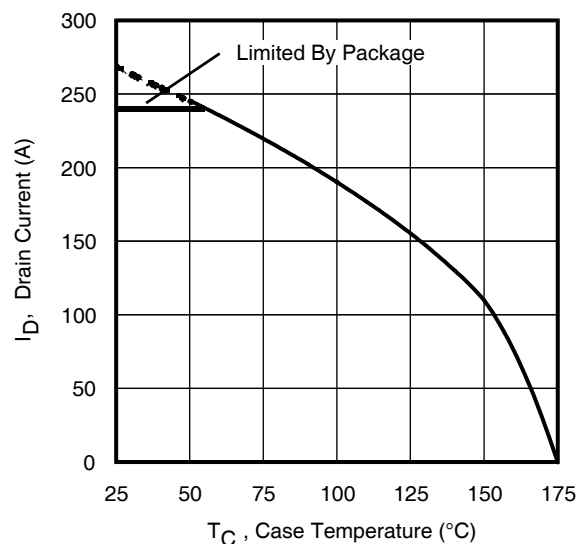


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	269①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	190	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	240	
I_{DM}	Pulsed Drain Current ②	990	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Max.	Units
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	464	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ⑨	897	
I_{AR}	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑩	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	40	—	mV/°C	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.70	2.00	mΩ	$V_{GS} = 10\text{V}$, $I_D = 100\text{A}$
		—	2.20	—	mΩ	$V_{GS} = 6.0\text{V}$, $I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150	μA	$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	1.9	—	Ω	

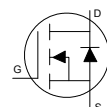
Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 93\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.
- ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1575\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_{θ} is measured at T_J approximately 90°C .
- ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 42\text{A}$, $V_{GS} = 10\text{V}$.
- ⑩ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994. please refer to application note to AN-994:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	223	—	—	S	$V_{DS} = 10\text{V}$, $I_D = 100\text{A}$
Q_g	Total Gate Charge	—	285	428	nC	$I_D = 100\text{A}$ $V_{DS} = 38\text{V}$ $V_{GS} = 10\text{V}$
Q_{gs}	Gate-to-Source Charge	—	62	—		
Q_{gd}	Gate-to-Drain Charge	—	86	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	199	—		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	$V_{DD} = 38\text{V}$ $I_D = 100\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
t_r	Rise Time	—	90	—		
$t_{d(off)}$	Turn-Off Delay Time	—	182	—		
t_f	Fall Time	—	91	—		
C_{iss}	Input Capacitance	—	13970	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	1135	—		$V_{DS} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	720	—		$f = 1.0\text{MHz}$
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	1048	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 60V ⑦
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	1283	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 60V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	269 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	990		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ⑤
dv/dt	Peak Diode Recovery dv/dt	—	11	—	V/ns	$T_J = 175^\circ\text{C}$, $I_S = 100\text{A}$, $V_{DS} = 75\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	42	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 64\text{V}$
		—	49	—		$T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$,
Q_{rr}	Reverse Recovery Charge	—	63	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤
		—	88	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.4	—	A	$T_J = 25^\circ\text{C}$

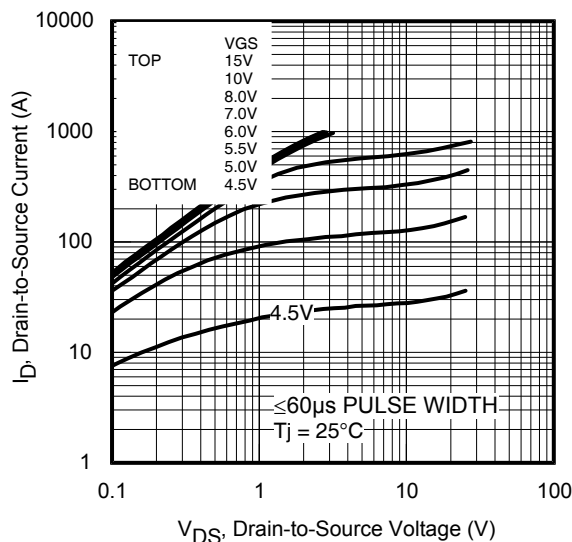


Fig 3. Typical Output Characteristics

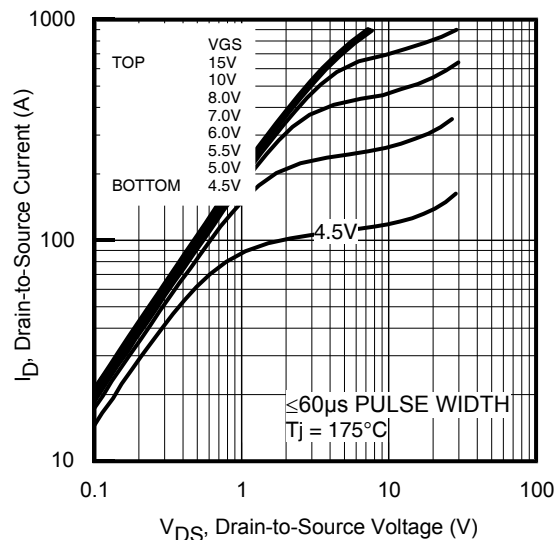


Fig 4. Typical Output Characteristics

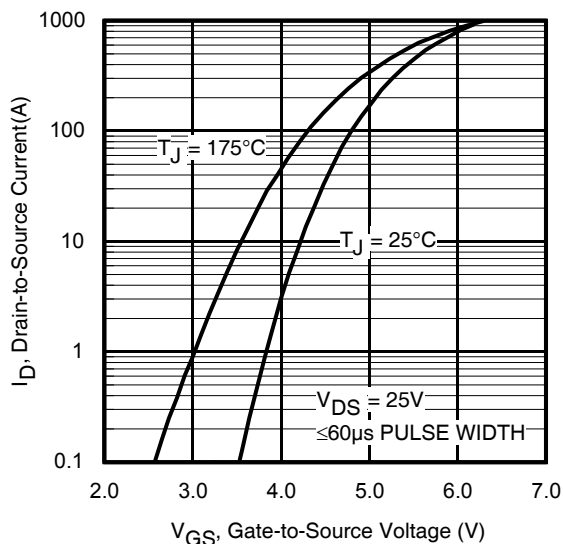


Fig 5. Typical Transfer Characteristics

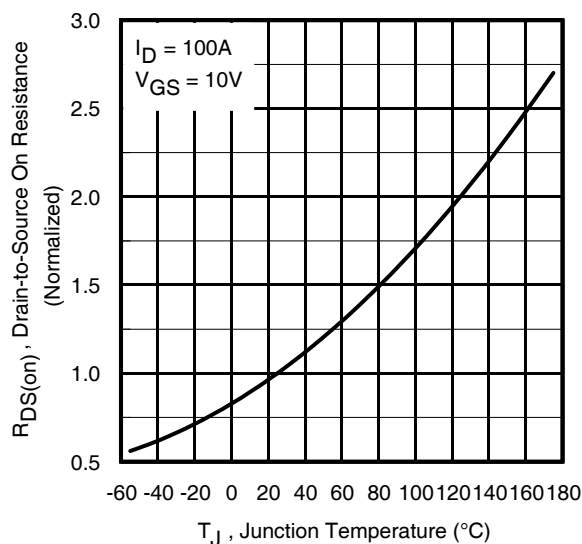


Fig 6. Normalized On-Resistance vs. Temperature

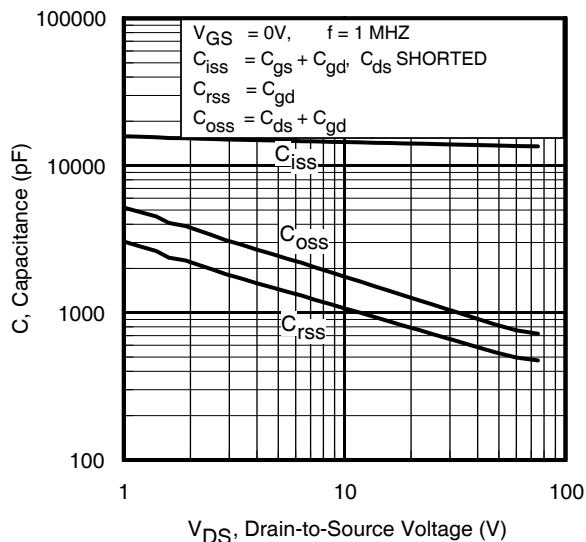


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

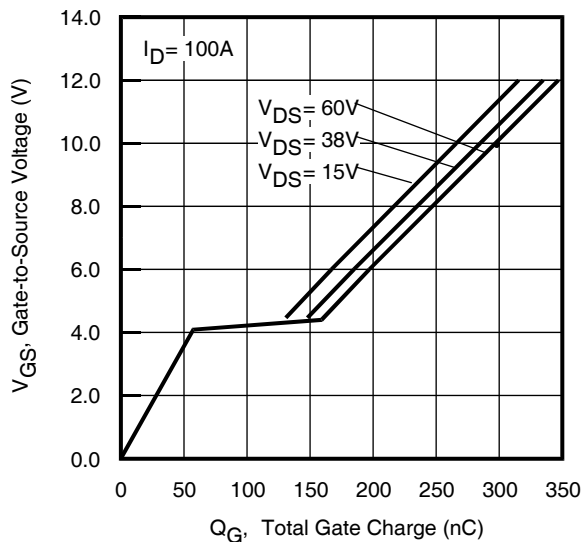
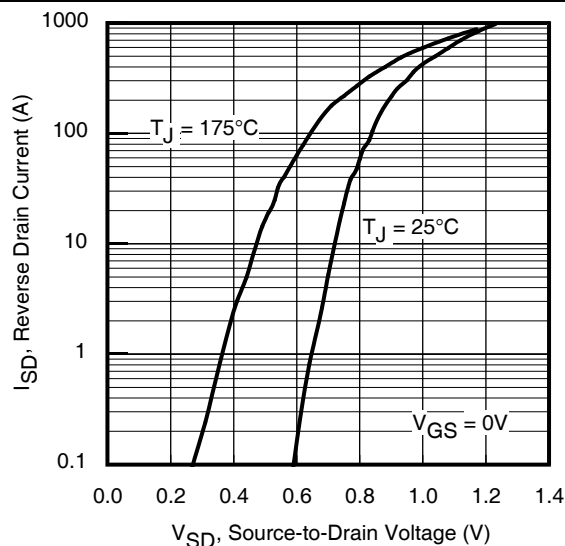
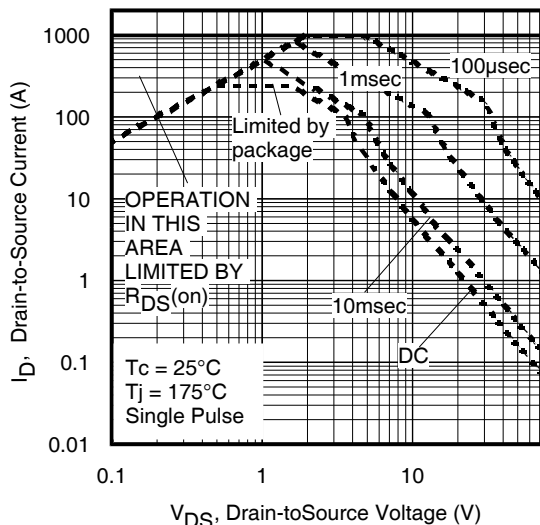
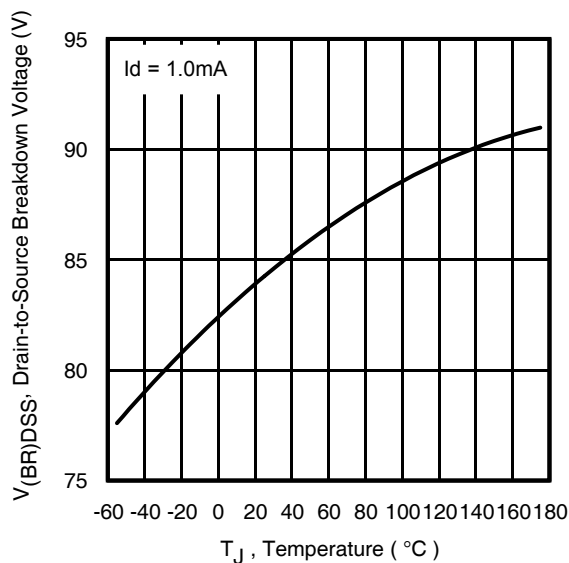
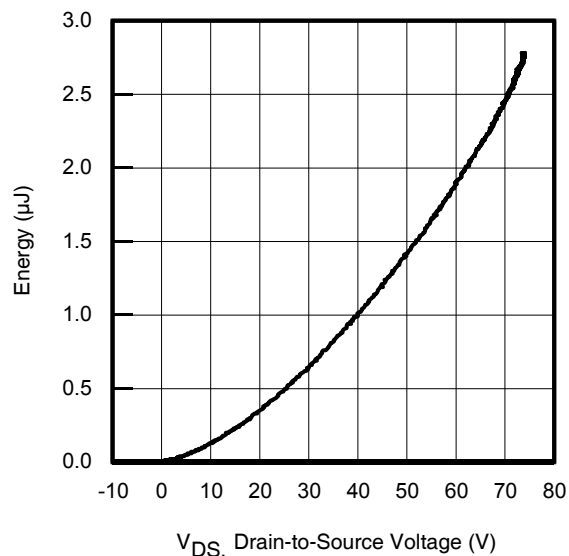
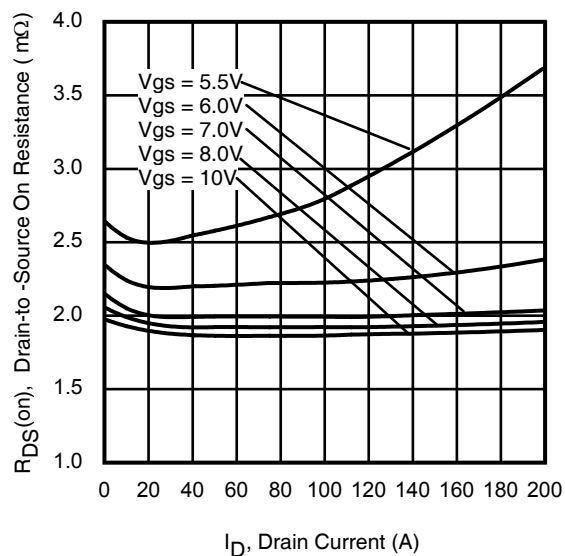


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 10. Maximum Safe Operating Area

Fig 11. Drain-to-Source Breakdown Voltage

Fig 12. Typical C_{oss} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current

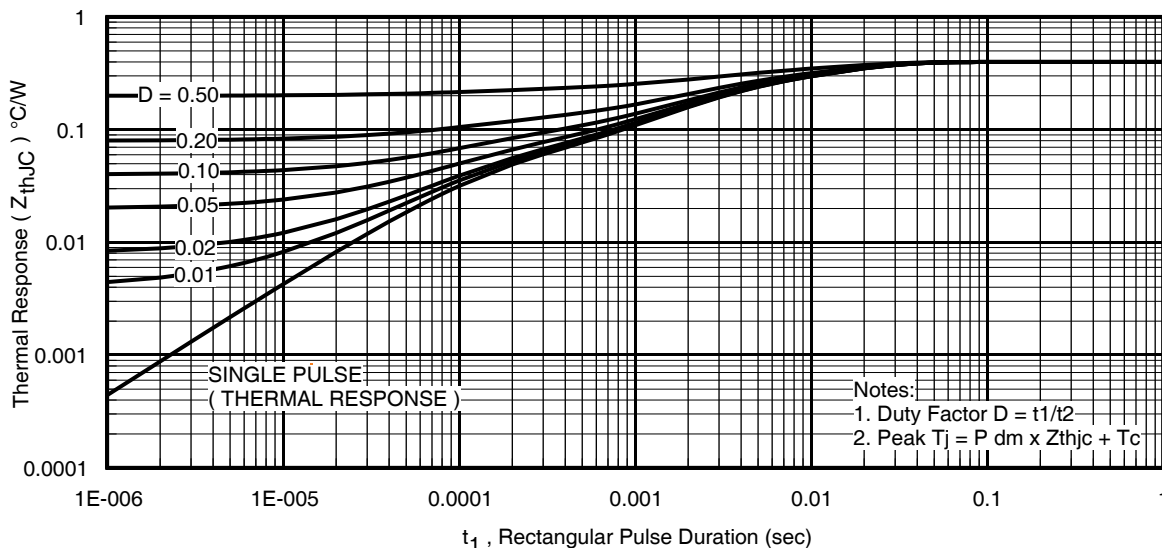


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

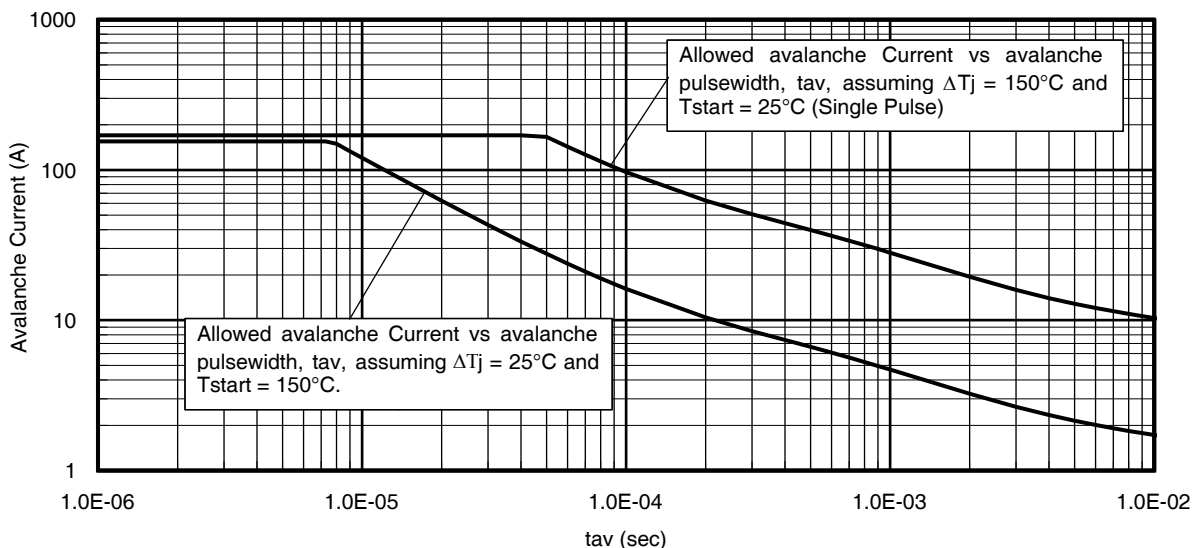


Fig 15. Avalanche Current vs. Pulse Width

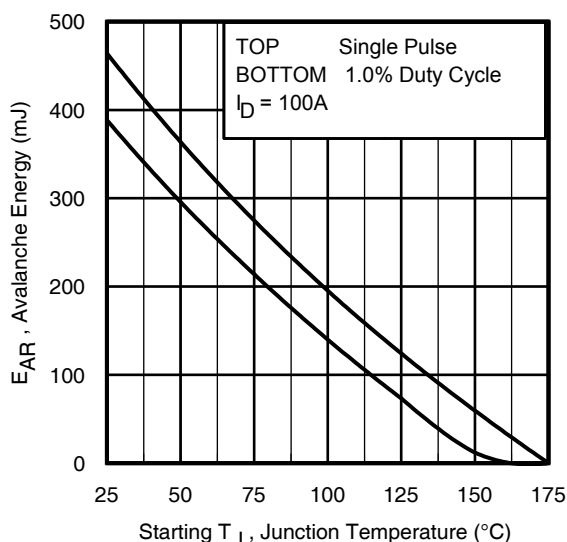
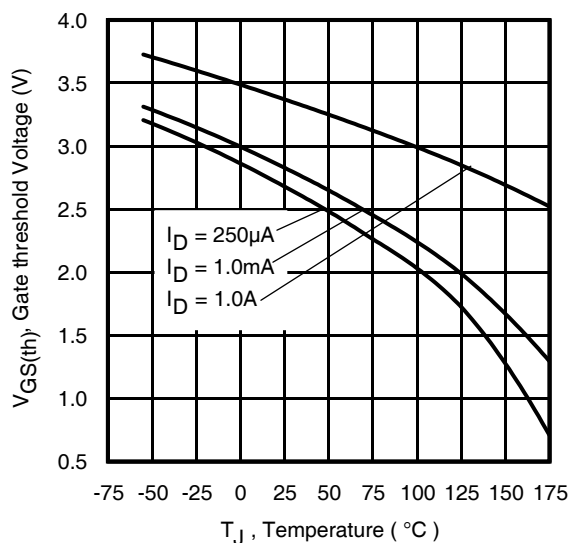
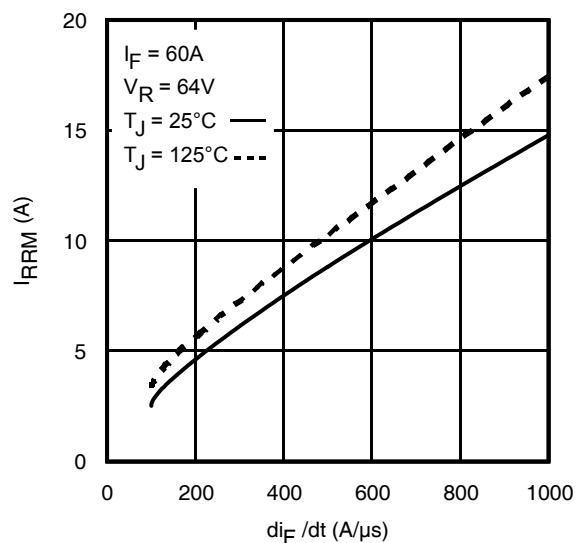
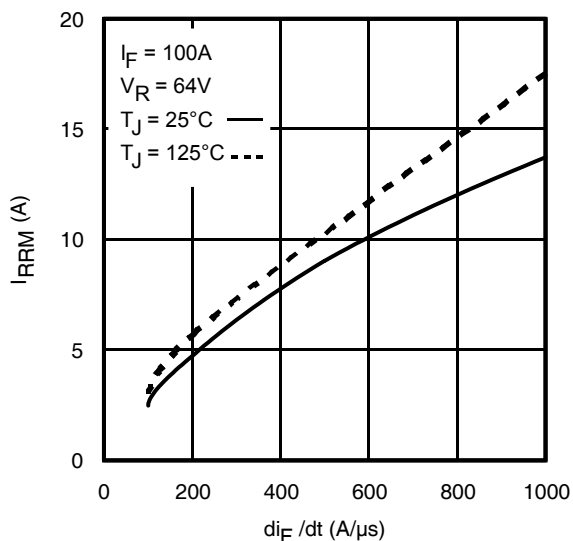
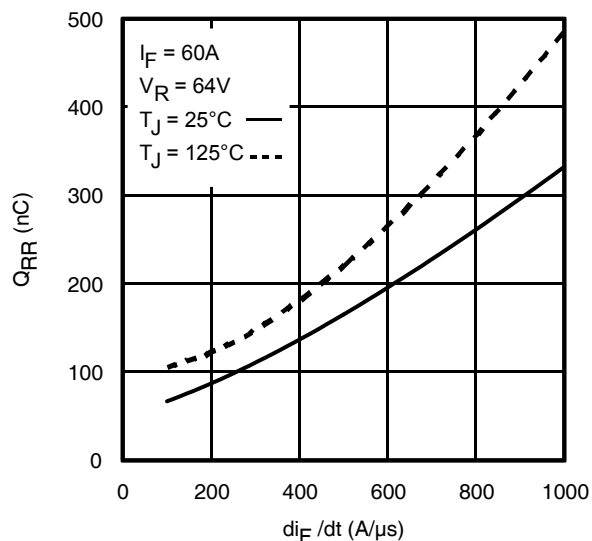
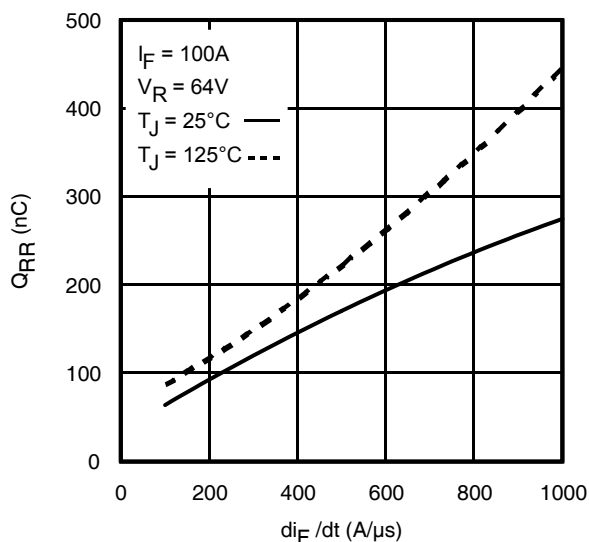


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Recovery Current vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt

Fig 21. Typical Stored Charge vs. di_F/dt

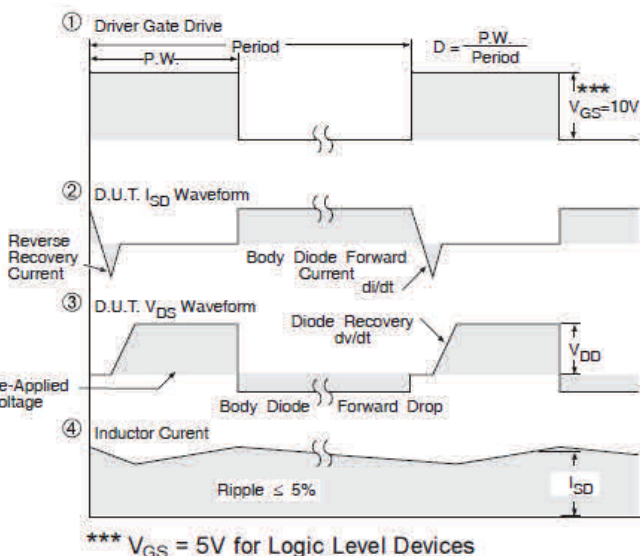
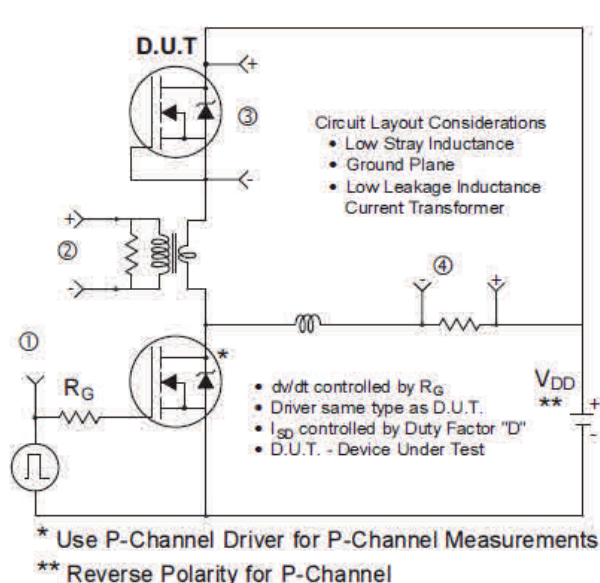


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

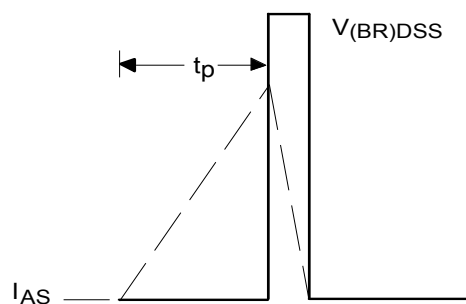
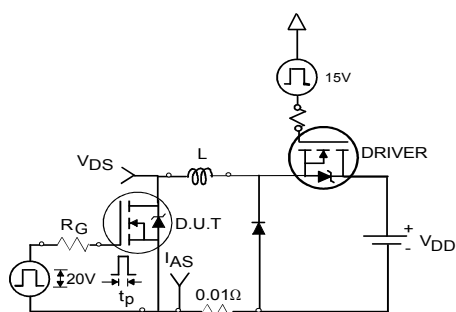


Fig 23a. Unclamped Inductive Test Circuit

Fig 23b. Unclamped Inductive Waveforms

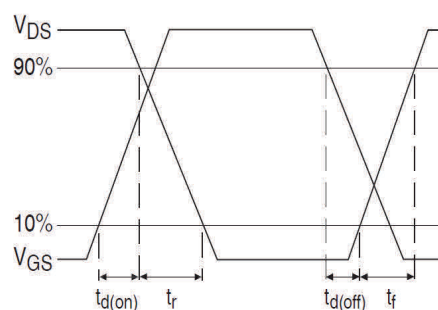
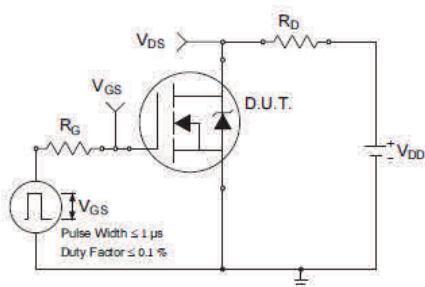


Fig 24a. Switching Time Test Circuit

Fig 24b. Switching Time Waveforms

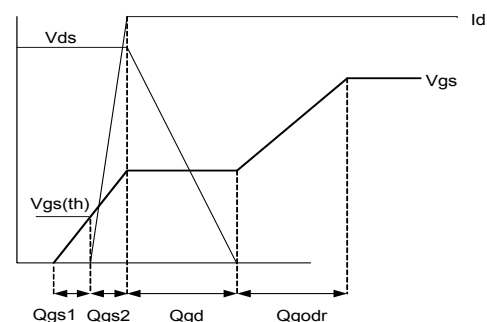
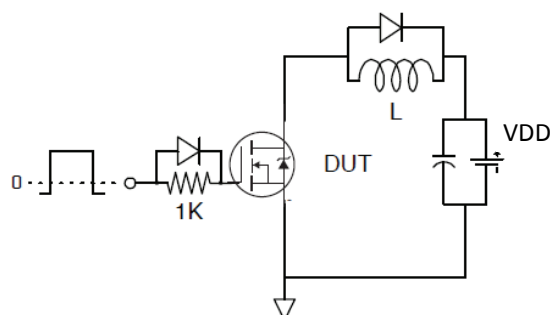


Fig 25a. Gate Charge Test Circuit

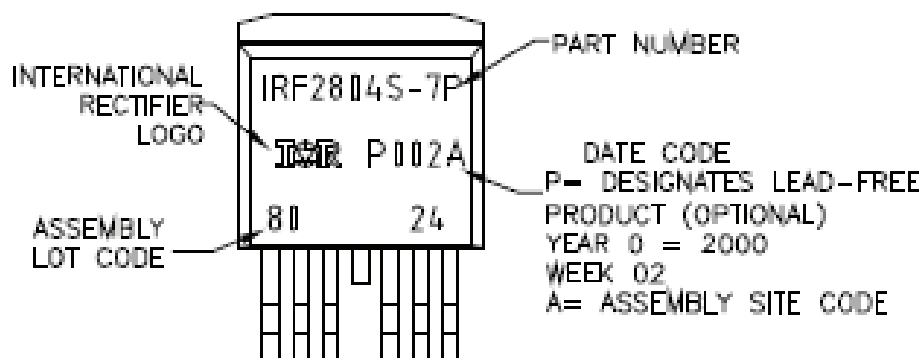
Fig 25b. Gate Charge Waveform

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
e2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		4
L4	4.78	5.28	.188	.208	

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

November 7, 2014

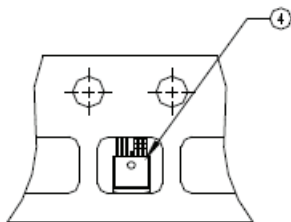
D²Pak-7Pin Part Marking Information



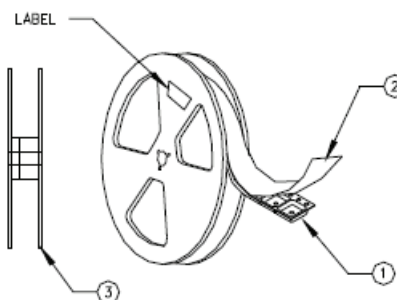
D2Pak-7Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL
 - 1.1 REEL SIZE 13 INCH DIAMETER.
 - 1.2 EACH REEL CONTAINING 800 DEVICES.
 - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
 - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
 - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
 - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



2. LABELLING (REEL AND SHIPPING BAG).
 - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
 - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
 - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
 - 2.4 QUANTITY:
 - 2.5 VENDOR CODE: IR
 - 2.6 LOT CODE:
 - 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	D ² Pak-7Pin	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
11/7/2014	- Updated $E_{AS} (L=1mH) = 897mJ$ on page 2 - Updated note 9 "Limited by T_{Jmax}, starting $T_J = 25^{\circ}C$, $L = 1mH$, $R_G = 50\Omega$, $I_{AS} = 42A$, $V_{GS} = 10V$" on page 2

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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