

# TPS561201 Step-Down Converter Evaluation Module User's Guide



## ABSTRACT

This user's guide contains information for the TPS561201 as well as support documentation for the TPS561201EVM-896 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS561201EVM-896.

## Table of Contents

<b>1 Introduction</b> .....	3
<b>2 Performance Specification Summary</b> .....	4
<b>3 Modifications</b> .....	5
3.1 Output Voltage Setpoint.....	5
<b>4 Test Setup and Results</b> .....	6
4.1 Input/Output Connections.....	6
4.2 Start-Up Procedure.....	6
4.3 Efficiency.....	7
4.4 Load Regulation.....	8
4.5 Line Regulation.....	8
4.6 Load Transient Response.....	9
4.7 Output Voltage Ripple.....	9
4.8 Input Voltage Ripple.....	10
4.9 Start-Up.....	10
4.10 Shut-Down.....	11
<b>5 Board Layout</b> .....	12
5.1 Layout.....	12
<b>6 Schematic, Bill of Materials, and Reference</b> .....	13
6.1 Schematic.....	14
6.2 Bill of Materials.....	14
6.3 Reference.....	16
<b>7 Revision History</b> .....	16

## List of Figures

Figure 4-1. Efficiency.....	7
Figure 4-2. Light-Load Efficiency.....	7
Figure 4-3. Load Regulation.....	8
Figure 4-4. Line Regulation.....	8
Figure 4-5. Load Transient Response, 10% to 100% Load Step.....	9
Figure 4-6. Output Voltage Ripple, $I_{OUT} = 1\text{ A}$ .....	9
Figure 4-7. Output Voltage Ripple, $I_{OUT} = 250\text{ mA}$ .....	9
Figure 4-8. Output Voltage Ripple, $I_{OUT} = 10\text{ mA}$ .....	9
Figure 4-9. Input Voltage Ripple, $I_{OUT} = 1\text{ A}$ .....	10
Figure 4-10. Start-Up Relative to Input Voltage.....	10
Figure 4-11. Start-Up Relative to EN.....	10
Figure 4-12. Shut-Down Relative to Input Voltage.....	11
Figure 4-13. Shut-Down Relative to EN.....	11
Figure 5-1. Top Assembly.....	12
Figure 5-2. Top Layer.....	12
Figure 5-3. Bottom Layer.....	12
Figure 6-1. TPS561201EVM-896 Schematic Diagram.....	14

## List of Tables

Table 1-1. Input Voltage and Output Current Summary.....	3
Table 2-1. TPS561201EVM-896 Performance Specifications Summary.....	4
Table 3-1. Output Voltages.....	5
Table 4-1. Connection and Test Points.....	6
Table 6-1. Bill of Materials.....	14

## Trademarks

D-CAP2™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 1 Introduction

The TPS561201 is a single, adaptive on-time, D-CAP2™ mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 580 kHz and enters plus skip mode in light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS561201 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS561201 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS561201 dc/dc synchronous converter is designed to provide up to a 1-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.768 V to 7 V. Rated input voltage and output current ranges for the evaluation module are given in [Table 1-1](#).

The TPS561201EVM-896 evaluation module (EVM) is a single, synchronous buck converter providing 1.05 V at 1 A from 4.5-V to 17-V input. This user's guide describes the TPS561201EVM-896 performance.

**Table 1-1. Input Voltage and Output Current Summary**

EVM	Input Voltage ( $V_{IN}$ ) Range	Output Current ( $I_{OUT}$ ) Range
TPS561201EVM-896	4.5 V to 17 V	0 A to 1 A

## 2 Performance Specification Summary

A summary of the TPS561201EVM-896 performance specifications is provided in [Table 2-1](#). Specifications are given for an input voltage of  $V_{IN} = 12\text{ V}$  and an output voltage of  $1.05\text{ V}$ , unless otherwise noted. The ambient temperature is  $25^{\circ}\text{C}$  for all measurement, unless otherwise noted.

**Table 2-1. TPS561201EVM-896 Performance Specifications Summary**

Specifications		Test Conditions	MIN	TYP	MAX	Unit
$V_{IN}$	Input voltage range		4.5	12	17	V
CH1	Output voltage			1.05		V
	Operating frequency	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$		580		kHz
	Output current range		0		2	A
	Overcurrent limit	$V_{IN} = 12\text{ V}$ , $L = 2.2\text{ }\mu\text{H}$		1.6		A
	Output ripple voltage	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$		20		mV <sub>PP</sub>

### 3 Modifications

These evaluation modules are designed to provide access to the features of the TPS561201. Some modifications can be made to this module.

#### 3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.768 V. The value of R1 for a specific output voltage can be calculated using [Equation 1](#).

$$R1 = \frac{R2 \times (V_{OUT} - 0.768 \text{ V})}{0.768 \text{ V}} \quad (1)$$

[Table 3-1](#) lists the R5 values for some common output voltages. Note that the values given in [Table 3-1](#) are standard values and not the exact value calculated using [Table 3-1](#).

**Table 3-1. Output Voltages**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C5 + C6 + C7 (μF)
			MIN	TYP	MAX	
1.0	3.09	10.0	2.2	2.2	4.7	20 - 68
1.05	3.74	10.0	2.2	2.2	4.7	20 - 68
1.2	5.76	10.0	2.2	2.2	4.7	20 - 68
1.5	9.53	10.0	2.2	2.2	4.7	20 - 68
1.8	13.7	10.0	2.2	2.2	4.7	20 - 68
2.5	22.6	10.0	3.3	3.3	4.7	20 - 68
3.3	33.2	10.0	3.3	3.3	4.7	20 - 68
5.0	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75.0	10.0	3.3	4.7	4.7	20 - 68

## 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS561201EVM-896. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

### 4.1 Input/Output Connections

The TPS561201EVM-896 is provided with I/O connectors and test points as shown in [Table 4-1](#). A power supply capable of supplying 1 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 1 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

**Table 4-1. Connection and Test Points**

Reference Designator	Function
J1	$V_{IN}$ (see <a href="#">Table 1-1</a> for $V_{IN}$ range)
J2	$V_{OUT}$ , 1.05 V at 1-A maximum
JP1	EN control. Shunt EN to GND to disable, shunt EN to $V_{IN}$ to enable.
TP1	$V_{IN}$ positive monitor point
TP2	GND monitor test point
TP3	EN test point
TP4	Switch node test point
TP5	Test point for loop response measurements
TP6	$V_{OUT}$ positive monitor point
TP7	GND monitor test point
TP8	GND monitor test point

### 4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate  $V_{IN}$  voltage to  $V_{IN}$  (J1-2) and GND (J1-1).
3. Move the jumper at JP1 (Enable control) from pins 1 and 2 (EN and GND), to pins 2 and 3 (EN and  $V_{IN}$ ) enabling the output.

### 4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS561201EVM-896 at an ambient temperature of 25°C.

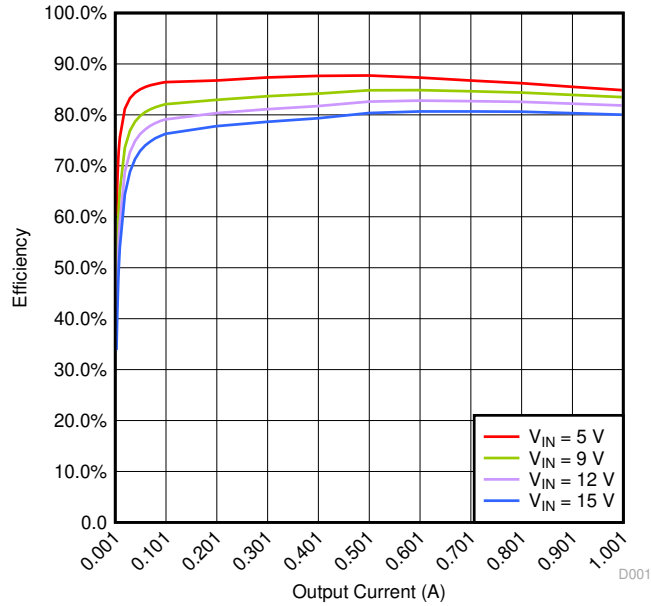


Figure 4-1. Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS561201EVM-896 at an ambient temperature of 25°C.

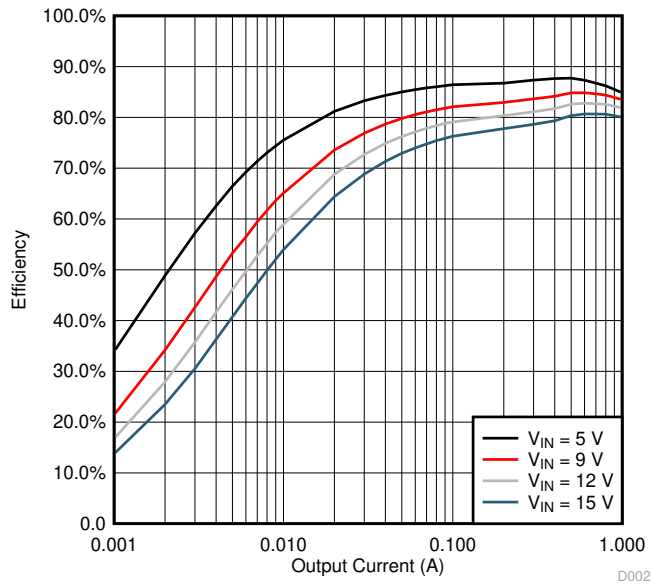
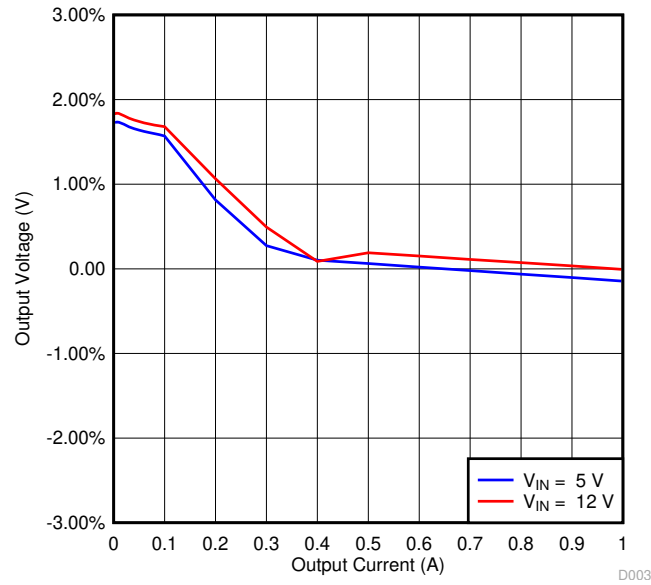


Figure 4-2. Light-Load Efficiency

### 4.4 Load Regulation

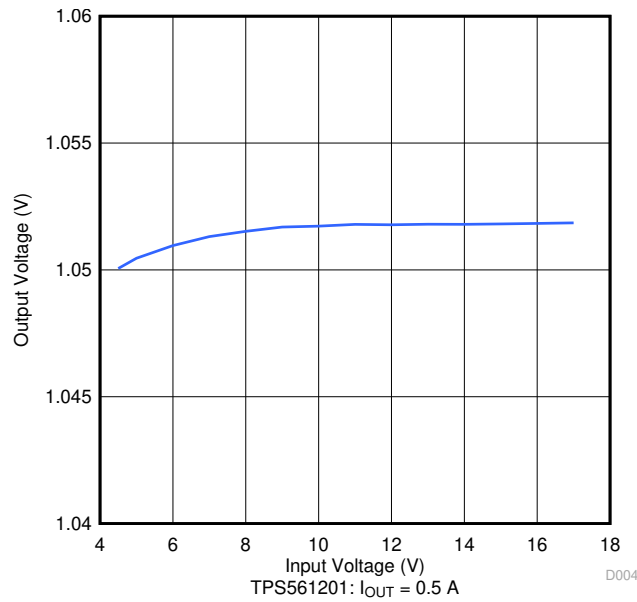
The load regulation for the TPS561201EVM-896 is shown in [Figure 4-3](#).



**Figure 4-3. Load Regulation**

### 4.5 Line Regulation

The line regulation for the TPS561201EVM-896 is shown in [Figure 4-4](#).



**Figure 4-4. Line Regulation**



## 4.6 Load Transient Response

The TPS561201EVM-896 response to load transient is shown in Figure 4-5. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

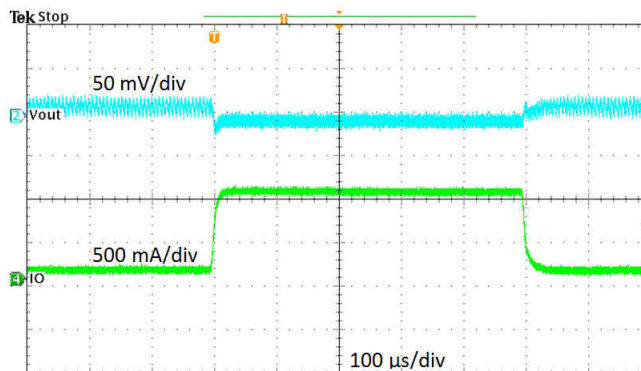


Figure 4-5. Load Transient Response, 10% to 100% Load Step

## 4.7 Output Voltage Ripple

The TPS561201EVM-896 output voltage ripple is shown in Figure 4-6, Figure 4-7, and Figure 4-8. The output currents are as indicated.

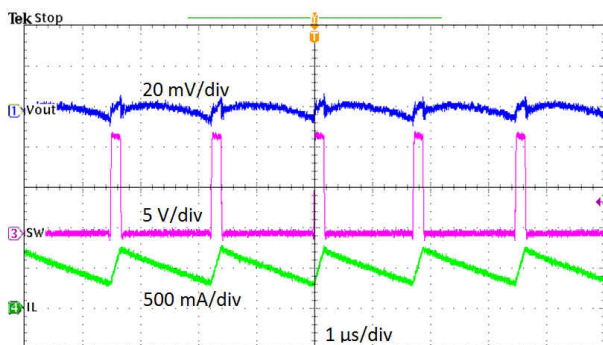


Figure 4-6. Output Voltage Ripple,  $I_{OUT} = 1\text{ A}$

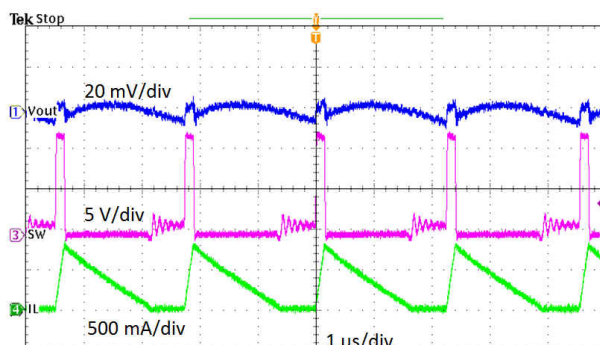


Figure 4-7. Output Voltage Ripple,  $I_{OUT} = 250\text{ mA}$

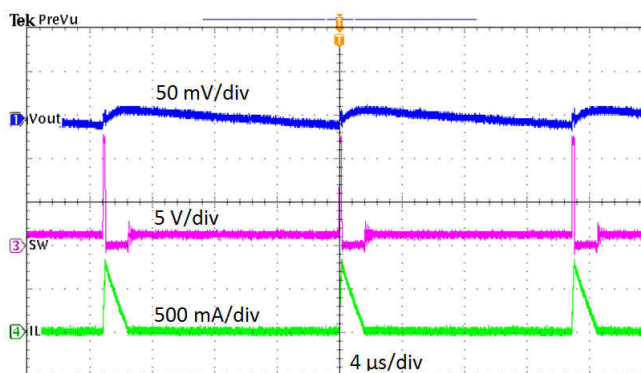
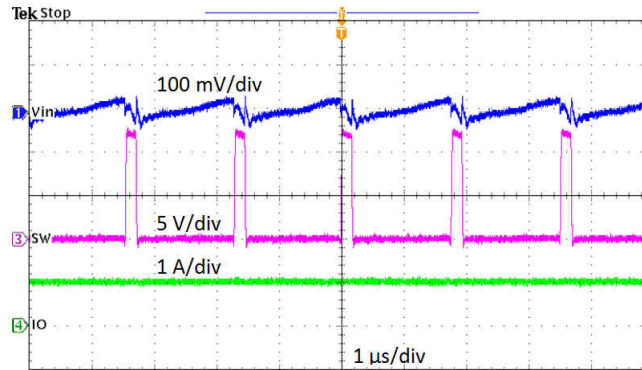


Figure 4-8. Output Voltage Ripple,  $I_{OUT} = 10\text{ mA}$

## 4.8 Input Voltage Ripple

The TPS561201EVM-896 input voltage ripple is shown in [Figure 4-9](#). The output current is as indicated.

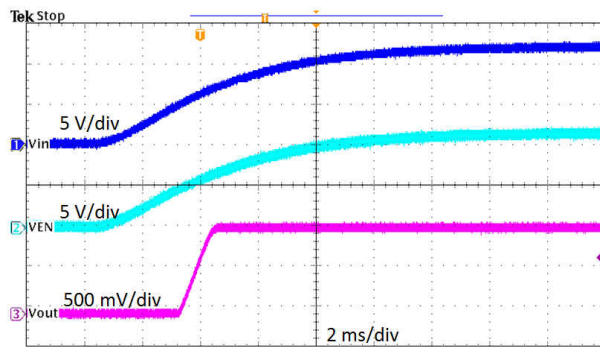


**Figure 4-9. Input Voltage Ripple,  $I_{OUT} = 1\text{ A}$**

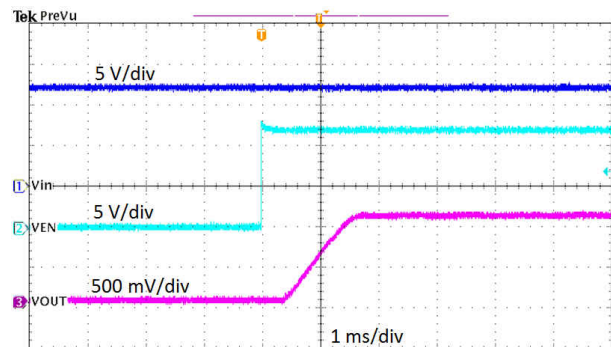
## 4.9 Start-Up

The TPS561201EVM-896 start-up waveform relative to  $V_{IN}$  is shown in [Figure 4-10](#). Load = 1.05  $\Omega$  resistive.

The TPS561201EVM-896 start-up waveform relative to enable (EN) is shown in [Figure 4-11](#). Load = 1.05  $\Omega$  resistive.



**Figure 4-10. Start-Up Relative to Input Voltage**



**Figure 4-11. Start-Up Relative to EN**

### 4.10 Shut-Down

The TPS561201EVM-896 shut-down waveform relative to  $V_{IN}$  is shown in Figure 4-12. Load = 1.05  $\Omega$  resistive.

The TPS561201EVM-896 shut-down waveform relative to EN is shown in Figure 4-13. Load = 1.05  $\Omega$  resistive.

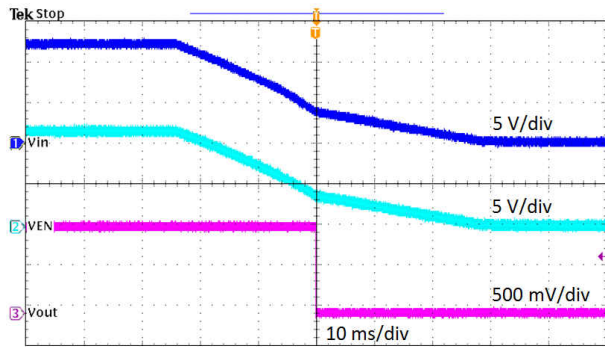


Figure 4-12. Shut-Down Relative to Input Voltage

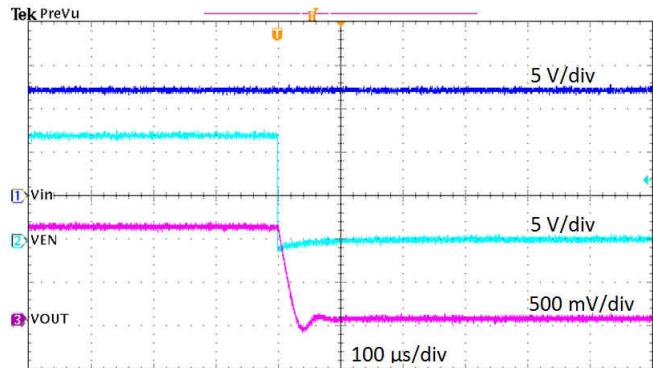


Figure 4-13. Shut-Down Relative to EN

## 5 Board Layout

This section provides a description of the TPS561201EVM-896, board layout, and layer illustrations.

### 5.1 Layout

The board layouts for the TPS561201EVM-896 are shown in [Figure 5-1](#), [Figure 5-2](#), and [Figure 5-3](#). The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS561201 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill, and the feedback trace from the point of regulation to the top of the resistor divider network.

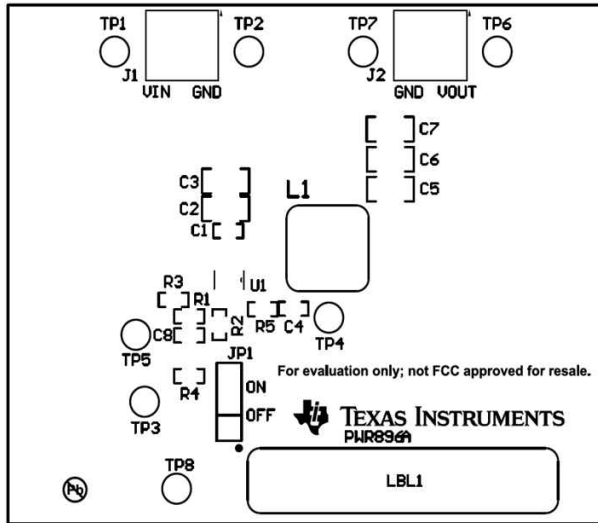


Figure 5-1. Top Assembly

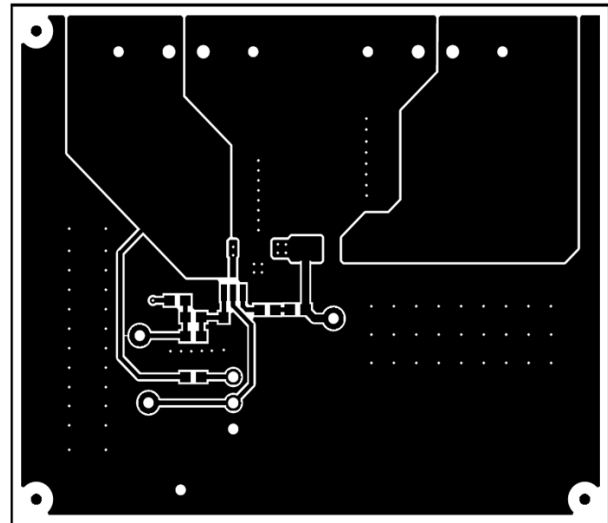


Figure 5-2. Top Layer

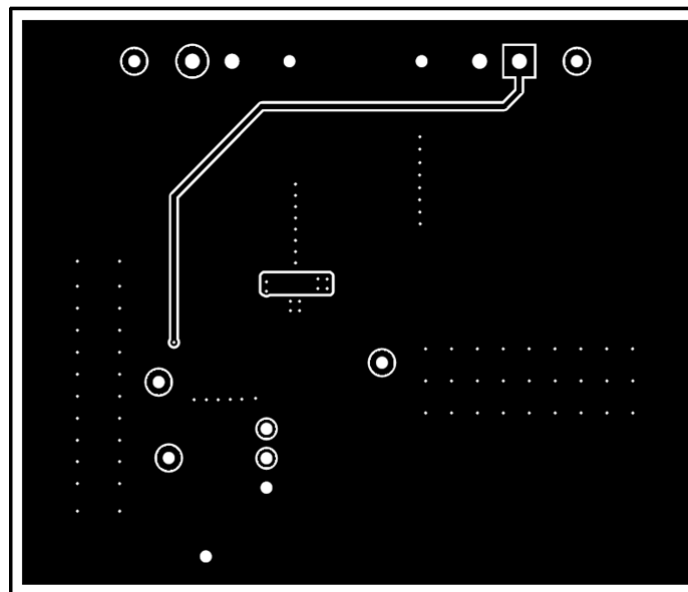


Figure 5-3. Bottom Layer

## **6 Schematic, Bill of Materials, and Reference**

## 6.1 Schematic

Figure 6-1 is the schematic for the TPS561201EVM-896.

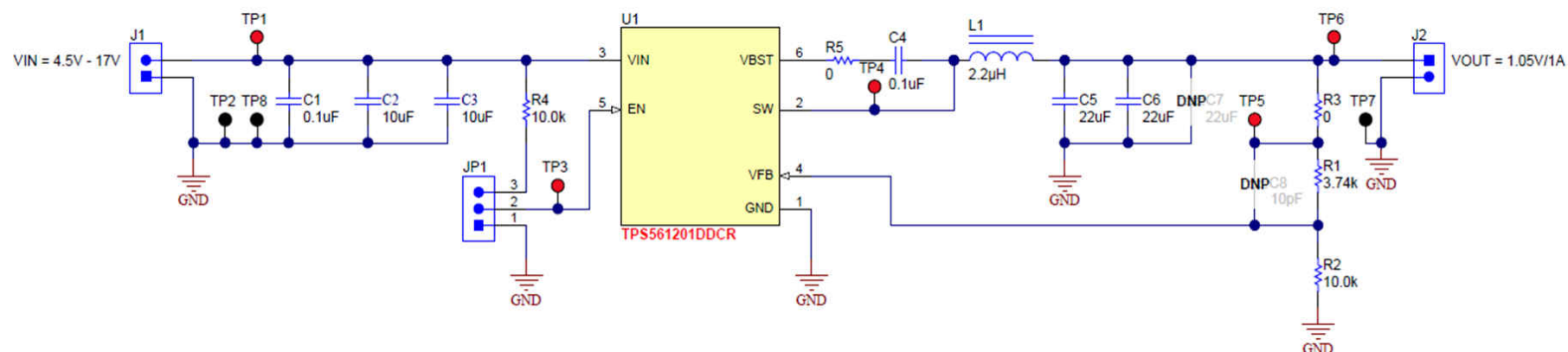


Figure 6-1. TPS561201EVM-896 Schematic Diagram

## 6.2 Bill of Materials

Table 6-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PWR896	Any
C1, C4	2	0.1 $\mu$ F	Capacitor, ceramic, 0.1 $\mu$ F, 25 V, $\pm$ 10%, X5R, 0603	0603	GRM188R61E104KA01D	Murata
C2, C3	2	10 $\mu$ F	Capacitor, ceramic, 10 $\mu$ F, 25 V, $\pm$ 10%, X5R, 1206	1206	GRM31CR61E106KA12L	Murata
C5, C6	2	22 $\mu$ F	Capacitor, ceramic, 22 $\mu$ F, 10 V, $\pm$ 10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata
C8	0	10 pF	Capacitor, ceramic, 10 pF, 100 V, $\pm$ 5%, C0G/NP0, 0603	0603	GRM1885C2A100JA01D	Murata
J1, J2	2		Terminal block, 6 A, 3.5 mm pitch, 2-Pos, TH	7.0 x 8.2 x 6.5mm	ED555/2DS	On-Shore Technology
JP1	1		Header, 100 mil, 3 x 1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
L1	1	2.2 $\mu$ H	Inductor, Shielded drum core, superflux, 2.2uH, 9A, 0.0115 $\Omega$ , SMD	WE-HC4	744311220	Wurth Elektronik eiSos
LBL1	1		Thermal transfer printable labels, 1.250" W x 0.250" H (10,000 per roll)	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R1	1	3.74 k $\Omega$	Resistor, 3.74 k $\Omega$ , 1%, 0.1 W, 0603	0603	CRCW06033K74FKEA	Vishay-Dale
R2, R4	2	10.0 k $\Omega$	Resistor, 10.0 k $\Omega$ , 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R3, R5	2	0	Resistor, 0 $\Omega$ , 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
SH-JP1	1	1 x 2	Shunt, 100 mil, gold plated, black	Shunt	969102-0000-DA	3M
TP1, TP3, TP4, TP5, TP6	5	Red	Test point, miniature, red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP7, TP8	3	Black	Test point, miniature, black, TH	Black Miniature Testpoint	5001	Keystone
U1	1		4.5 V to 16 V Input, 1-A synchronous step-down voltage regulator, DDC0006A	DDC0006A	TPS561201DDC	Texas Instruments

**Table 6-1. Bill of Materials (continued)**

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C7	0	22 $\mu$ F	Capacitor, ceramic, 22 $\mu$ F, 10V, $\pm$ 10%, X7R, 1206	1206	GRM31CR71A226KE15L	Murata

### 6.3 Reference

1. *TPS56120x 4.5 V to 17 V Input, 1-A Synchronous Step-Down Voltage Regulator in SOT-23 data sheet (SLVSC95)*

### 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (April 2017) to Revision A (August 2021)</b>	<b>Page</b>
• Updated user's guide title.....	3
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	3

---



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated