

FEATURES

- Configured for 200W, 36 to 72V
- Provision for Short Pin Control of Turn-on
- I2C Monitoring of Load Current, Input and Output Voltage
- I2C Control of Device Features and Reporting of Device Status
- Provision for On-Board Input and Output Bypassing
- High Voltage Layout Enforces 60 mil Minimum Spacing
- LEDs Indicate +48V Input, +48V/5A Output, Power Bad, Alert Status, and I2C Port Logic States
- Input Clamping Included On Board

APPLICATIONS


- Servers, Routers, Switches
- Mass Storage
- Central Office Computing
- Fan Trays

DESCRIPTION

Demonstration Circuit 786 showcases the LTC[®]4260CGN positive high voltage Hot Swap[™] controller with I2C compatible monitoring in a 200W, 36 to 72V application. Included on board is an input clamp and snubber, input and output voltage dividers for UV, OV, and PWRGD, LEDs to indicate the presence of various voltages and signals, high voltage layout rules and turret terminals for critical signals to facilitate evaluation in a working system.

A distinct line of demarcation runs the length of the board, separating high voltage +48V referred potentials from ground. Input and output connections are made by 93 mil turrets which if removed, accommodate insertion of up to 12 gauge wires for in-situ testing. An I2C port designed to interface with DC590A allows control of DC786A with LTC's Quick Eval software.

Design files for this circuit board are available. Call the LTC factory.

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BOARD LAYOUT

The top of the board contains the core Hot Swap controller and associated components, along with LEDs. Also on top are various configuration jumpers and all connection turrets. The large turrets may be removed to permit installation of up to 12 gauge wire for direct, low resistance connections to the board. None of the turrets are swaged.

The bottom of the board contains components for software identification of the board, provision for A to D converter input scaling dividers, I2C line LED driv-

ers, and LED current limiting resistors. Also on the bottom is the LTC4260CGN supply bypass capacitor, C3, and space for optional input and output bypassing. Except for C3, the other components are largely unrelated to the core application and are included for the purposes of the demo board itself.

Thermal layout requirements for the FDB3632 MOSFET are modest, as the maximum, continuous worst-case dissipation is less than 600mW. Typical dissipation is less than 150mW, resulting in a temperature rise of less than 10°C.

The board is designed with two ground planes, on layers 2 and 3. Layer 2 is a small signal ground plane which picks up ground for dividers, PROBE GND, the small GND turrets, C3 and the timing capacitor, CT, as well as all I2C and configuration jumper related grounding. Layer 3 is reserved for large signal grounding, including CIN, COUT, 3 large GND turrets, input and output LEDs, and the input clamp and snubber. These two ground planes join at PROBE GND. The large GND turrets are provided to accommodate multiple ground connections of meters, power supplies, loads, etc., and there is no need for load current to be routed through the circuit board.

A clear line of demarcation separates +48V copper from ground, passing under R9, CIN, Z1, CSNUB, R27, R1, U1, R7, C1 COUT, and R10. 55-60 mils spacing on unpassivated surfaces is generally recommended for 48V circuits. This rule is bent in the vicinity of the LTC4260CGN's pins 2, 3 and 4, where the spacing necks down to about 30 mils. In practice this area could be passivated with conformal coating, or one of the other package options could be used (see the LTC4260 data sheet).

CIRCUIT NOTES

DC786A uses an $8\text{m}\Omega$, 5% sense resistor (R5). Coupled with the LTC4260's minimum current limit sense voltage threshold of 40mV, this guarantees a minimum current of 4.76A before the onset of current limiting or circuit breaker action. Thus 200W is available down to approximately 42V, dropping to $\approx 170\text{W}$ at 36V. Using a less common sense resistor value of $7\text{m}\Omega$ increases the power at 36V to 195W.

The UV and OV trip points are set by separate dividers to facilitate modification. The trip points are as follows:

UV turning on = 43V
UV turning off = 38.5V
OV turning off = 71V
OV turning on = 69.2V

A/D CONVERTER INPUT OPTIONS

The A/D external monitor input (pin 13, ADIN) is connected to a jumper, **JP8**, ADIN SELECT. As shipped this jumper connects ADIN to a divider (R11, R12) which in turn connects to the +48V input, and gives a full scale of approximately 100V. Moving the jumper to EXT connects R14 and R17. The board is stuffed with $R14=10\text{k}\Omega$ and R17 is omitted; in this condition the ADIN turret connected to the LTC4260's ADIN pin through $10\text{k}\Omega$ and as shown, gives a 2.56V full scale sensitivity. R11, R12, R14, and R17 may be changed to accommodate different scaling factors. The ADIN pin full scale is 2.56V, $\pm 2\%$.

The R11-R12 divider is built with 1% resistors, which add up to 2% measurement error. Up to 4% total measurement error is possible, or 2V error out of a 50V input.

MORE CURRENT

Space is provided for up to three 2010 surface mount sense resistors, and a TO-247 (TO-3P) MOSFET. This allows modification of the board for higher current applications. There is more copper between +48V INPUT and +48V/5A OUTPUT than the turrets and a TO-247 can handle. The limitation is at the source of Q1, where the trace narrows to about 200 mils X 4 layers, all 1 ounce. This is good for about 40A continuous. There is an equivalent of about 1 to 1.5 squares of 1-ounce copper between the input and output turret terminals.

Kelvin sensing is located under the center R5 position. If using 1 resistor, put it in the middle; if using 2 resistors (ideally equal value) put them in the outside positions; if using a high value resistor to "trim" a low value unit, put the low value component in the middle and the high value component on the outside.

Q1 is best removed with two large, hot soldering irons, such as a Weller WTCPS controlled temperature iron with a PTE8 tip. First cut the leads (or desolder and lift), then apply the heat along Q1's tab shear line, and pluck the part from the board using a pliers and a third hand, immediately removing the soldering irons. Tab removal should take only a few seconds.

In high current applications do not forget to upgrade Z1. If long leads are present between the LTC4260 and load bypassing, install 10 μ F or more bypassing at COUT to eliminate the chance of MOSFET oscillation and large negative excursions at +48V/5A OUTPUT.

SHORT PINS

If your system uses a short pin to sense board insertion, move **JP1** to SHORT PIN and, using the SHORT PIN turret, connect the aforementioned short pin. This is a direct connection to the LTC4260's BD_PRST\ pin; if deleterious voltages are anticipated, add a series resistor and clamping. BD_PRST\ is good for -0.3 to +12V on its own.

BD_PRST\ is also logic compatible, with a 1.235V threshold and 130mV hysteresis.

PWRGD (GPIO)

Refer to the schematic. The LTC4260 GPIO pin defaults to an open drain power good configuration, going high when FB determines the output voltage is adequate. In this configuration GPIO pulls low when power is bad, and turns on D3. D3 pulls to the output rail, demonstrating the high voltage capability of GPIO. If GPIO is reconfigured as an input by I2C control or used as a logic output, simply remove R4 (on the bottom of the board).

PROBE GND

Use this if you need to refer measurements to the LTC4260's ground. Do not connect power supplies and loads to this ground.

INTVCC

INTVCC was included on the LTC4260 to allow bypassing of the internal 5.5V supply rail for superior noise immunity. It is also permissible to steal a small current of up to 1mA off of the INTVCC pin to bias address pins or ancillary circuits. A turret is provided for connections to INTVCC.

CIN, COUT

The LTC4260 serves equally well on either side of the connector; as a port on a backplane or as a card-centric Hot Swap controller. Holes are included for addition of an input capacitor or load capacitor at CIN and COUT. Do not neglect polarity markings.

ALERT\

If the evaluation software is set to free-run (using the "Start" button), alert conditions will turn on D4 (red) but just as quickly, D4 will extinguish when the software polls the LTC4260. D4 therefore lights for only a brief flash in the free-run mode. If you want to see it stay lit, operate the software interface in "Refresh" (manual) mode.

I2C PORT

If the I2C port (**JP7**) is disconnected, the turret terminals SDAO, SDAI, and SCL can be connected directly to an I2C bus. Power for D4-7 is supplied by **JP7**, so in this mode the LEDs will not light. Setting **JP3** SDA to COM connects SDAO and SDAI together for communication to a non-isolated bus. Splitting SDAO and SDAI facilitates optically isolated applications (see the LTC4260 data sheet).

The I2C address is selected by using **JP4**, **JP5** and **JP6** to pull the address pins high, low, or allowing them to float. An address table is shown in the data sheet. The evaluation software automatically scans and identifies the I2C address, regardless of the setting.

JUMPER SUMMARY

JP1 BD_PRST\: connects BD_PRST\ pin either to ground or to the SHORT PIN turret. SHORT PIN is then connected to logic, an opto isolator, a short pin, or an insertion detection switch to initiate turn-on of the LTC4260.

JP2 ON CONFIG: at start-up the LTC4260 operates in one of two modes: in AUTO mode it turns on when BD_PRST\ is grounded; in I2C mode it waits for

BD_PRST) and an I2C command to turn on. (OV and UV conditions must also be satisfied.)

JP3 SDA: COM is the normal configuration, shorting SDAO and SDAI together. SPLIT allows adaptation to isolated systems; see data sheet Figure 13.

JP4, JP5, JP6, ADR0,1,2: sets address by strapping ADRx pins high, low, or allowing them to float.

JP7 I2C PORT: connector for DC590A I2C adaptor card. This converts a computer's USB port to I2C. DC590A also supplies power via **JP7** to D4-7. If DC590A is not connected, D4-7 will not light.

JP8 ADIN: selects either +48V INPUT or ADIN turret as an input for the ADIN pin. Use divider R14, R17 to scale inputs from the turret.

EVALUATION SOFTWARE

The Quick Eval software is available from the LTC website, and requires a DC590A to interface the software (running on a PC with a USB port) to I2C (at **JP7**). Attached is a quick start guide for the software. Figure 1. shows the default graphical user interface.

1) Register Display Options

The bits of registers A, B, C, or D, are shown in detail depending on the option selected (Figure 2A, 2B 2C, and 2D). Checking a box to the left of each bit of the Read/Write registers sets the respective bit, while unchecking a box clears the bit. The bit status is shown to the right of each bit after every refresh of the interface. The Clear button for register D clears out the bits in this register.

In the Register List option (Figure 2E) a display of a status bit map of the all the registers is shown and is updated with each refresh of the interface.

The Reg Send option (Figure 2F) allows for the user to enter and send data to a particular register. Select the register to be written to in the drop down menu. Enter

the data in hex and click on Send Data to send the data or Send/Refresh so send and refresh the interface.

2) START/Refresh Buttons

Click on the START button to enable a timer that continuously updates the interface with the latest data from the LTC4260 approximately every 500ms. This button will display STOP when the timer is enabled. Click on STOP to stop the timer. Click on Refresh for a single update.

3) FET Control

The status of the FET is shown with a color display. When the FET On bit (C3) is read as high and the FET On Control bit (A3) is set, the FET is On, the shape display will be green and the FET control button will read "Turn FET Off". If C3 is low and A3 is set, the FET is off, the shape display will be the color red and the FET control button will read "Clear Faults". In all other cases, the FET is off, the shape display is red and the FET control button will read "Turn FET On"

The "Turn FET On" control button sets bits A3 logic high. "Turn FET Off" or "Clear Faults" clears bit A3 to logic low.

4) Address Selection

Select in the drop down list box the Write address byte of the LTC4260 that is to be communicated with. If multiple LTC4260s are on the bus lines, the Mass Write address BEh can be selected to communicate with all LTC4260s at the same time. The Auto find button will scan through the 27 individual LTC4260 addresses and list which addresses responded with an acknowledge. The ARA button sends the Alert Response protocol and displays the address of the device that replies with its address.

5) Data Display Option

The Fixed option (Figure 3A) shows the data byte in hex for registers E, F, and G and displays the calculated Vdd sense, Source voltage, and ADIN values using the following equations:

$$V_{dd} \text{ sense} = \text{Sense}(\text{data}) * \text{SenseScale} \text{ mV}$$

$$\text{Source voltage} = \text{Source}(\text{data}) * \text{SourceScale} \text{ V}$$

$$\text{ADIN voltage} = \text{ADIN}(\text{data}) * \text{ADINScale} \text{ V}$$

The Adjusted option allows the user to enter Rs, R1 and R2. The calculated values are shown using the following equations:

$$I_{dd} \text{ sense} = V_{dd} \text{ sense} / R_s \text{ mA}$$

$$\text{ADIN full} = \text{ADIN voltage} * (R_1 + R_2) / R_2 \text{ V}$$

QUICK START PROCEDURE

BASIC OPERATION

Demonstration circuit 786 is easy to set up to evaluate the performance of the LTC4260CGN.

1. To permit autonomous operation, verify that the jumpers are set as follows:

JP1 BD_PRST\ : GND

JP2 ON CONFIG: AUTO

2. With the power off connect the input supply to +48V INPUT and the output load as shown in Fig.4
3. Turn on the power at the input.
4. Check that the LTC4260 automatically turns on. Green LEDs D1 and D2 show when power is applied to the input and available at the output. If the output voltage is low as judged by the PWRGD/GPIO divider R7 and R8, red LED D3 turns on.

The point at which UV deems the input to be worthy of turn-on and GPIO judges the output to be "good" are mutually exclusive; these are two different comparators driven by two different voltage dividers. As configured there is a narrow range between 43V and 47V where D2 and D3 are on simultaneously.

5. To convert to I2C control, set the jumpers as follows:

JP1 BD_PRST\ : GND

JP2 ON CONFIG: I2C

JP3 SDA: COM

JP4 ADR0: LOW

JP5 ADR1: LOW

JP6 ADR2: LOW

JP7 I2C PORT: Connect the DC786A to the DC590A USB controller board via 14-pin ribbon cable and open the QuickEval software on the PC. Upon first connection, QuickEval will identify the DC786A and open the LTC4260 interface. When the interface is closed, the user is returned to the main QuickEval program.

6. In this configuration the LTC4260 defaults to the off condition. D4-7 are useful to view the status of the ALERT\ output and to debug stuck I2C lines. Under normal conditions D5-7 flicker faintly and briefly when a communications transaction takes place. When activated, D4 (ALERT\) stays lit until reset by the I2C port. D4-7 are buffered by Q2-5 so that they do not load the I2C lines.

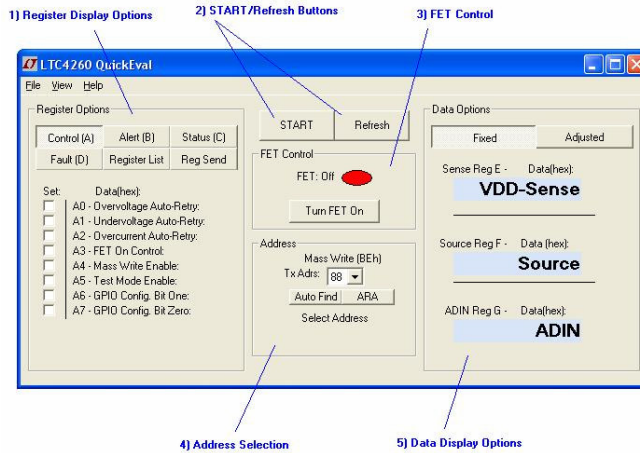


Figure 1. Default LTC4260 Quick Eval Interface

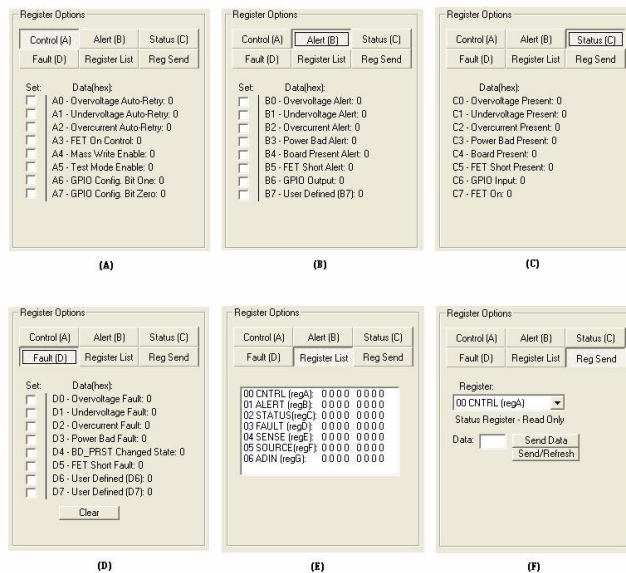


Figure 2. Register Display Options

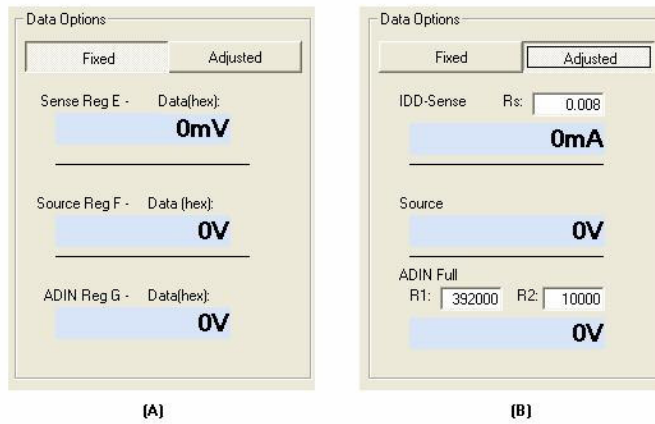


Figure 3. Data Display Options

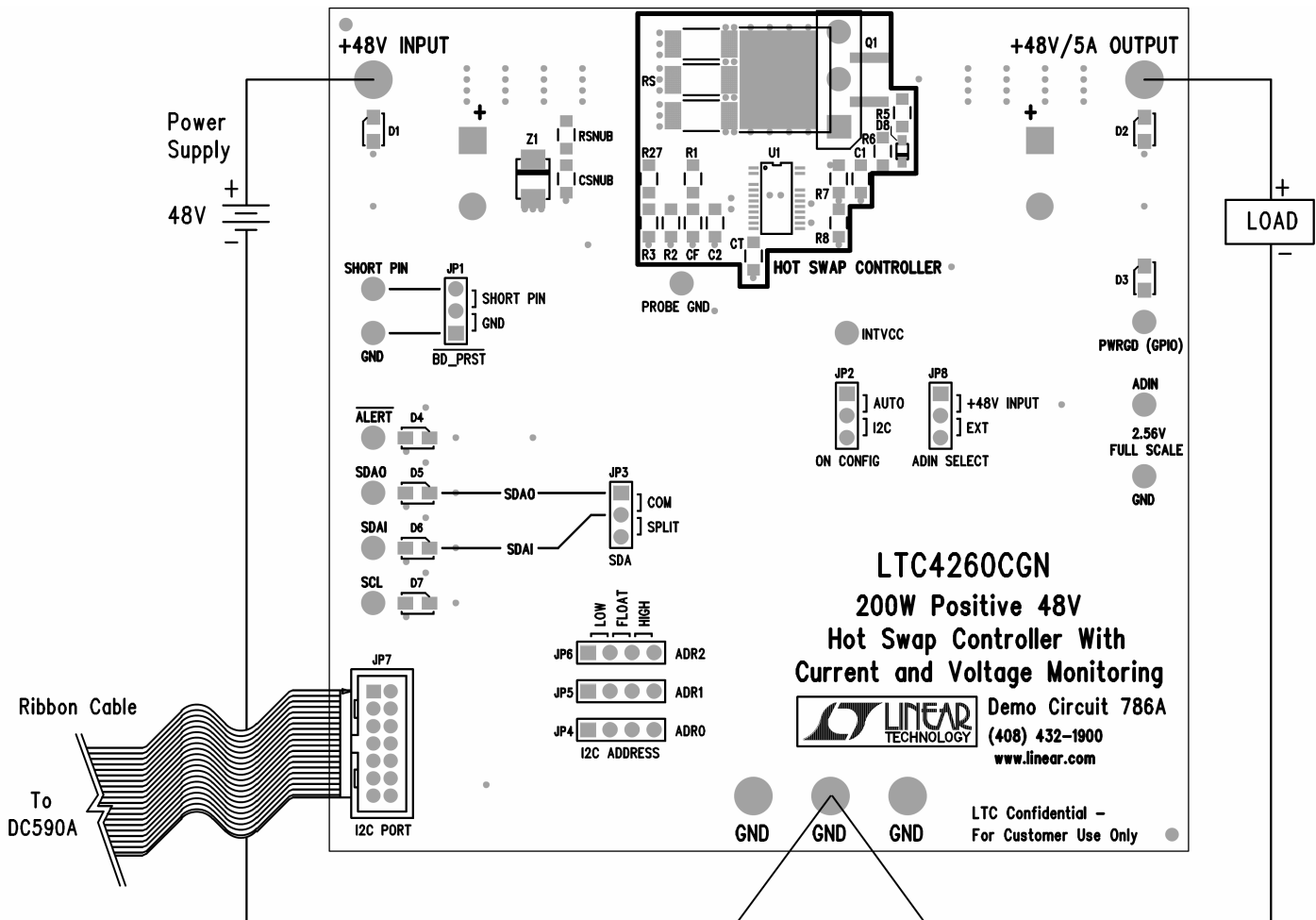
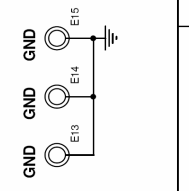
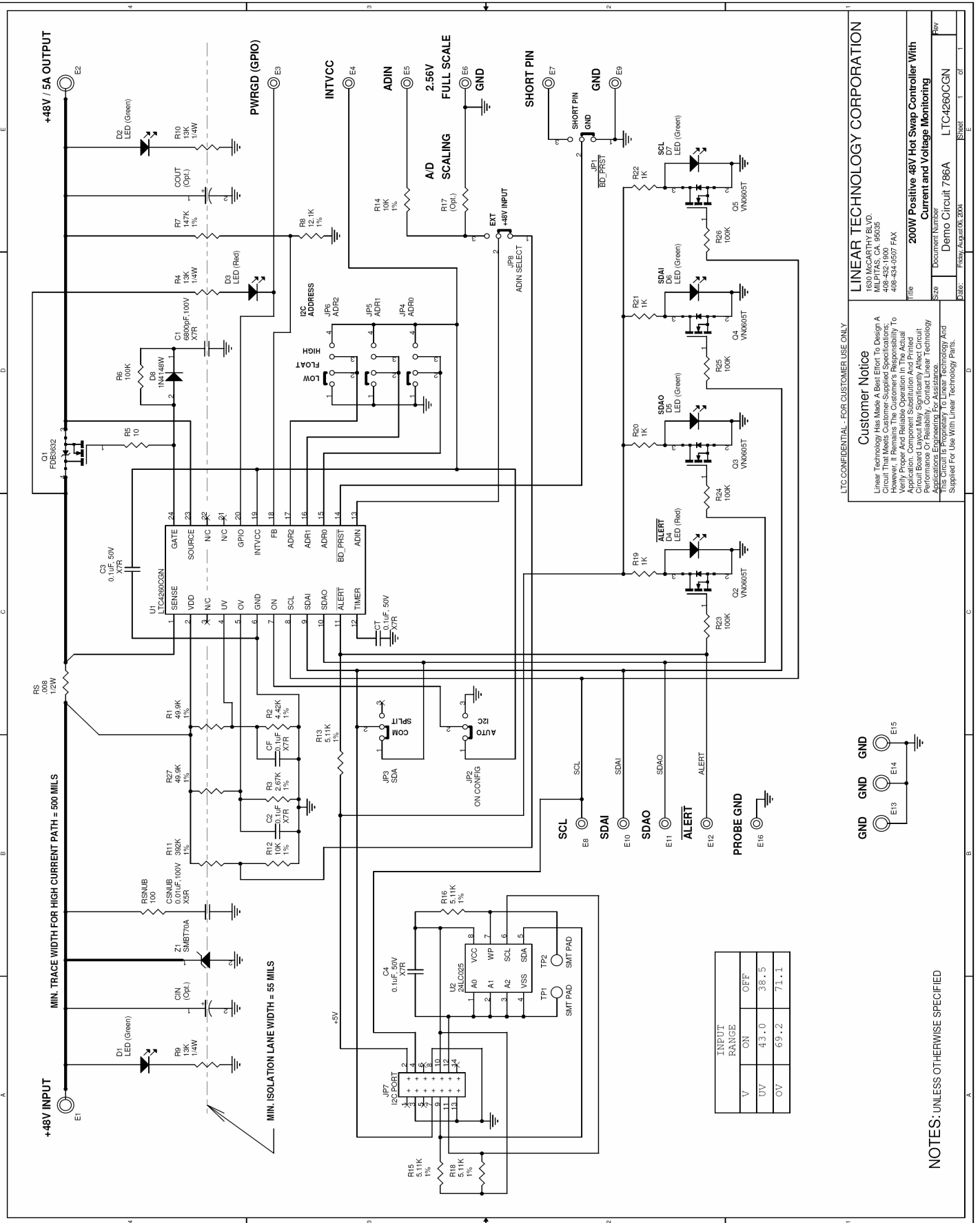


Figure 4. Proper Measurement Equipment Setup



INPUT RANGE	ON	OFF
V	43.0	38.5
UV	69.2	71.1

NOTES: UNLESS OTHERWISE SPECIFIED