CY7C1049BN

512 K × 8 Static RAM

Features

- High speed
  - t_{AA} = 17 ns
- Low active power
  - 1073 mW (max.)
- Low CMOS standby power
  - 2.75 mW (max.)
- 2.0 V data retention (400 µW at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features

Functional Description

The CY7C1049BN is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

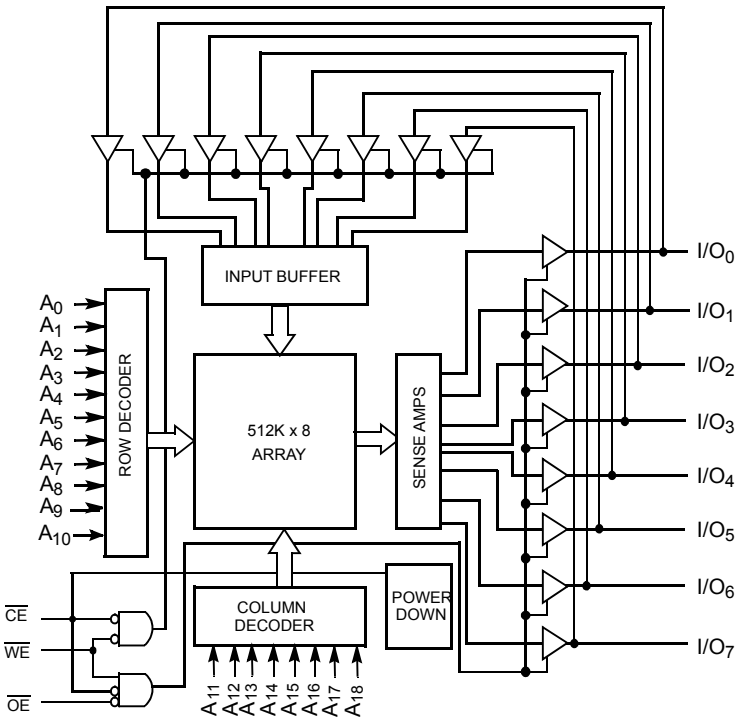
Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049BN is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, click here.

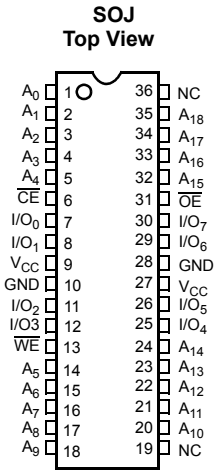
Logic Block Diagram



Contents

Pinouts

Figure 1. 36-pin SOJ pinout (Top View)



Selection Guide

Description	CY7C1049BNL-17
Maximum Access Time (ns)	17
Maximum Operating Current (mA)	195
Maximum CMOS Standby Current (mA)	0.5

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND [1] .....–0.5 V to +7.0 V

DC Voltage Applied to Outputs in High Z State [1] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [1] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial L	0 °C to +70 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C1049B-17		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage [1]		–0.3	0.3	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	–	195	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	40	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3 V, f = 0, Commercial	–	0.5	mA

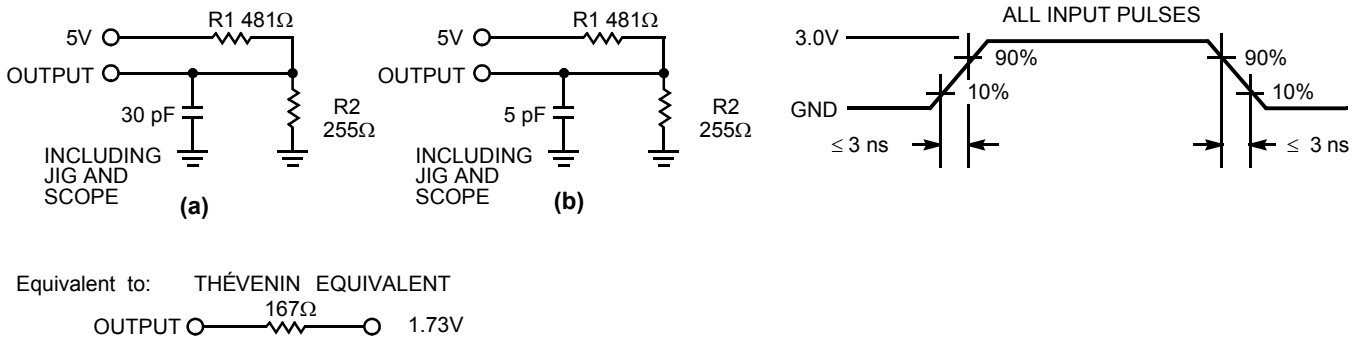
Note
1. Minimum voltage is–2.0V for pulse durations of less than 20 ns.

Capacitance

Parameter [2]	Description	Test Conditions	Max.	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	I/O capacitance		8	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



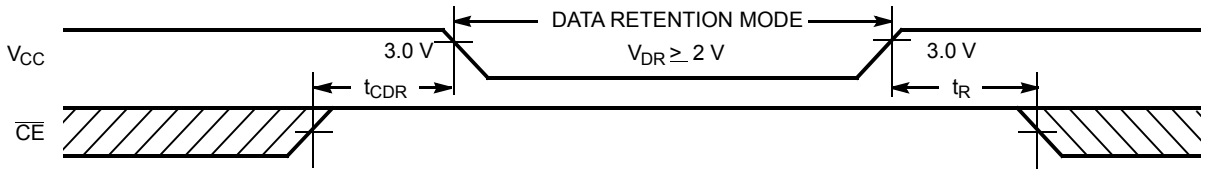
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [3]			Min	Max	Unit
V_{DR}	V_{CC} for Data Retention				2.0	–	V
I_{CCDR}	Data Retention Current	Commercial	L	V_{CC} = V_{DR} = 3.0 V,	–	200	µA
t_{CDR} [2]	Chip Deselect to Data Retention Time			$\overline{CE} \geq V_{CC} - 0.3$ V,	0	–	ns
t_R [4]	Operation Recovery Time			$V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
2. Tested initially and after any design or process changes that may affect these parameters.
3. No input may exceed V_{CC} + 0.5 V.
4. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.

Switching Characteristics

Over the Operating Range

Parameter [5]	Description	CY7C1049BNL-17		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(typical) to the First Access [6]	1	–	ms
t_{RC}	Read Cycle Time	17	–	ns
t_{AA}	Address to Data Valid	–	17	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	17	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7, 8]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [7]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]	–	7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down	–	17	ns
Write Cycle [9, 10]				
t_{WC}	Write Cycle Time	17	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12	–	ns
t_{AW}	Address Set-Up to Write End	12	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-Up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	12	–	ns
t_{SD}	Data Set-Up to Write End	8	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]	–	8	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 [11, 12]

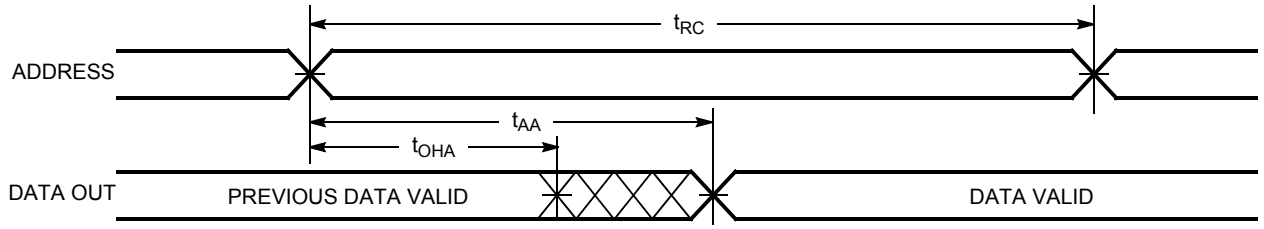
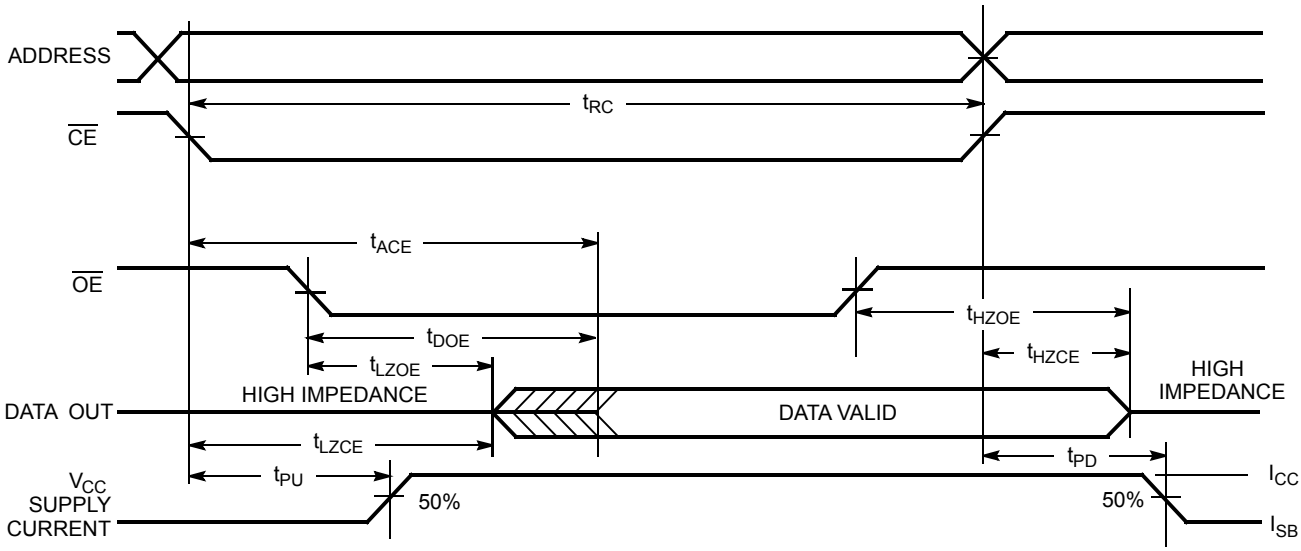


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Notes

11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]

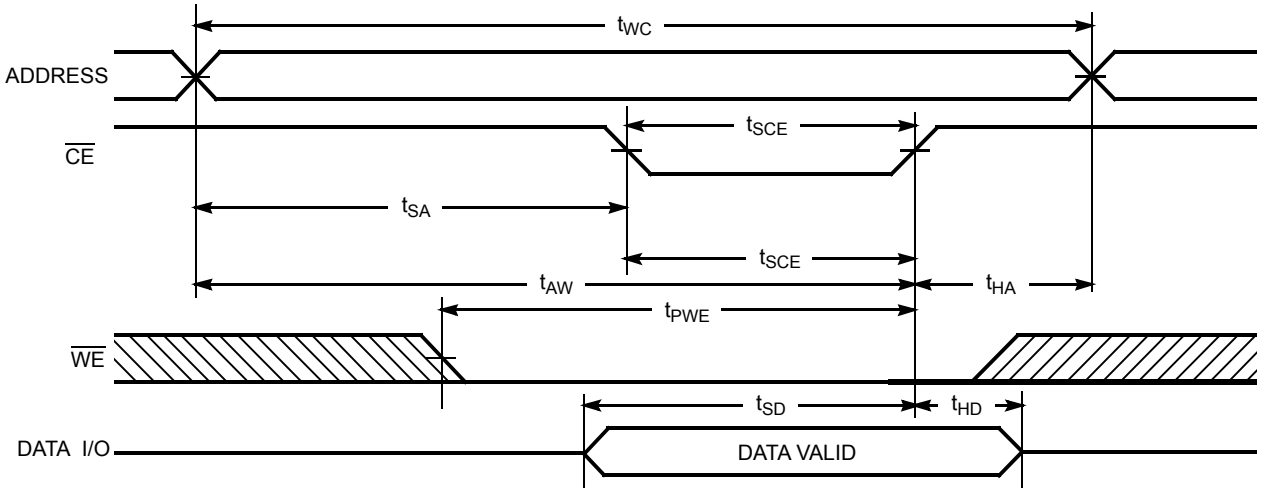
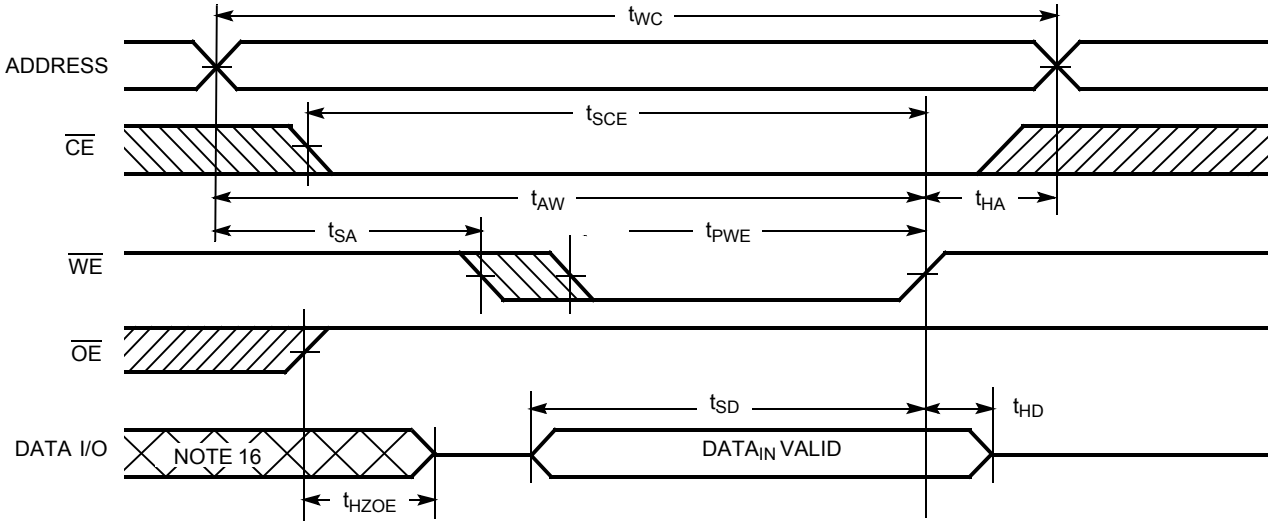


Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH during Write) [14, 15]

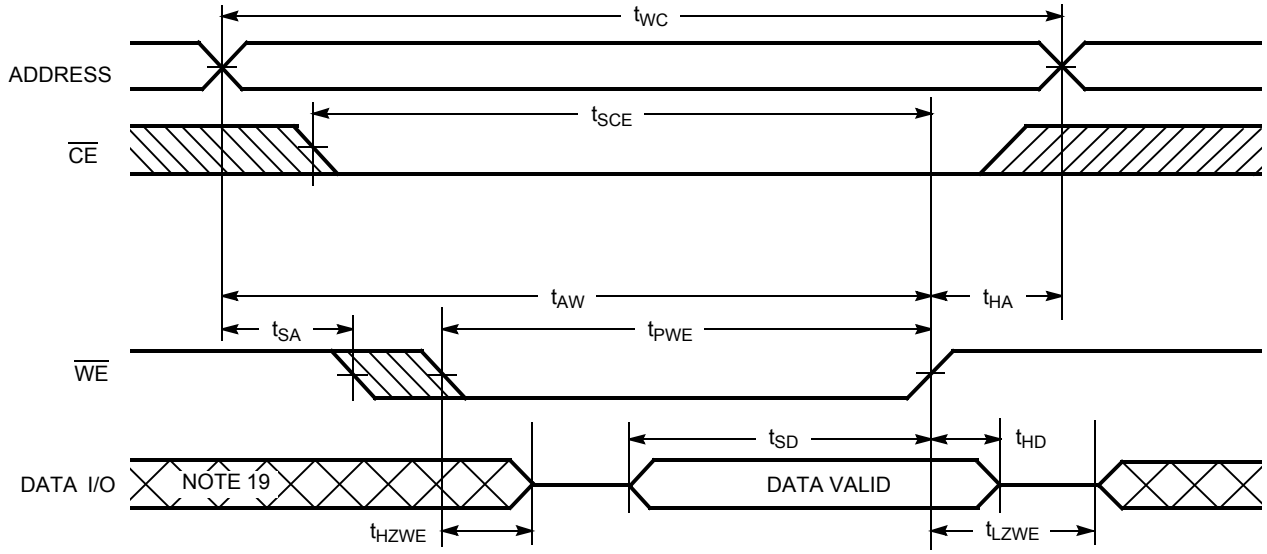


Notes

14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17, 18]



Notes

17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
18. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.
19. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

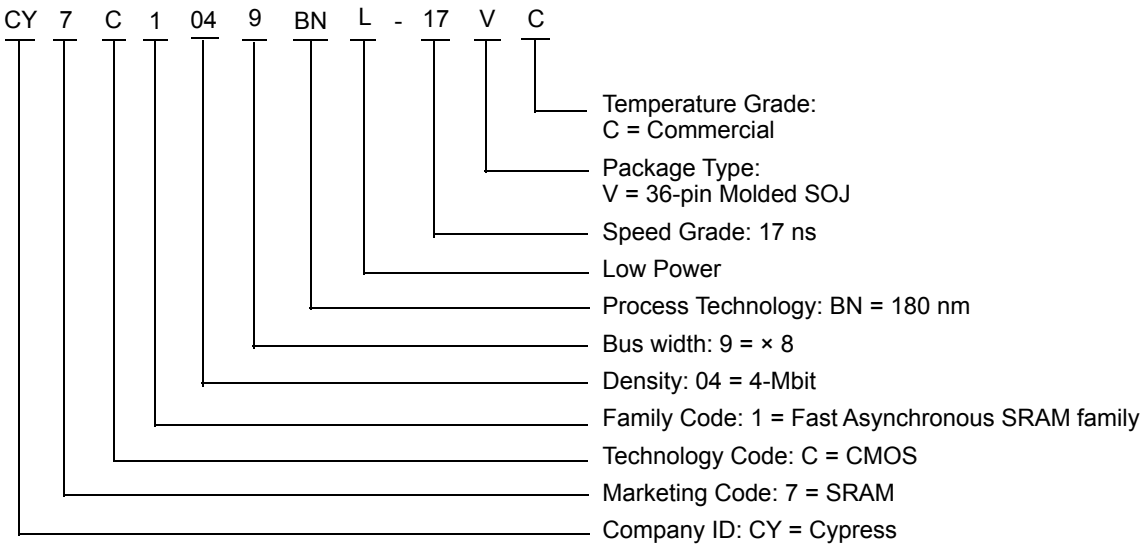
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

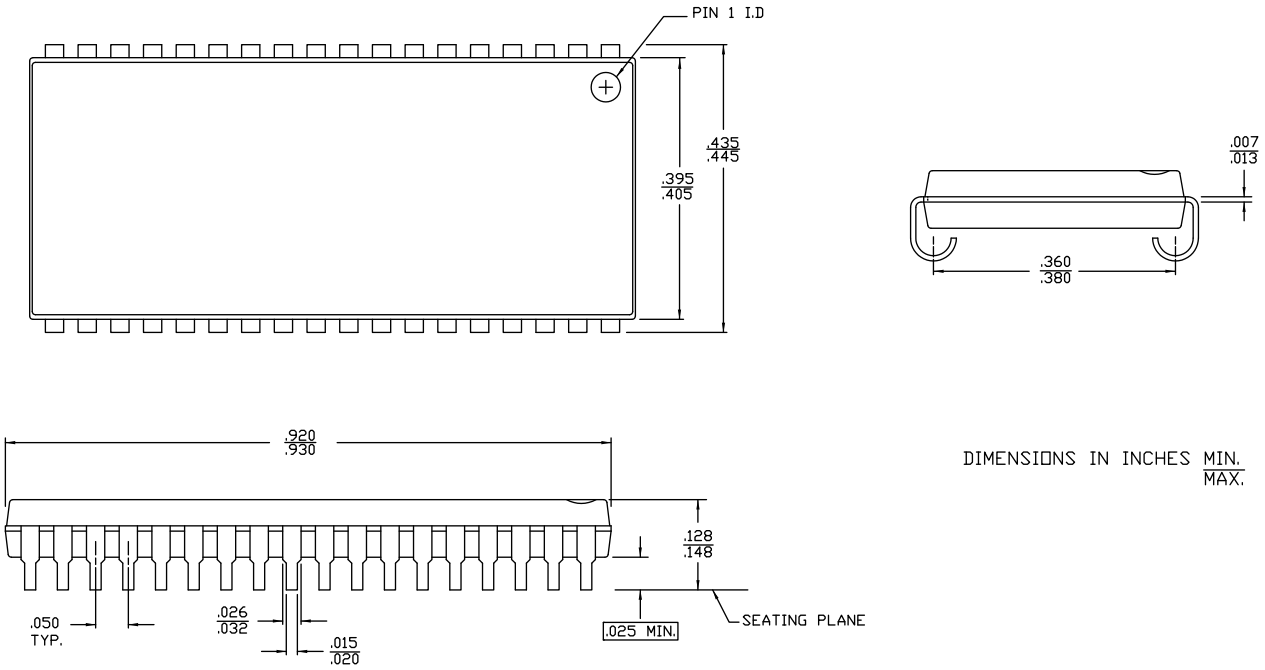
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
17	CY7C1049BNL-17VC	51-85090	36-pin (400-Mil) Molded SOJ	Commercial

Ordering Code Definitions



Package Diagram

Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1049BN, 512 K × 8 Static RAM Document Number: 001-76449				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3539227	TAVA	03/01/2012	New data sheet.
*A	4371513	VINI	05/06/2014	Updated Switching Waveforms: Added Note 18 and referred the same note in Figure 8. Updated to new template. Completing Sunset Review.
*B	4573121	VINI	11/18/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*C	4765735	VINI	05/14/2015	Updated Package Diagram: spec 51-85090 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*D	6012105	AESATP12	01/03/2018	Updated logo and copyright.

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