

## Evaluating the **ADM2461E** 500 kbps, 5.7 kV RMS, Signal Isolated, Half-Duplex RS-485 Transceiver with $\pm 15$ kV IEC ESD

### FEATURES

- Simplified evaluation of the **ADM2461E** signal isolated 500 kbps half-duplex RS-485 transceiver
- 2-layer PCB compliant with EN 55032 Class B radiated emissions
- Footprint for standard half-duplex, 16-lead, SOIC\_W package with 8.0 mm creepage and clearance
- 2 on-board **ADP7104** LDO regulators with jumper options for simplified evaluation in multiple supply configurations
- Jumper options to utilize flexible,  $V_{DD1}$  low voltage supply rail for interfacing with I/O nodes as low as 1.7 V
- SMA connector for Tx/D input signal
- Optional on-board **LTC1799** oscillator for providing Tx/D signal
- Screw terminal blocks for connecting power, digital, and RS-485 signals

- Jumper selectable enable and disable for digital input signals
- Resistors and footprints for termination
- Test points for measuring all signals

### EVALUATION KIT CONTENTS

EVAL-ADM2461EEBZ

### EQUIPMENT NEEDED

- Oscilloscope
- Signal generator
- 3 V to 5.5 V supply
- 1.7 V to 5.5 V supply

### DOCUMENTS NEEDED

**ADM2461E** data sheet

### EVAL-ADM2461EEBZ EVALUATION BOARD PHOTOGRAPH

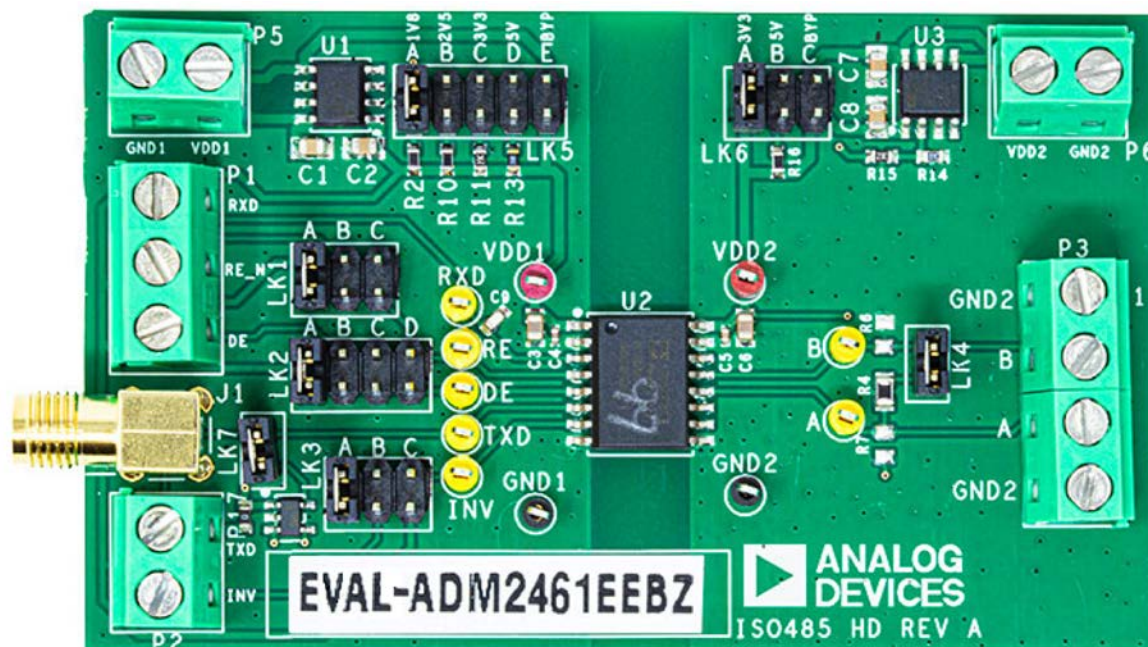


Figure 1.

22798-001

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REVISION HISTORY

6/2020—Revision 0: Initial Version

## GENERAL DESCRIPTION

The EVAL-ADM2461EEBZ allows for the simplified, efficient evaluation of the [ADM2461E](#) 500 kbps, 5.7 kV rms, signal isolated, half-duplex, RS-485 transceiver.

The EVAL-ADM2461EEBZ comes with options for the evaluation of the [ADM2461E](#) in an individual system. Digital and RS-485 bus signals are easily accessible via the screw terminal blocks on the EVAL-ADM2461EEBZ. Each digital input can be configured via the on-board jumper options.

Two on-board [ADP7104](#) low dropout (LDO) regulators accept an input voltage up to 20 V and output a range of selectable supply voltages to the  $V_{DD1}$  pin and  $V_{DD2}$  pin, which are configurable via jumper options. The LDO regulators can be bypassed to power the [ADM2461E](#)  $V_{DD1}$  supply pin and  $V_{DD2}$  supply pin directly from an external power supply.

The flexible  $V_{DD1}$  pin primary side logic supply allows the device to operate with a digital input/output (I/O) voltage of 1.7 V to 5.5 V, which enables communication with modern nodes using

either a 1.8 V or 2.5 V power supply. The  $V_{DD1}$  pin can also be supplied from the [ADP7104](#) regulated supply.

Alternative methods can be used to provide the transmit data input (TxD) signal to the [ADM2461E](#). An optional [LTC1799](#) oscillator is included on the EVAL-ADM2461EEBZ and can be configured to provide a clock signal as the TxD digital input within a 10 kHz to 250 kHz range. A terminal block allows an easy wired connection to a microcontroller or processor. For optimal signal integrity, use the on-board Subminiature Version A (SMA) connector to connect an external data signal.

The EVAL-ADM2461EEBZ has a footprint for the [ADM2461E](#) isolated, half-duplex RS-485 transceiver in a 10.10 mm × 10.65 mm, 16-lead, standard small outline, wide body (SOIC\_W) package.

For full details on the [ADM2461E](#), see the [ADM2461E](#) data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADM2461EEBZ.

## EVALUATION BOARD HARDWARE

### SETTING UP THE EVALUATION BOARD

The EVAL-ADM2461EEBZ is an isolated RS-485 transceiver, which requires a power supply on both sides of the [ADM2461E](#). The [ADM2461E](#) is powered via the VDD1 and VDD2 connections on the P5 and P6 screw terminal connectors. The supply voltages connected to these terminals can either be regulated or connected directly to the V<sub>DD1</sub> pin and V<sub>DD2</sub> pin of the [ADM2461E](#). Insert the LK5 jumper into Position E to power the V<sub>DD1</sub> pin directly from the VDD1 connector on P5. Insert the LK6 jumper into Position C to power the V<sub>DD2</sub> pin directly from the VDD2 terminal on P6.

The two on-board [ADP7104](#) voltage regulators can be configured to provide a range of regulated supply voltages to the V<sub>DD1</sub> pin and V<sub>DD2</sub> pin of the [ADM2461E](#). Various voltage options can be selected using the LK5 and LK6 jumpers. The V<sub>DD1</sub> pin is fitted with a 10  $\mu$ F decoupling capacitor (C3) and a 0.1  $\mu$ F decoupling capacitor (C4). The V<sub>DD2</sub> pin is fitted with a 10  $\mu$ F decoupling capacitor (C6) and a 0.1  $\mu$ F decoupling capacitor (C5). See Table 1, Table 2, and Table 3 for more details on the jumper and power supply connections. The corresponding labeled test points allow for monitoring of the EVAL-ADM2461EEBZ VDD1 and VDD2 supply voltages.

### INPUT AND OUTPUT CONNECTIONS

Digital input and output signals are connected via the P1 and P2 screw terminal blocks to allow wire connections from the EVAL-ADM2461EEBZ to a signal generator or microcontroller. The EVAL-ADM2461EEBZ includes screw terminals for the receiver data output (RxD), receiver enable (RE), and driver enable (DE) on P1, and screw terminals for TxD and the cable invert (INV) function on P2.

Alternatively, jumper connections can connect these signals to the V<sub>DD1</sub> pin or GND<sub>1</sub> pins of the [ADM2461E](#) (see Table 1).

Connections to the RS-485 bus are made via the P3 screw terminal block. The EVAL-ADM2461EEBZ has two bus signals, Pin A and Pin B, for the noninverting input and output signal and the inverting input and output signal, respectively. The common ground connection of the RS-485 bus can be connected to the P3 screw terminal block of the EVAL-ADM2461EEBZ. Test points are available on the EVAL-ADM2461EEBZ and are appropriately labeled for all digital and bus signals.

### RADIATED EMISSIONS

The [ADM2461E](#) encodes data across the isolation barrier using an amplitude shift keying (ASK) modulation scheme, which is optimized for both high noise immunity and minimal radiated emissions. The EVAL-ADM2461EEBZ is a 2-layer printed circuit board (PCB) that meets the EN 55032 Class B radiated emissions requirements under full load while operating at a maximum data rate of 500 kbps. To maximize the margin to the EN 55032 Class B specification, adhere to the following guidelines:

- Place a 0.1  $\mu$ F capacitor (C4) between the V<sub>DD1</sub> pin and the GND<sub>1</sub> pin (Pin 2).
- Place a 0.1  $\mu$ F capacitor (C5) between the V<sub>DD2</sub> pin and GND<sub>1</sub> pin (Pin 15).
- Ensure that the decoupling capacitors are placed as close as possible to the corresponding [ADM2461E](#) pins.

The EVAL-ADM2461EEBZ, designed according to these guidelines, meets EN 55032 and CISPR32 Class B requirements with margin.

**Table 1. Jumper Configurations**

Link	Jumper Connection	Description
LK1	A	Connects the <a href="#">ADM2461E</a> $\overline{\text{RE}}$ input pin to the V <sub>DD1</sub> pin. This setting disables the receiver.
	B	Connects the <a href="#">ADM2461E</a> $\overline{\text{RE}}$ input pin to the $\overline{\text{RE}}$ terminal on the P1 connector.
	C	Connects the <a href="#">ADM2461E</a> $\overline{\text{RE}}$ input pin to the GND <sub>1</sub> pins. This setting enables the receiver.
LK2	A	Connects the <a href="#">ADM2461E</a> DE input pin to the V <sub>DD1</sub> pin. This setting enables the driver.
	B	Connects the <a href="#">ADM2461E</a> DE input pin to the DE terminal on the P1 connector.
	C	Connects the <a href="#">ADM2461E</a> DE input pin to the GND <sub>1</sub> pins. This setting disables the driver.
	D	Connects the <a href="#">ADM2461E</a> DE input pin to the $\overline{\text{RE}}$ input signal. Therefore, the input for both $\overline{\text{RE}}$ and DE is set by the LK1 jumper. This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK3	A	Connects the <a href="#">ADM2461E</a> INV input pin to the GND <sub>1</sub> pins. This setting is used for normal operation.
	B	Connects the <a href="#">ADM2461E</a> INV input pin to the INV terminal on the P2 connector.
	C	Connects the <a href="#">ADM2461E</a> INV input pin to the V <sub>DD1</sub> pin. This setting enables the cable inversion feature.
LK4	Inserted	Connects the 120 $\Omega$ R4 termination resistor across the <a href="#">ADM2461E</a> Pin A and Pin B.
	Not inserted	Disconnects the 120 $\Omega$ R4 termination resistor across the <a href="#">ADM2461E</a> Pin A and Pin B.

Link	Jumper Connection	Description
LK5	A	Configures the <a href="#">ADP7104</a> voltage regulator, U1, to supply a regulated 1.8 V to the <a href="#">ADM2461E</a> V <sub>DD1</sub> pin.
	B	Configures the <a href="#">ADP7104</a> voltage regulator, U1, to supply a regulated 2.5 V to the <a href="#">ADM2461E</a> V <sub>DD1</sub> pin.
	C	Configures the <a href="#">ADP7104</a> voltage regulator, U1, to supply a regulated 3.3 V to the <a href="#">ADM2461E</a> V <sub>DD1</sub> pin.
	D	Configures the <a href="#">ADP7104</a> voltage regulator, U1, to supply a regulated 5 V to the <a href="#">ADM2461E</a> V <sub>DD1</sub> pin.
	E	Bypasses the <a href="#">ADP7104</a> voltage regulator, U1, and powers the <a href="#">ADM2461E</a> V <sub>DD1</sub> supply pin directly from the VDD1 terminal on the P5 connector.
LK6	A	Configures the <a href="#">ADP7104</a> voltage regulator, U3, to supply a regulated 3.3 V to the <a href="#">ADM2461E</a> V <sub>DD2</sub> pin.
	B	Configures the <a href="#">ADP7104</a> voltage regulator, U3, to supply a regulated 5 V to the <a href="#">ADM2461E</a> V <sub>DD2</sub> pin.
	C	Bypasses the <a href="#">ADP7104</a> voltage regulator, U3, and powers the <a href="#">ADM2461E</a> V <sub>DD2</sub> supply pin directly from the VDD2 terminal on the P6 connector.
LK7	Inserted	Connects the output of the <a href="#">LTC1799</a> oscillator to the <a href="#">ADM2461E</a> TxD pin.
	Not inserted	Disconnects the output of the <a href="#">LTC1799</a> oscillator from the <a href="#">ADM2461E</a> TxD pin.

## OTHER BOARD COMPONENTS

The EVAL-ADM2461EEBZ has footprints for an R4 termination resistor. A 120  $\Omega$  termination resistor is fitted to R4 on the EVAL-ADM2461EEBZ, but this resistor can be removed or replaced with a resistor of a different value as needed. Insert the LK4 jumper to connect the R4 resistor and add a 120  $\Omega$  load to the RS-485 driver and receiver.

### Biassing Resistors for Bus Idle Fail-Safe

The [ADM2461E](#) has a built in receiver fail-safe for the bus idle condition, but there are footprints on the EVAL-ADM2461EEBZ for fitting an R7 pull-up resistor to the VDD2 supply on Pin A of the [ADM2461E](#), as well as the R6 pull-down resistor to the GND2 supply on Pin B of the [ADM2461E](#). These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in bus idle condition depends on the minimum supply voltage and the termination scheme. For 5 V transceiver operation, 1140  $\Omega$  is recommended. For 3.3 V transceiver operation, 900  $\Omega$  is recommended.

See the [AN-960 Application Note](#) for more information about the bus idle fail-safe.

### On-Board LTC1799 Oscillator

An [LTC1799](#) clock oscillator is provided on the evaluation board to allow evaluation of the [ADM2461E](#) without the need for an external signal source.

To use the [LTC1799](#) oscillator for evaluation, insert the LK7 jumper. This setting connects the oscillator output ([LTC1799](#)) to the [ADM2461E](#) TxD input pin. The sum of the R3 and R12 resistors is used to configure the switching frequency of the clock oscillator within the 100 kHz to 250 kHz range. The frequency is calculated using the following equation:

$$f_{osc} = 10 \text{ MHz} \left( \frac{10 \text{ k}\Omega}{N(R3 + R12)} \right),$$

$$4 \text{ k}\Omega \leq (R3 + R12) \leq 1 \text{ M}\Omega, N = 1, 10$$

The value of N is controlled with the R18 resistor. When R18 is not inserted, N = 10. Insert a 0  $\Omega$  resistor at R18 to set N = 1 for higher frequency operation. The EVAL-ADM2461EEBZ ships with N = 10 and R3 + R12 = 40 k $\Omega$ , which sets the oscillator output frequency to 250 kHz.

The [LTC1799](#) oscillator is powered from the VDD1 supply, and can only be used when the VDD1 supply voltage is between 2.7 V and 5.5 V. By removing the 0  $\Omega$  R17 resistor, the [LTC1799](#) can be disconnected from the VDD1 supply.

### ADP7104 LDO Regulator

The evaluation board features two on-board [ADP7104](#) LDO regulators that allow flexible power supply configurations during evaluation.

The V<sub>DD1</sub> regulator (U1) is powered from the VDD1 terminal on the P5 connector, and is configured using the LK5 jumper. This jumper position selects the regulator output to the V<sub>DD1</sub> pin. Available voltage options are 1.8 V, 2.5 V, 3.3 V, and 5 V. To bypass the V<sub>DD1</sub> regulator (U1) and power the V<sub>DD1</sub> pin directly from the VDD1 terminal, insert the LK5 jumper to Position E.

The V<sub>DD2</sub> regulator (U3) is powered from the VDD2 terminal on the P6 connector, and is configured using the LK6 jumper. This jumper position selects the regulator output to the [ADM2461E](#) V<sub>DD2</sub> pin. Available voltage options are 3.3 V and 5 V. To bypass the V<sub>DD2</sub> regulator (U3) and power the V<sub>DD2</sub> pin directly from the VDD2 terminal, insert the LK6 jumper to Position C.

Table 2 and Table 3 list the supported power supply configurations and the associated jumper configurations.

Table 2. Primary Side Input Supply Configurations

Jumper LK5	V <sub>DD1</sub> Input Voltage Range	V <sub>DD1</sub> Supply
A	2.2 V to 20 V	Regulator provides 1.8 V
B	2.9 V to 20 V	Regulator provides 2.5 V
C	3.7 V to 20 V	Regulator provides 3.3 V
D	5.4 V to 20 V	Regulator provides 5 V
E	1.7 V to 5.5 V	Supplied directly from the VDD1 terminal on P5

Table 3. Secondary Side Input Supply Configurations

Jumper LK6	V <sub>DD2</sub> Input Voltage Range	V <sub>DD2</sub> Supply
A	3.7 V to 20 V	Regulator provides 3.3 V
B	5.4 V to 20 V	Regulator provides 5 V
C	3 V to 5.5 V	Supplied directly from the VDD2 terminal on P6

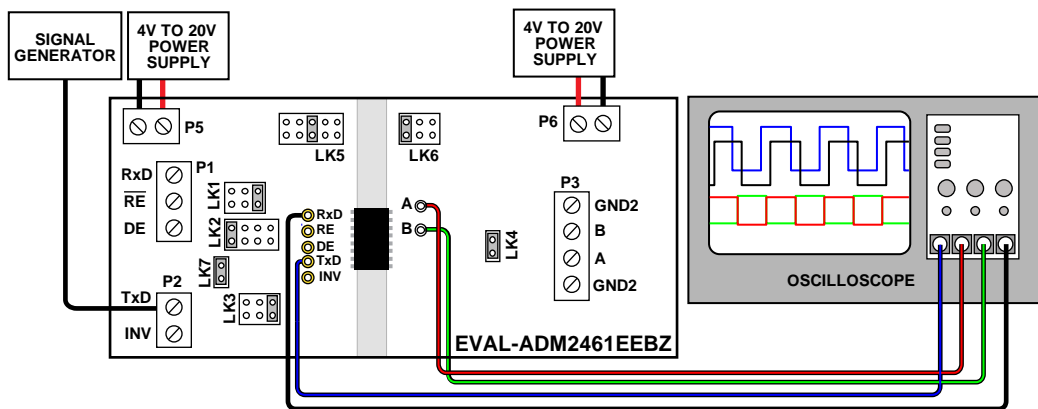


Figure 2. Half-Duplex RS-485 Loopback Test

# HALF-DUPLEX RS-485 TRANSCEIVER LOOPBACK TEST

A loopback test can be set up with the EVAL-ADM2461EEBZ. The [ADM2461E](#) is a half-duplex RS-485 transceiver within which the transmitter and receiver are connected together. In a half-duplex device, when both the driver and receiver are enabled, data applied to the TxD input pin of the [ADM2461E](#) is transmitted by the driver and then received on the RxD output pin of the [ADM2461E](#). This loopback configuration evaluates both the transmitter and receiver of the [ADM2461E](#) on the evaluation board.

The details of this loopback test are shown in Table 1 and in Figure 2. A signal generator is connected to the TxD pin, which allows verification of the bus signals and the receiver output. Note that during the test, the jumper position for LK1 is Position C, LK2 is Position A, and LK3 is Position A. See Table 2 for the jumper configurations for different power supply configurations. Insert the LK4 jumper to terminate the transmitter and receiver with a 120  $\Omega$  resistor.

# IEC 61000-4-2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The EVAL-ADM2461EEBZ is tested and verified to achieve protection against IEC 61000-4-2 ESD to  $\pm 12$  kV (contact discharge) and  $\pm 15$  kV (air discharge) on the [ADM2461E](#) Pin A and Pin B.

The IEC 61000-4-2 ESD standard describes testing using two coupling methods known as contact discharge and air discharge. Contact discharge implies direct contact between the discharge gun and the equipment under test (EUT). The [ADM2461E](#) is tested using both of these methods.

During testing, the [ADM2461E](#) Pin A and Pin B are subjected to at least 10 positive and 10 negative single discharges with a 1 sec interval between each pulse. The highest specified IEC 61000-4-2 ESD test is Level 4, which defines a contact discharge voltage of  $\pm 8$  kV and an air discharge voltage of  $\pm 15$  kV. The [ADM2461E](#) meets or exceeds these ratings. See the [ADM2461E](#) data sheet for ESD details.



## EVALUATION BOARD SCHEMATICS AND ARTWORK

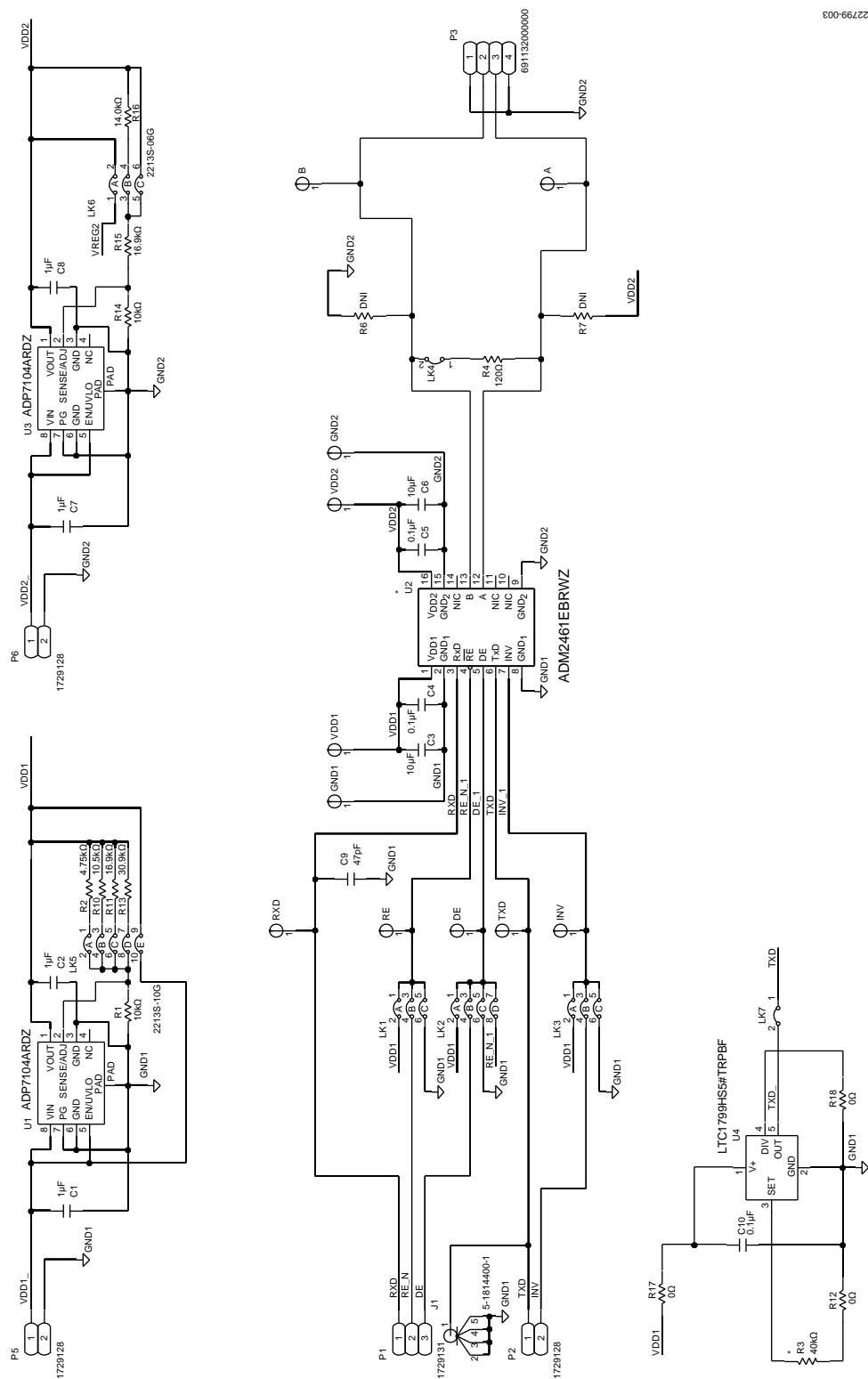


Figure 3. EVAL-ADM2461EEBZ Schematic

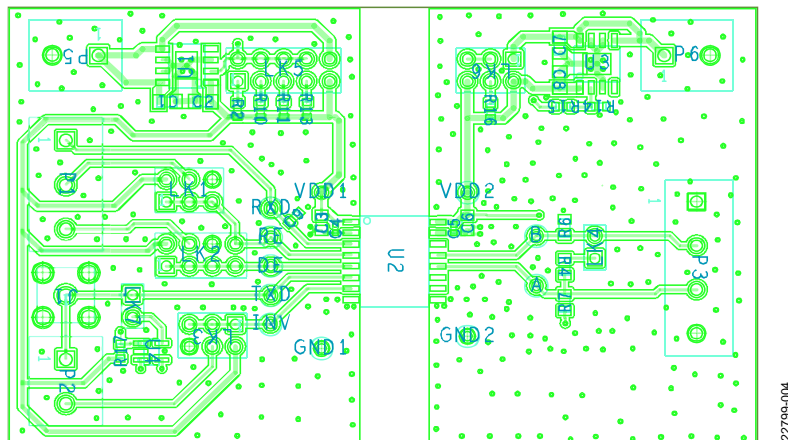


Figure 4. EVAL-ADM2461EEBZ Component Side, Layer 1

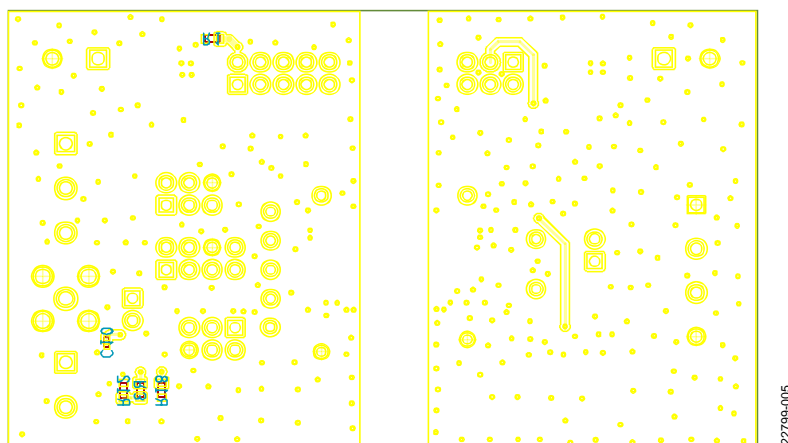


Figure 5. EVAL-ADM2461EEBZ, Layer 2

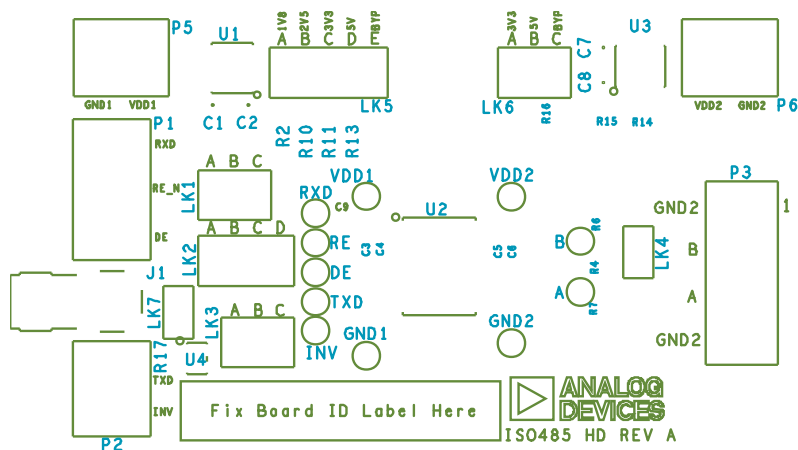


Figure 6. EVAL-ADM2461EEBZ, Silkscreen



## ORDERING INFORMATION

## BILL OF MATERIALS

Table 4. EVAL-ADM2461EEBZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
7	A, B, DE, INV, RE, RxD, TxD	Test points, yellow	Keystone Electronics	36-5004-ND
3	C4, C5, C10	Capacitors, 0.1 $\mu$ F, 0402	Murata	GRM155R61E104KA87D
4	C1, C2, C7, C8	Capacitors, 1 $\mu$ F, 0805	Murata	GCM21BR71E105KA56L
2	C3, C6	Capacitors, 10 $\mu$ F, 0805	TDK	C2012X5R1E106K085AC
1	C9	Capacitor, 47 pF, 0603	AVX Corporation	06035A470JAT2A
2	GND1, GND2	Test points, black	Components Corporation	TP-105-01-00
1	J1	Coaxial, right angle SMA connector	TE Connectivity	5-1814400-1
3	LK1, LK3, LK6	6-pin (3 $\times$ 2), 0.1 inch headers and shorting blocks	Multicomp	2213S-06G
1	LK2	8-pin (4 $\times$ 2), 0.1 inch header and shorting block	Multicomp	2213S-08G
1	LK5	10-pin (5 $\times$ 2), 0.1 inch header and shorting block	Multicomp	2213S-10G
2	LK4, LK7	2-pin (1 $\times$ 2), 0.1 inch headers and shorting blocks	Harwin	M20-9990246
1	P1	Three position terminal blocks	Phoenix Contact	1729131
3	P2, P5, P6	Two position terminal blocks	Phoenix Contact	1729128
1	P3	Four position terminal blocks	Wurth Electronik	691132000000
2	R12, R17	Resistors, 0 $\Omega$ , 0603	Multicomp	MC0603WG00000T5E-TC
1	R18	Resistor, do not install (DNI), 0603	Not applicable	Not applicable
2	R1, R14	Resistors, 10 k $\Omega$ , 0603	Panasonic	ERJ-3EKF1002V
1	R10	Resistor, 10.5 k $\Omega$ , 0603	Panasonic	ERA-3AEB1052V
2	R11, R15	Resistors, 16.9 k $\Omega$ , 0603	Panasonic	ERJ-3EKF1692V
1	R13	Resistor, 30.9 k $\Omega$ , 0603	Panasonic	ERJ-3EKF3092V
1	R16	Resistor, 14 k $\Omega$ , 0603	Panasonic	ERJ-3EKF1402V
1	R2	Resistor, 4.75 k $\Omega$ , 0603	Panasonic	ERJ-3EKF4751V
1	R3	Resistor, 40 k $\Omega$ , 0603	Vishay	CRCW060340K0FKEA
2	R6, R7	Resistors, DNI, 0805	Not applicable	Not applicable
1	R4	Resistors, 120 $\Omega$ , 0805	Panasonic	ERJ-P6WF1200V
2	U1, U3	Low noise CMOS LDOs	Analog Devices, Inc.	<a href="#">ADP7104ARDZ-R7</a>
1	U2	500 kbps, 5.7 kV signal isolated RS-485 transceiver	Analog Devices	<a href="#">ADM2461EEBZ</a>
1	U4	1 kHz to 33 MHz oscillator	Analog Devices	<a href="#">LTC1799HS5#TRPBF</a>
2	VDD1, VDD2	Test points, red	Components Corporation	TP-105-01-02

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

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