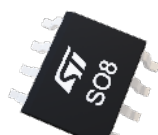


Low power, 1.7 MHz, rail-to-rail output, 36 V operational amplifier



MiniSO8



SO8



DFN8 (3 x 3 mm)
Wettable flanks

Features

- Low offset voltage: 1 mV max. @ 25 °C
- Low current consumption: 375 μ A max. / operator @ 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 1.7 MHz
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage includes ground
- High ESD tolerance: 4 kV HBM
- EMI hardened
- Extended temperature range: -40 to 125 °C
- Automotive qualification
- Micropackage: SO8, MiniSO8, DFN8 3x3 Wettable flanks

Maturity status link

[TSB622](#)

Related products

TSB612	For lower speed
TSB572	For higher speed and rail-to-rail inputs
TSB712	For a higher precision and speed

Applications

- Industrial
- Power supplies
- Automotive

Description

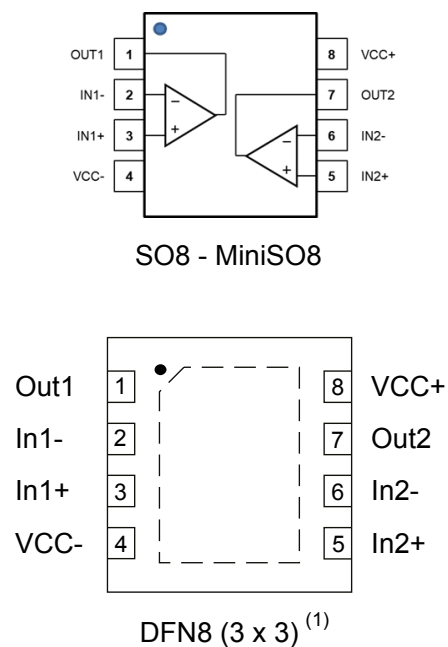
The [TSB622](#) is a general purpose dual operational amplifier featuring an extended supply voltage operating range and rail-to-rail output. It also offers an excellent speed/power consumption ratio with 1.7 MHz gain bandwidth product while consuming less than 375 μ A per operator at 36 V supply voltage.

The [TSB622](#) operates over a wide temperature range from -40 °C to 125 °C making this device ideal for industrial and automotive applications with the associated qualification.

Thanks to its small package size, the [TSB622](#) can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin connections

Figure 1. Pin connections (top view)



⁽¹⁾ Exposed pad can be left floating or connected to ground.

Table 1. Pin description

Pin n°	Pin name	Description
1	OUT1	Output
2	IN1 -	Negative input voltage
3	IN1 +	Positive input voltage
4	VCC -	Negative supply voltage
5	IN2 +	Positive input voltage
6	IN2 -	Negative input voltage
7	OUT2	Output
8	VCC +	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	40	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	V
V_{in}	Input voltage	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V
I_{in}	Input current ⁽³⁾	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	150	°C
R_{th-jc}	Thermal resistance junction to ambient ^{(4) (5)}		°C/W
	SO8	125	
	MiniSO8	190	
	DFN8 3x3 WF	40	
ESD	Human Body Model (HBM) ⁽⁶⁾	4000	V
	Machine Model (MM) ⁽⁷⁾	200	
	Charged Device Model (CDM) ⁽⁸⁾	1500	

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. Input current must be limited by a resistor in series with the inputs.
4. R_{th} are typical values.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. According to JEDEC standard JESD22-A114F.
7. According to JEDEC standard JESD22-A115A.
8. According to ANSI/ESD STM5.3.1.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 36	V
V_{icm}	Common mode voltage on input pins	$(V_{CC-}) - 0.1$ to $(V_{CC+}) - 1$	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4. Electrical characteristics $V_{CC+} = 2.7\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V _{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
Δ V _{IO} /ΔT	Input offset voltage drift	Tmin < T < Tmax		2		μV/°C
I _{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I _{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log (ΔV _{icm} /ΔV _{io})	V _{icm} = - 0.1 to V _{CC} -1 V, V _{OUT} = V _{CC} /2	90	115		dB
		Tmin < T < Tmax	85			
A _{VD}	Large signal voltage gain	V _{OUT} = 0.5 V to (V _{CC} -0.5 V)	90	105		dB
		Tmin < T < Tmax	82			
V _{OH}	High-level output voltage, V _{OH} = V _{CC} - V _{OUT}	T = 25 °C		35	46	mV
		Tmin < T < Tmax			55	
V _{OL}	Low-level output voltage	T = 25 °C		50	60	
		Tmin < T < Tmax			75	
I _{OUT}	I _{sink}	V _{OUT} = V _{CC}	20	27		mA
		Tmin < T < Tmax	10			
	I _{source}	V _{OUT} = 0 V	20	28		
		Tmin < T < Tmax	8			
I _{CC}	Supply current (per channel)	No load, V _{OUT} = V _{CC} /2		280	330	μA
		Tmin < T < Tmax			400	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 100 pF	1	1.45		MHz
		Tmin < T < Tmax	0.7			
Φ _m	Phase margin	R _L = 10 kΩ, C _L = 100 pF		60		degrees
G _m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.30	0.53		V/μs
		Tmin < T < Tmax	0.20			
E _N	Equivalent input noise voltage	f = 1 kHz		30		nV/√Hz
THD+N	Total harmonic distortion + noise	f _{in} = 1 kHz, Gain = 1, R _L = 100 kΩ, V _{icm} = (V _{CC} -1 V) / 2, BW = 22 kHz, V _{OUT} = 1 Vpp		0.005		%
C _S	Channel separation	f = 1 kHz		120		dB
t _{rec}	Overload recovery time			2		μs

Table 5. Electrical characteristics $V_{CC+} = 12\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V _{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
Δ V _{IO} /ΔT	Input offset voltage drift	Tmin < T < Tmax		2		μV/°C
I _{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I _{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log (ΔV _{icm} /ΔV _{io})	V _{icm} = - 0.1 to V _{CC} -1 V, V _{OUT} = V _{CC} /2	100	130		dB
		Tmin < T < Tmax	95			
A _{VD}	Large signal voltage gain	V _{OUT} = 0.5 V to (V _{CC} -0.5 V)	98	115		dB
		Tmin < T < Tmax	90			
V _{OH}	High-level output voltage, V _{OH} = V _{CC} - V _{OUT}	T = 25 °C		68	80	mV
		Tmin < T < Tmax			95	
V _{OL}	Low-level output voltage	T = 25 °C		86	100	
		Tmin < T < Tmax			125	
I _{OUT}	I _{sink}	V _{OUT} = V _{CC}	25	35		mA
		Tmin < T < Tmax	10			
	I _{source}	V _{OUT} = 0 V	30	37		
		Tmin < T < Tmax	15			
I _{CC}	Supply current (per channel)	No load, V _{OUT} = V _{CC} /2		295	345	μA
		Tmin < T < Tmax			420	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 100 pF	1.1	1.55		MHz
		Tmin < T < Tmax	0.8			
Φ _m	Phase margin	R _L = 10 kΩ, C _L = 100 pF		60		degrees
G _m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.35	0.58		V/μs
		Tmin < T < Tmax	0.20			
E _N	Equivalent input noise voltage	f = 1 kHz		30		nV/√Hz
THD+N	Total harmonic distortion + noise	f _{in} = 1 kHz, Gain = 1, R _L = 100 kΩ, V _{icm} = (V _{CC} -1 V) / 2, BW = 22 kHz, V _{OUT} = 1 Vpp		0.005		%
C _S	Channel separation	f = 1 kHz		120		dB
t _{rec}	Overload recovery time			2		μs

Table 6. Electrical characteristics $V_{CC+} = 36\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V _{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
Δ V _{IO} /ΔT	Input offset voltage drift	Tmin < T < Tmax		2		μV/°C
I _{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I _{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log (ΔV _{icm} /ΔV _{io})	V _{icm} = -0.1 to V _{CC} -1 V, V _{OUT} = V _{CC} /2	105	135		dB
		Tmin < T < Tmax	100			
SVR	Supply voltage rejection ratio: 20 log (ΔV _{CC} /ΔV _{io})	V _{CC} = 4.5 to 36 V, V _{icm} = 0 V	100	124		dB
		Tmin < T < Tmax	95			
A _{VD}	Large signal voltage gain	V _{OUT} = 0.5 V to (V _{CC} -0.5 V)	105	120		dB
		Tmin < T < Tmax	100			
V _{OH}	High-level output voltage, V _{OH} = V _{CC} - V _{OUT}	T = 25 °C		110	140	mV
		Tmin < T < Tmax			180	
V _{OL}	Low-level output voltage	T = 25 °C		125	150	
		Tmin < T < Tmax			195	
I _{OUT}	I _{sink}	V _{OUT} = V _{CC}	35	45		mA
		Tmin < T < Tmax	15			
	I _{source}	V _{OUT} = 0 V	35	45		
		Tmin < T < Tmax	25			
I _{CC}	Supply current (per channel)	No load, V _{OUT} = V _{CC} /2		310	375	μA
		Tmin < T < Tmax			420	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 100 pF	1.2	1.7		MHz
		Tmin < T < Tmax	0.95			
Φ _m	Phase margin	R _L = 10 kΩ, C _L = 100 pF		58		degrees
G _m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.35	0.60		V/μs
		Tmin < T < Tmax	0.25			
E _N	Equivalent input noise voltage	f = 1 kHz		25		nV/√Hz
THD+N	Total harmonic distortion + noise	f _{in} = 1 kHz, Gain = 1, R _L = 100 kΩ, V _{icm} = (V _{CC} - 1 V) / 2, BW = 22 kHz, V _{OUT} = 1 Vpp		0.005		%
C _S	Channel separation	f = 1 kHz		120		dB
t _{rec}	Overload recovery time			2		μs

4 Typical performance characteristics

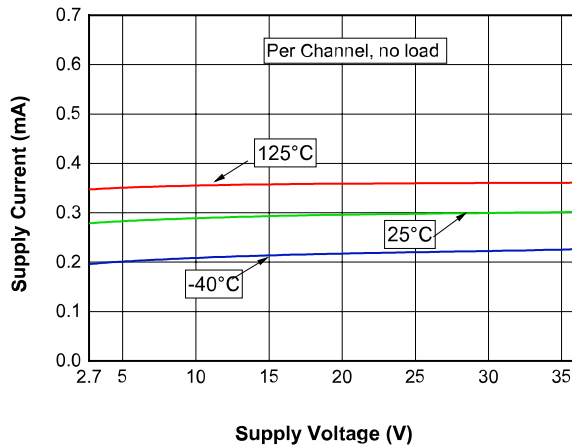
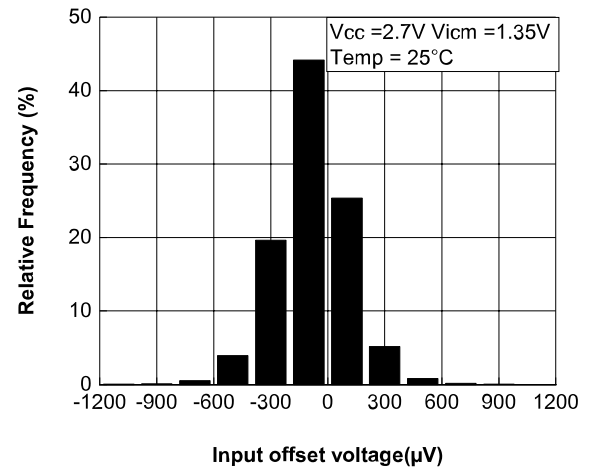
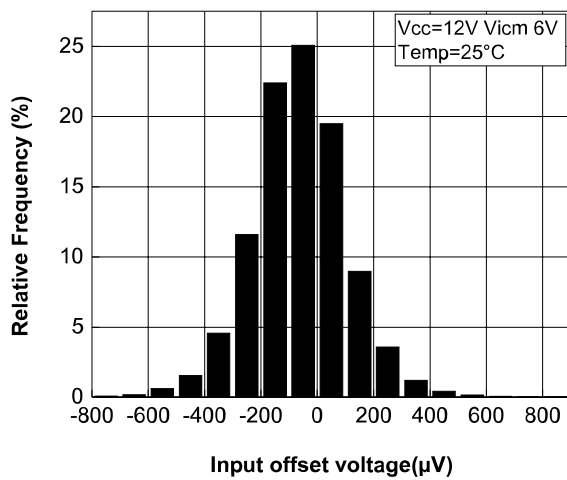
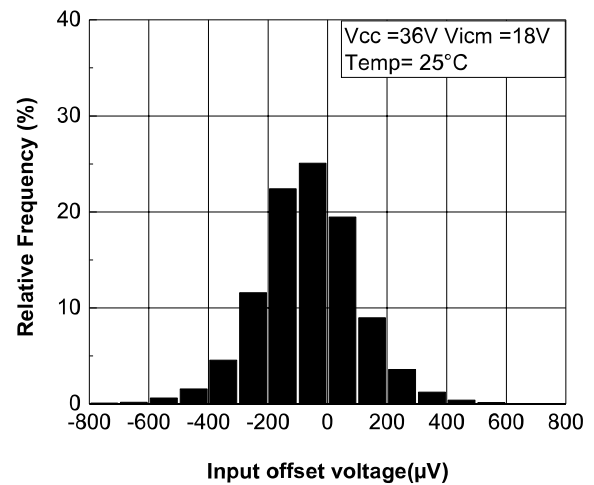
Figure 2. Supply current vs. supply voltage

Figure 3. Input offset voltage distribution at $V_{CC} = 2.7\text{ V}$

Figure 4. Input offset voltage distribution at $V_{CC} = 12\text{ V}$

Figure 5. Input offset voltage distribution at $V_{CC} = 36\text{ V}$


Figure 6. Input offset voltage vs. temperature at $V_{CC} = 36\text{ V}$

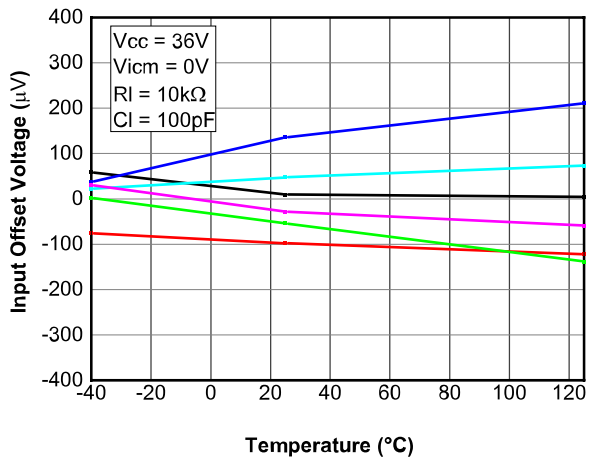


Figure 7. Input offset voltage temperature variation distribution at $V_{CC} = 36\text{ V}$

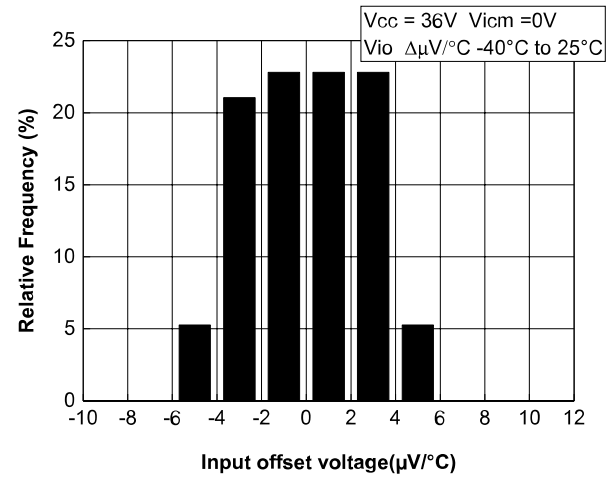


Figure 8. Input offset voltage temperature variation distribution at $V_{CC} = 36\text{ V}$

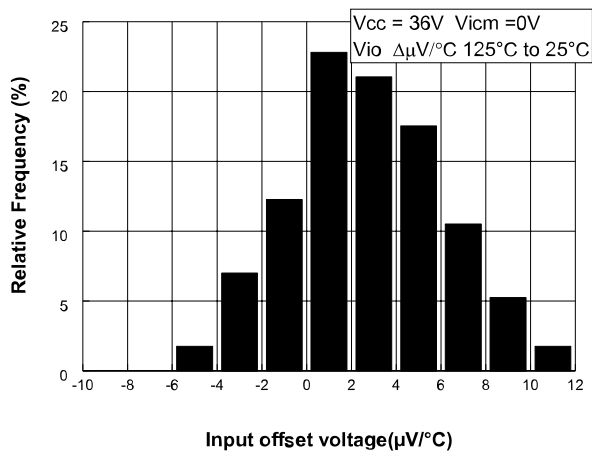


Figure 9. Input offset voltage vs. common-mode voltage at $V_{CC} = 36\text{ V}$

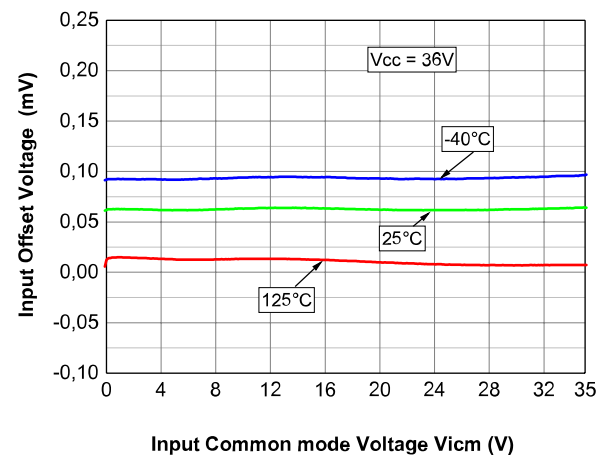


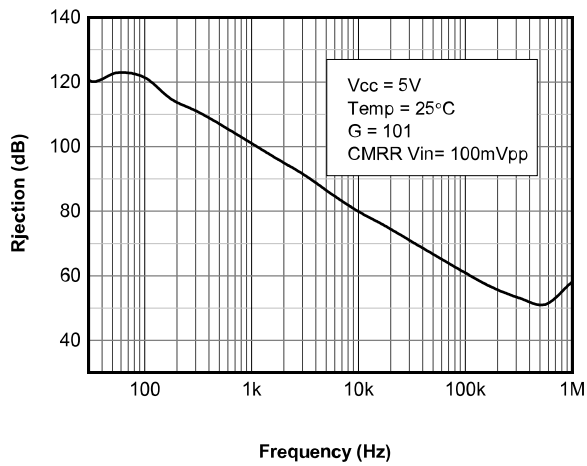
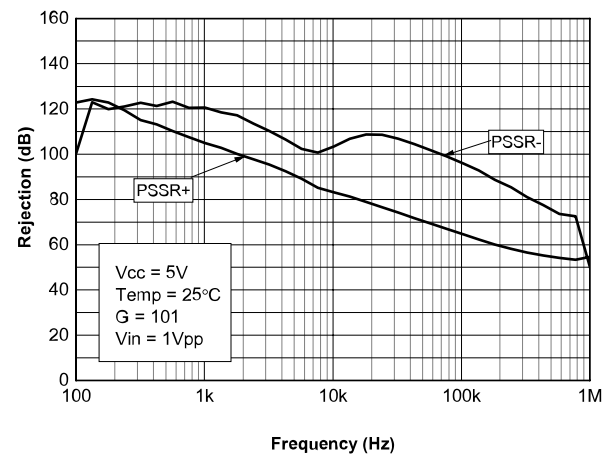
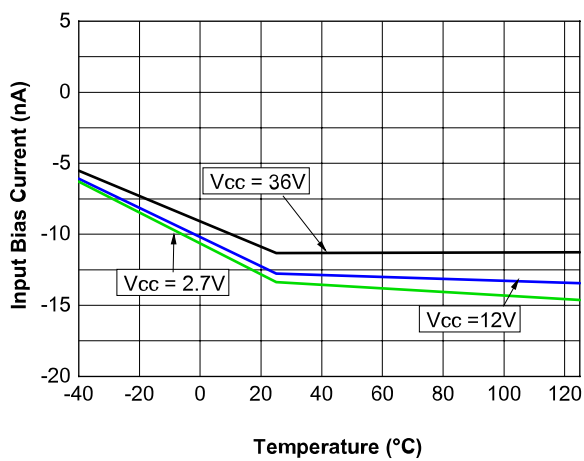
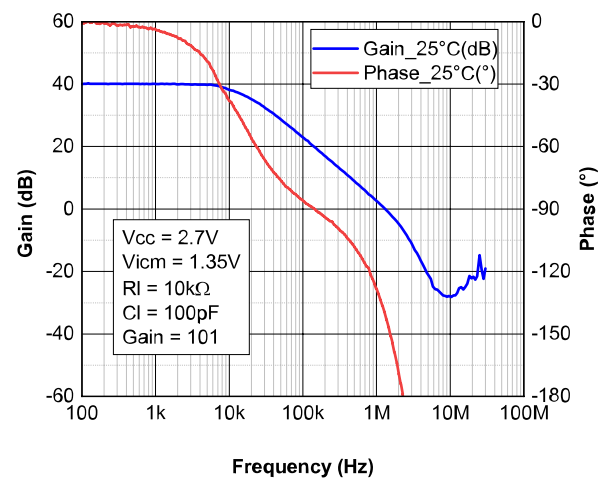
Figure 10. Common-mode reject. ratio CMR at $V_{CC} = 5\text{ V}$

Figure 11. Supply voltage rejection ratio SVR at $V_{CC} = 5\text{ V}$

Figure 12. Input bias current vs. temperature

Figure 13. Bode diagram at $V_{CC} = 2.7\text{ V}$


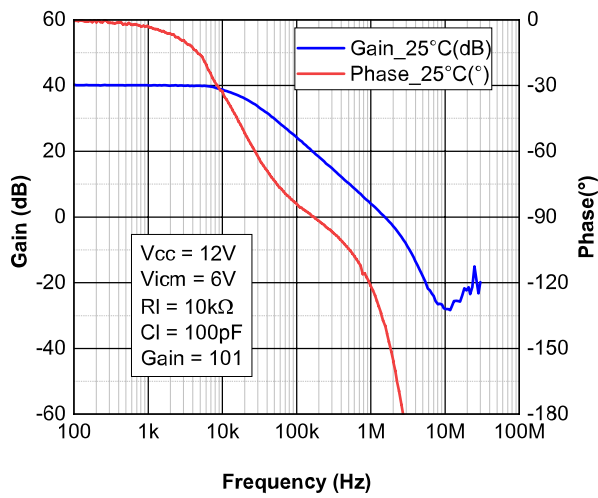
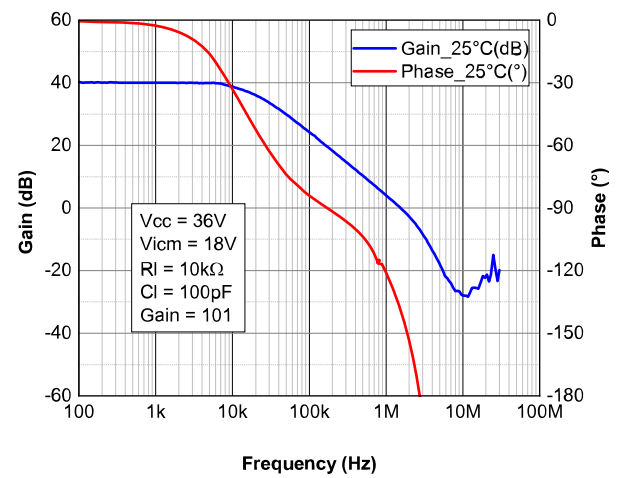
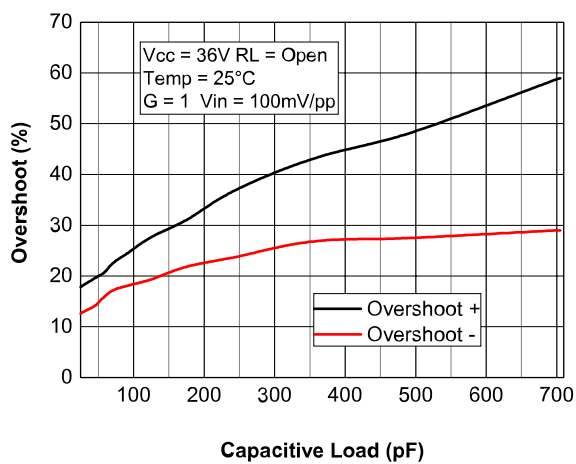
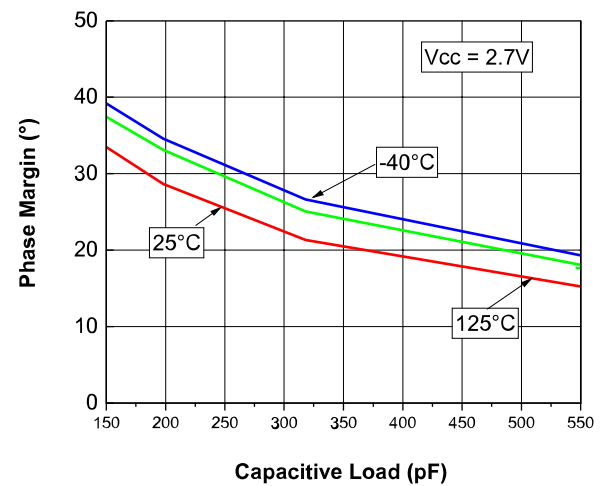
Figure 14. Bode diagram at $V_{CC} = 12\text{ V}$

Figure 15. Bode diagram at $V_{CC} = 36\text{ V}$

Figure 16. Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$

Figure 17. Phase margin vs. capacitive load at $V_{CC} = 2.7\text{ V}$


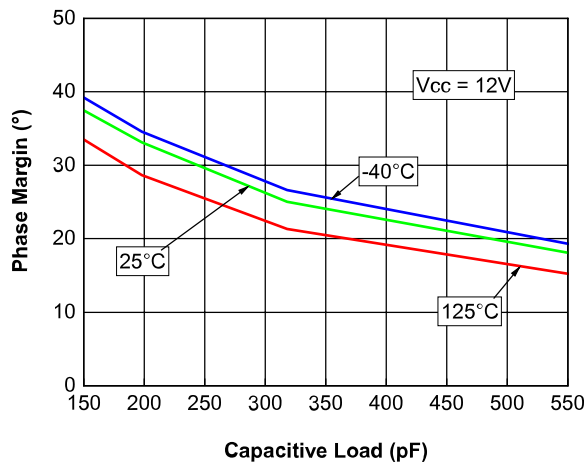
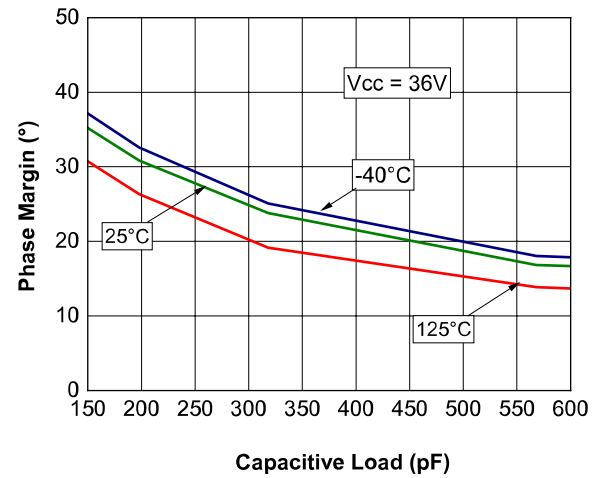
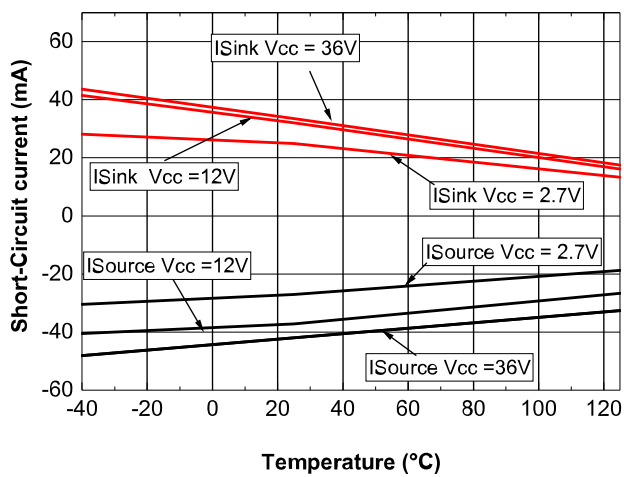
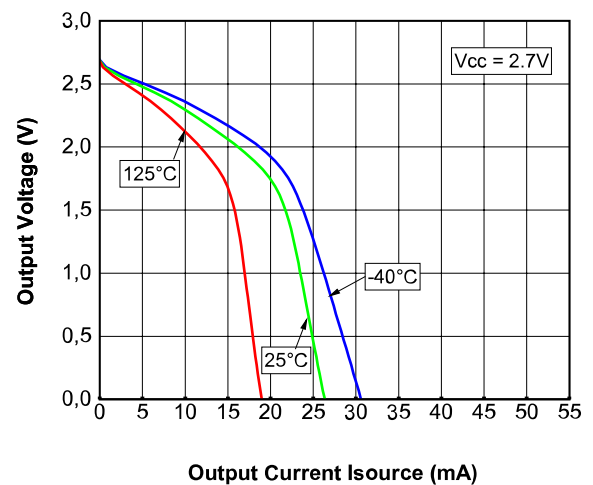
Figure 18. Phase margin vs. capacitive load at $V_{CC} = 12\text{ V}$

Figure 19. Phase margin vs. capacitive load at $V_{CC} = 36\text{ V}$

Figure 20. Short-circuit current vs. temperature

Figure 21. Output source current vs. output voltage at $V_{CC} = 2.7\text{ V}$


Figure 22. Output source current vs. output voltage at $V_{CC} = 12\text{ V}$

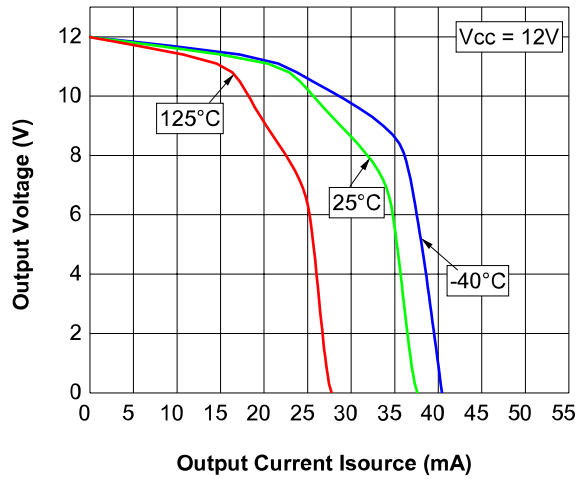


Figure 23. Output source current vs. output voltage at $V_{CC} = 36\text{ V}$

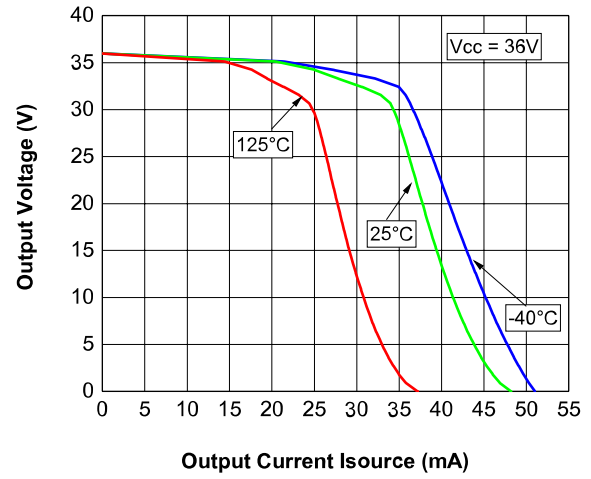


Figure 24. Output sink current vs. output voltage at $V_{CC} = 2.7\text{ V}$

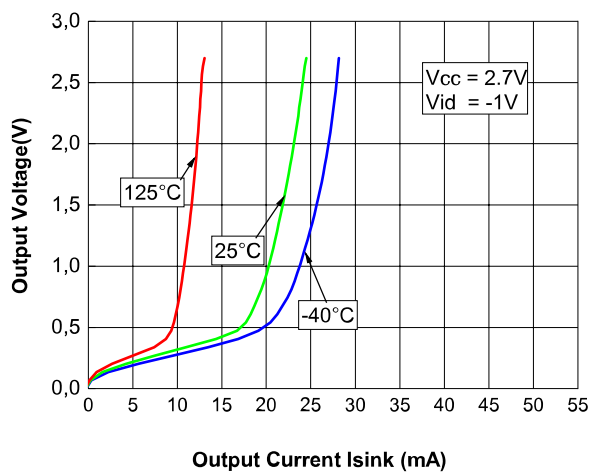


Figure 25. Output sink current vs. output voltage at $V_{CC} = 12\text{ V}$

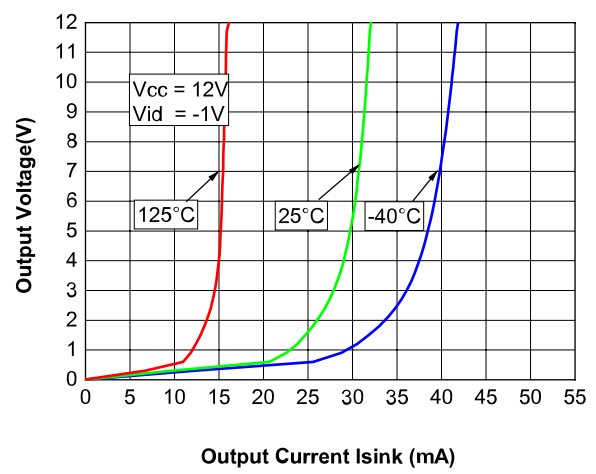


Figure 26. Output sink current vs. output voltage at $V_{CC} = 36\text{ V}$

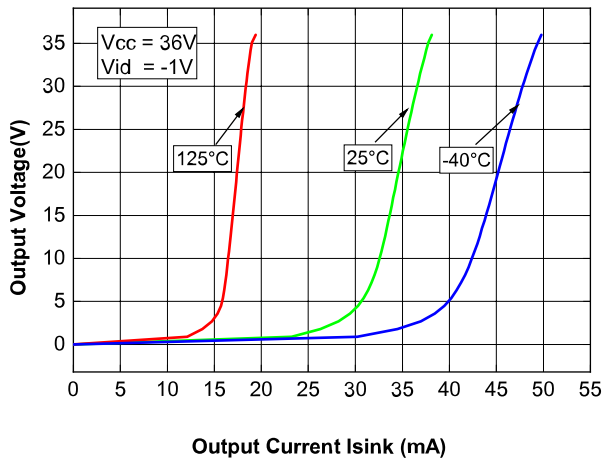


Figure 27. Slew rate at $V_{CC} = 2.7\text{ V}$

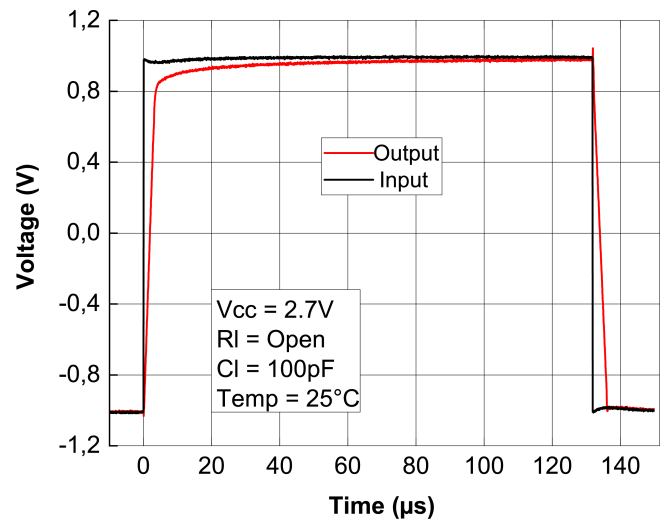


Figure 28. Slew rate at $V_{CC} = 12\text{ V}$

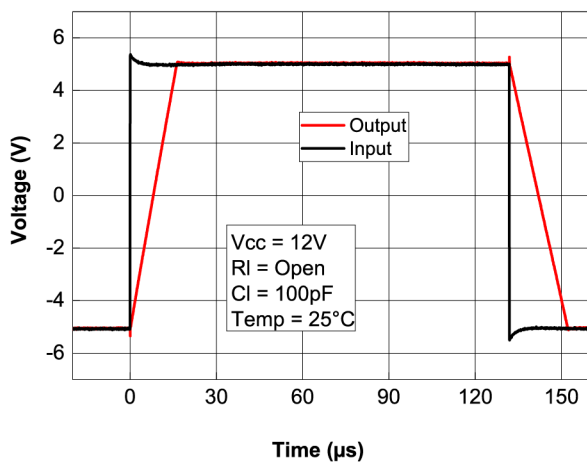


Figure 29. Slew rate at $V_{CC} = 36\text{ V}$

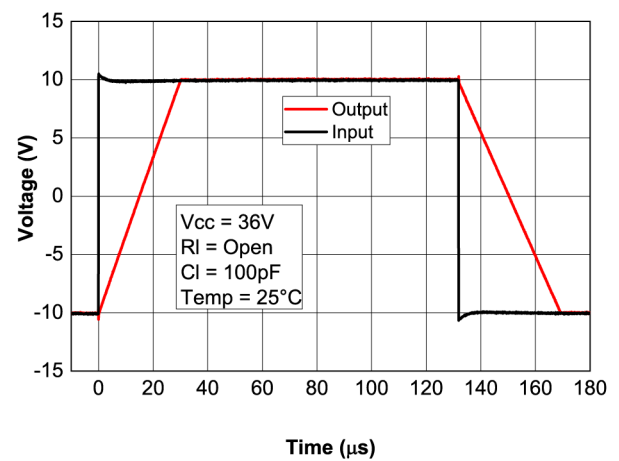


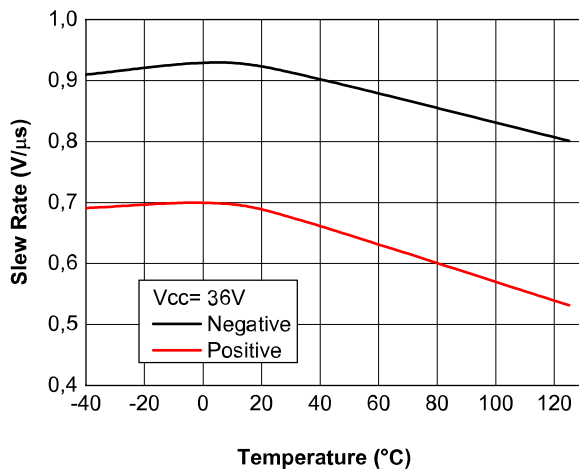
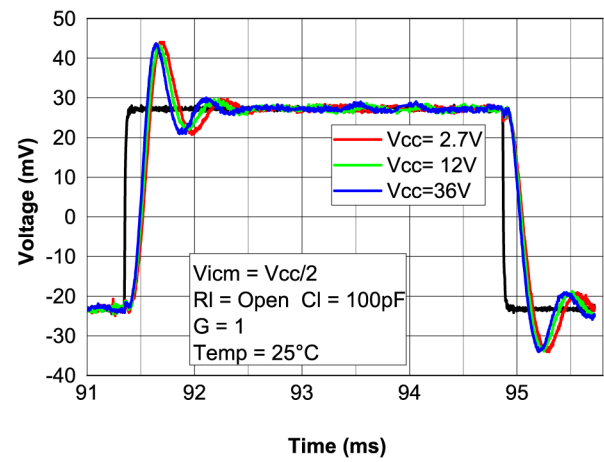
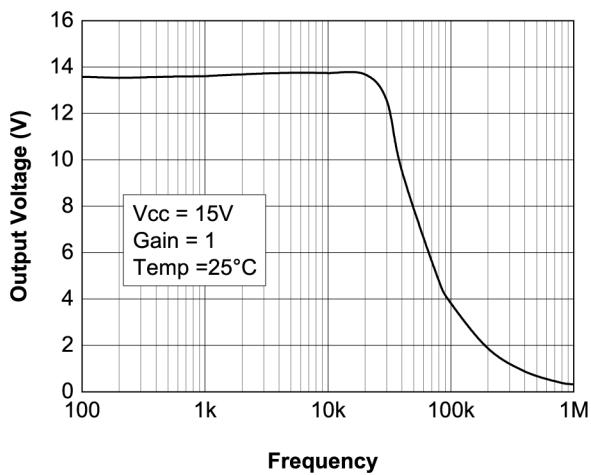
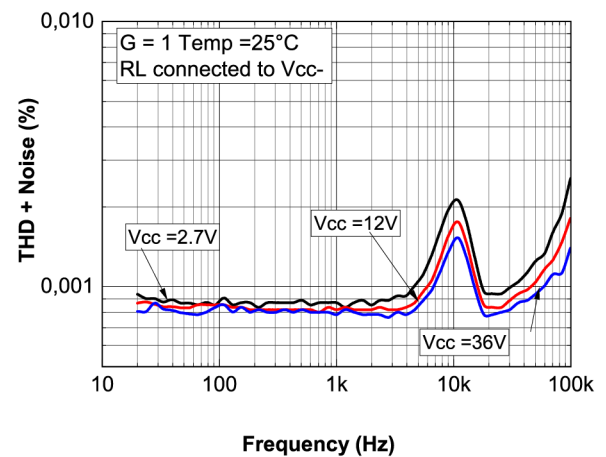
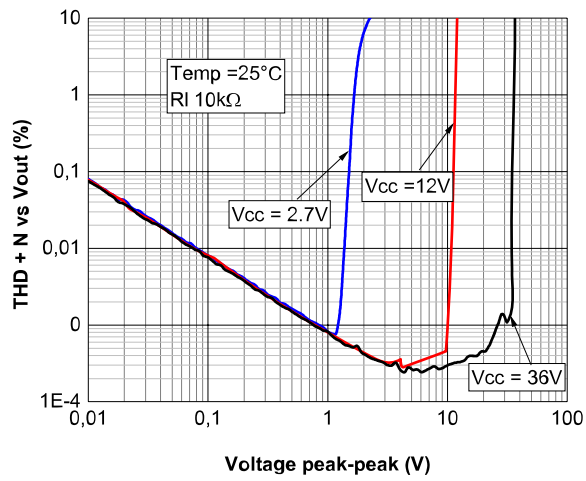
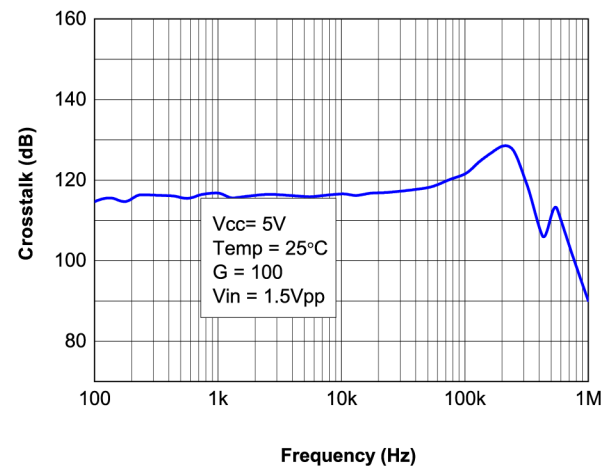
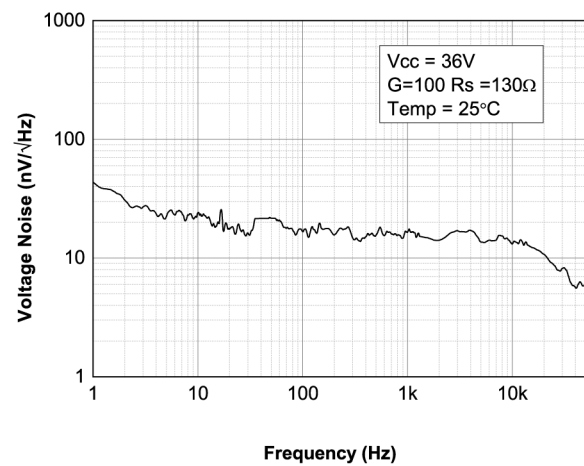
Figure 30. Slew rate vs. temperature at $V_{CC} = 36\text{ V}$

Figure 31. Small signal step response

Figure 32. Maximum output voltage vs. frequency

Figure 33. THD+Noise vs. frequency


Figure 34. THD+Noise vs. output voltage

Figure 35. Cross talk vs. frequency

Figure 36. Equivalent input noise voltage vs. frequency


5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO8 package information

Figure 37. SO8 package outline

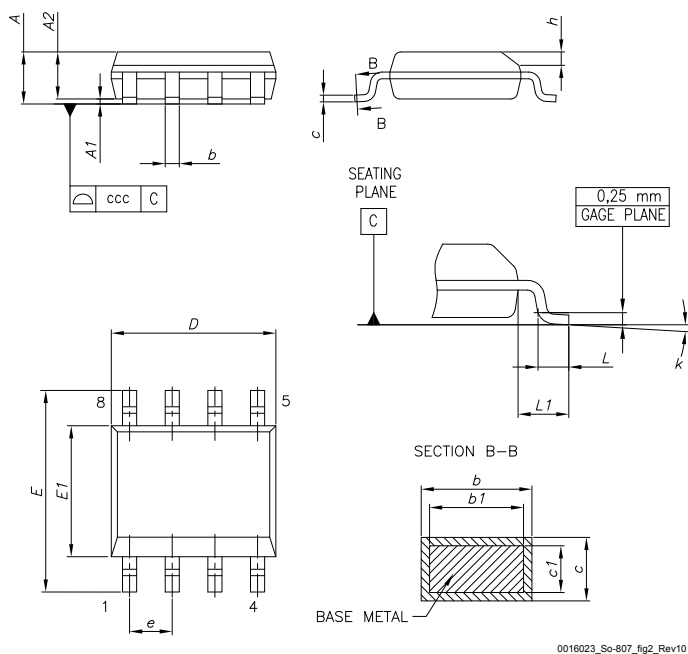


Table 7. SO8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

5.2 MiniSO8 package information

Figure 38. MiniSO8 package outline

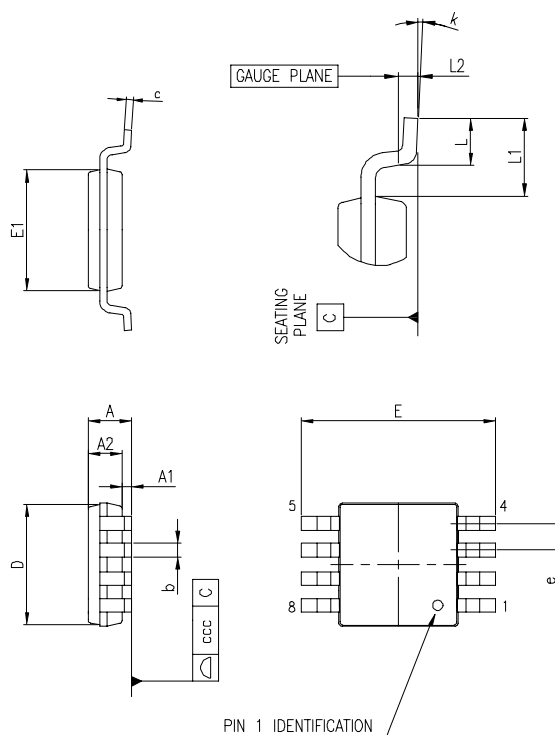


Table 8. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

5.3 DFN8 3x3 package information

Figure 39. DFN8 3x3 package outline and mechanical data

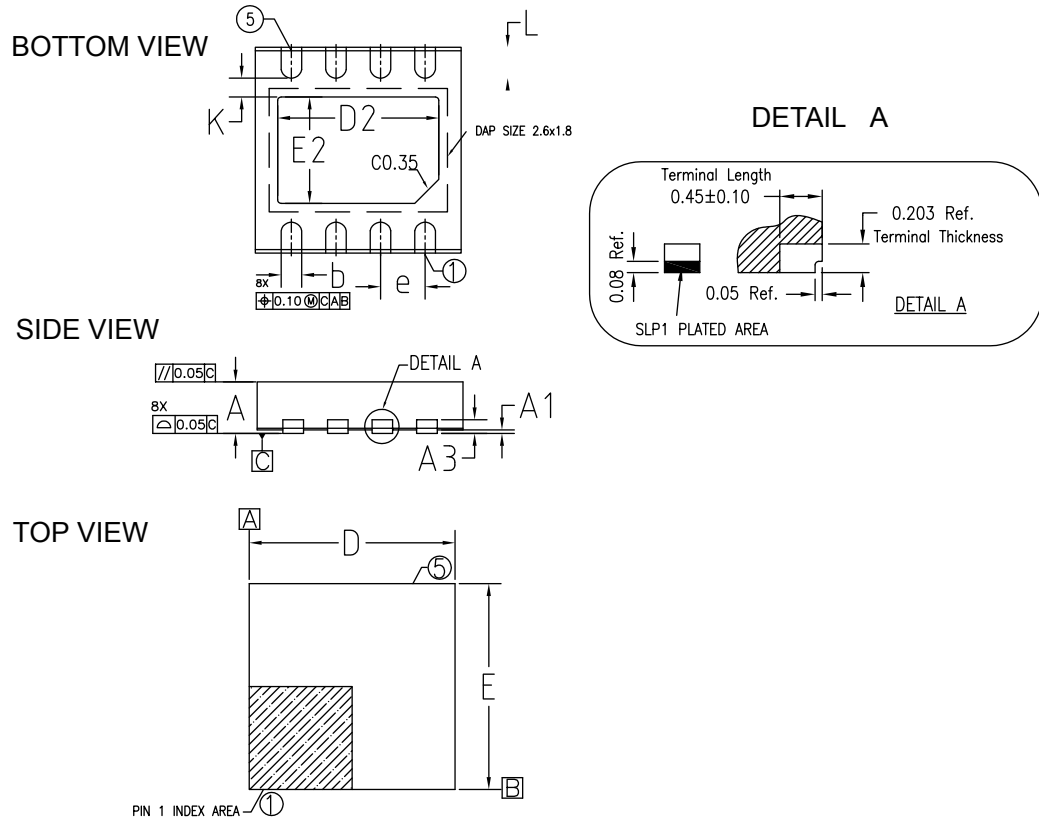
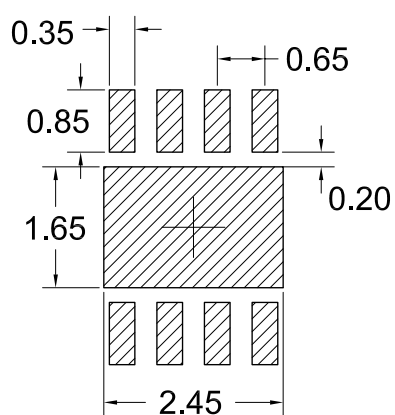


Table 9. DFN8 3x3 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.0		0.05
A3	0.20 Ref.		
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.25	2.35	2.45
e	0.65 BSC		
E	2.95	3.00	3.05
E2	1.45	1.55	1.65
L	0.35	0.45	0.55
K	2.75 Ref.		
N	8		

Figure 40. DFN8 3x3 footprint data



6 Ordering information

Table 10. Order code

Order code	Package	Packaging	Marking
TSB622IDT	SO8	Tape & Reel	TSB622I
TSB622IYDT ⁽¹⁾			TSB622IY
TSB622IST	MiniSO8		K2K
TSB622IYST ⁽¹⁾			K2L
TSB622IQ3T	DFN8 3x3 WF		K2K
TSB622IYQ3T ⁽¹⁾			K2L

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Nov-2021	1	Initial release.
15-Feb-2022	2	Updated Figure 2 .

Contents

1	Pin connections	2
2	Absolute maximum ratings and operating conditions	3
3	Electrical characteristics.....	4
4	Typical performance characteristics	7
5	Package information.....	16
5.1	SO8 package information.....	17
5.2	MiniSO8 package information	18
5.3	DFN8 3x3 package information.....	19
6	Ordering information	21
	Revision history	22

List of tables

Table 1.	Pin description	2
Table 2.	Absolute maximum ratings	3
Table 3.	Operating conditions	3
Table 4.	Electrical characteristics $V_{CC+} = 2.7\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)	4
Table 5.	Electrical characteristics $V_{CC+} = 12\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)	5
Table 6.	Electrical characteristics $V_{CC+} = 36\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)	6
Table 7.	SO8 mechanical data	17
Table 8.	MiniSO8 mechanical data	18
Table 9.	DFN8 3x3 mechanical data	19
Table 10.	Order code	21
Table 11.	Document revision history	22

List of figures

Figure 1.	Pin connections (top view)	2
Figure 2.	Supply current vs. supply voltage	7
Figure 3.	Input offset voltage distribution at $V_{CC} = 2.7\text{ V}$	7
Figure 4.	Input offset voltage distribution at $V_{CC} = 12\text{ V}$	7
Figure 5.	Input offset voltage distribution at $V_{CC} = 36\text{ V}$	7
Figure 6.	Input offset voltage vs. temperature at $V_{CC} = 36\text{ V}$	8
Figure 7.	Input offset voltage temperature variation distribution at $V_{CC} = 36\text{ V}$	8
Figure 8.	Input offset voltage temperature variation distribution at $V_{CC} = 36\text{ V}$	8
Figure 9.	Input offset voltage vs. common-mode voltage at $V_{CC} = 36\text{ V}$	8
Figure 10.	Common-mode reject. ratio CMR at $V_{CC} = 5\text{ V}$	9
Figure 11.	Supply voltage rejection ratio SVR at $V_{CC} = 5\text{ V}$	9
Figure 12.	Input bias current vs. temperature	9
Figure 13.	Bode diagram at $V_{CC} = 2.7\text{ V}$	9
Figure 14.	Bode diagram at $V_{CC} = 12\text{ V}$	10
Figure 15.	Bode diagram at $V_{CC} = 36\text{ V}$	10
Figure 16.	Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$	10
Figure 17.	Phase margin vs. capacitive load at $V_{CC} = 2.7\text{ V}$	10
Figure 18.	Phase margin vs. capacitive load at $V_{CC} = 12\text{ V}$	11
Figure 19.	Phase margin vs. capacitive load at $V_{CC} = 36\text{ V}$	11
Figure 20.	Short-circuit current vs. temperature	11
Figure 21.	Output source current vs. output voltage at $V_{CC} = 2.7\text{ V}$	11
Figure 22.	Output source current vs. output voltage at $V_{CC} = 12\text{ V}$	12
Figure 23.	Output source current vs. output voltage at $V_{CC} = 36\text{ V}$	12
Figure 24.	Output sink current vs. output voltage at $V_{CC} = 2.7\text{ V}$	12
Figure 25.	Output sink current vs. output voltage at $V_{CC} = 12\text{ V}$	12
Figure 26.	Output sink current vs. output voltage at $V_{CC} = 36\text{ V}$	13
Figure 27.	Slew rate at $V_{CC} = 2.7\text{ V}$	13
Figure 28.	Slew rate at $V_{CC} = 12\text{ V}$	13
Figure 29.	Slew rate at $V_{CC} = 36\text{ V}$	13
Figure 30.	Slew rate vs. temperature at $V_{CC} = 36\text{ V}$	14
Figure 31.	Small signal step response	14
Figure 32.	Maximum output voltage vs. frequency	14
Figure 33.	THD+Noise vs. frequency	14
Figure 34.	THD+Noise vs. output voltage	15
Figure 35.	Cross talk vs. frequency	15
Figure 36.	Equivalent input noise voltage vs. frequency	15
Figure 37.	SO8 package outline	17
Figure 38.	MiniSO8 package outline	18
Figure 39.	DFN8 3x3 package outline and mechanical data	19
Figure 40.	DFN8 3x3 footprint data	20

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved