

Features

- Temperature Range
 - Automotive: -40 °C to 125 °C
- High speed
 - $t_{AA} = 15 \text{ ns}$
- Optimized voltage range: 2.5 V to 2.7 V
- Low active power: 220 mW (Max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed/power
- Available in Pb-free and non Pb-free 44-pin TSOP II, 44-pin (400-Mil) Molded SOJ and Pb-free 48-ball FBGA packages

Functional Description

The CY7C1021CV26 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

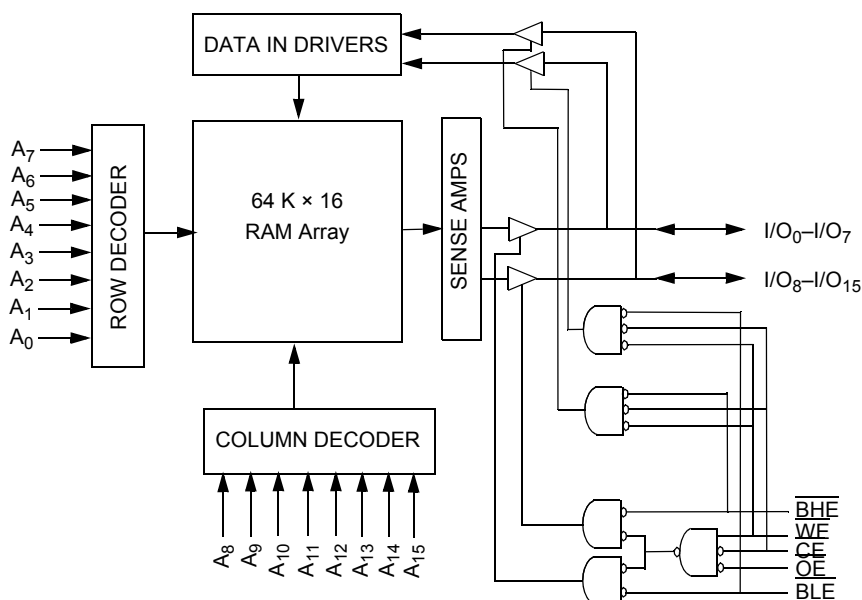
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the BHE and BLE are disabled ($\overline{BHE}$, BLE HIGH), or during a Write operation ($\overline{CE}$ LOW, and WE LOW).

For a complete list of related resources, [click here](#).

Logic Block Diagram



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Selection Guide

Description ^[1]	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

Pin Configurations

Figure 1. 44-pin SOJ/TSOP II pinout ^[2]

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Figure 2. 48-ball FBGA pinout ^[2]

1	2	3	4	5	6	
BLE	OE	A ₀	A ₁	A ₂	NC	A
I/O ₈	BHE	A ₃	A ₄	CE	I/O ₀	B
I/O ₉	I/O ₁₀	A ₅	A ₆	I/O ₂	I/O ₁	C
V _{SS}	I/O ₁₁	NC	A ₇	I/O ₃	V _{CC}	D
V _{CC}	I/O ₁₂	NC	NC	I/O ₄	V _{SS}	E
I/O ₁₄	I/O ₁₃	A ₁₄	A ₁₅	I/O ₅	I/O ₆	F
I/O ₁₅	NC	A ₁₂	A ₁₃	WE	I/O ₇	G
NC	A ₈	A ₉	A ₁₀	A ₁₁	NC	H

Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
- NC pins are not connected on the die.

Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A ₀ –A ₁₅	1–5, 18–21, 24–27, 42–44	Input	Address Inputs used to select one of the address locations.
I/O ₀ –I/O ₁₅	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	No Connects. This pin is not connected to the die.
WE	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
CE	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}$, $\overline{\text{BLE}}$	40, 39	Input/Control	Byte Write Select Inputs, active LOW. $\overline{\text{BHE}}$ controls I/O ₁₅ –I/O ₈ , $\overline{\text{BLE}}$ controls I/O ₇ –I/O ₀ .
OE	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When de-asserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} to relative GND^[3] -0.5 V to +4.6 V

DC voltage applied to outputs in high Z state^[3] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[3] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	-40 °C to +125 °C	2.5 V–2.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.3	–	V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 1.0 \text{ mA}$	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage ^[3]		-0.3	0.8	V
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-3	+3	μA
I_{OZ}	Output leakage current	$GND \leq V_I \leq V_{CC}$, output disabled	-3	+3	μA
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	–	80	mA
I_{SB1}	Automatic CE power-down Current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	15	mA
I_{SB2}	Automatic CE power-down Current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	–	10	mA

Note

3. $V_{IL}(\text{min.}) = -2.0\text{V}$ and $V_{IH}(\text{max.}) = V_{CC} + 0.5 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

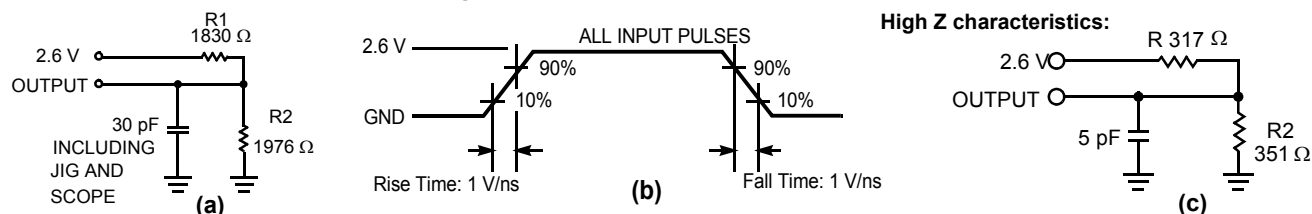
Parameter ^[4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 2.6\text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[4]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3×4.5 inch, four-layer printed circuit board	76.92	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		15.86	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[5]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except high Z) are tested using the Thevenin load shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

Switching Characteristics

Over the Operating Range

Parameter ^[6]	Description	-15		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	15	–	ns
t _{AA}	Address to data valid	–	15	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	15	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	7	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to low Z ^[7]	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to high Z ^[7, 8]	–	7	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to low Z ^[7]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to high Z ^[7, 8]	–	7	ns
t _{PU} ^[9]	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t _{PD} ^[9]	$\overline{\text{CE}}$ HIGH to power-down	–	15	ns
t _{DBE}	Byte enable to data valid	–	7	ns
t _{LZBE}	Byte enable to low Z	0	–	ns
t _{HZBE}	Byte disable to high Z	–	7	ns
Write Cycle ^[10, 11]				
t _{WC}	Write cycle time	15	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	10	–	ns
t _{AW}	Address set-up to write end	10	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address set-up to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	10	–	ns
t _{SD}	Data set-up to write end	8	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to low Z ^[7]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to high Z ^[7, 8]	–	7	ns
t _{BW}	Byte enable to end of write	9	–	ns

Notes

- Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.6 V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of [Figure 3](#). Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 [12, 13]

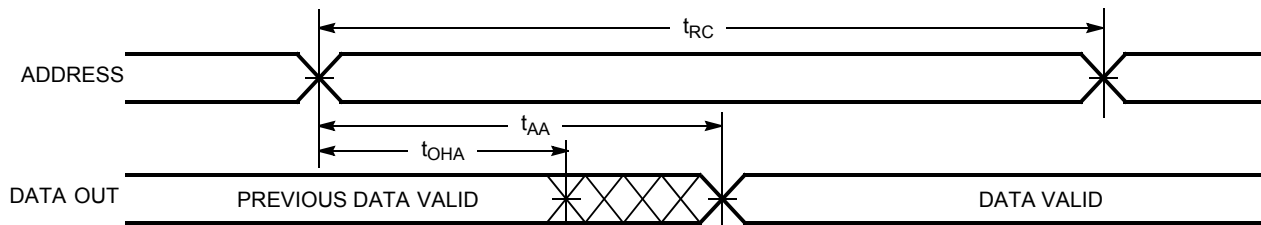
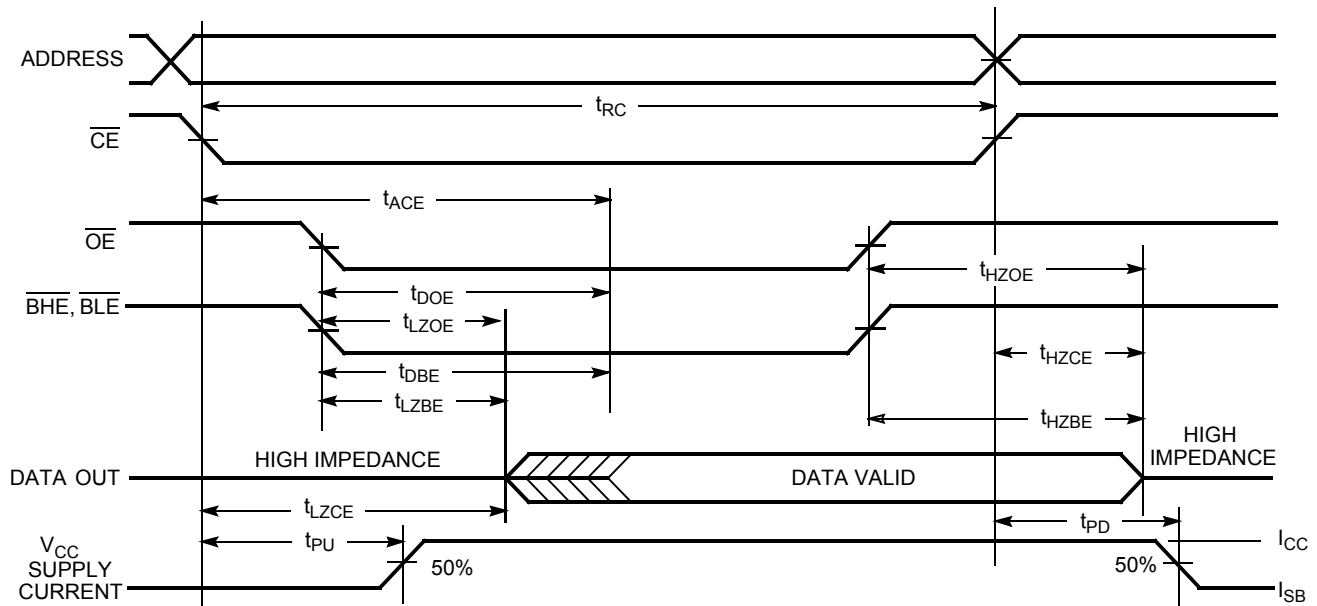


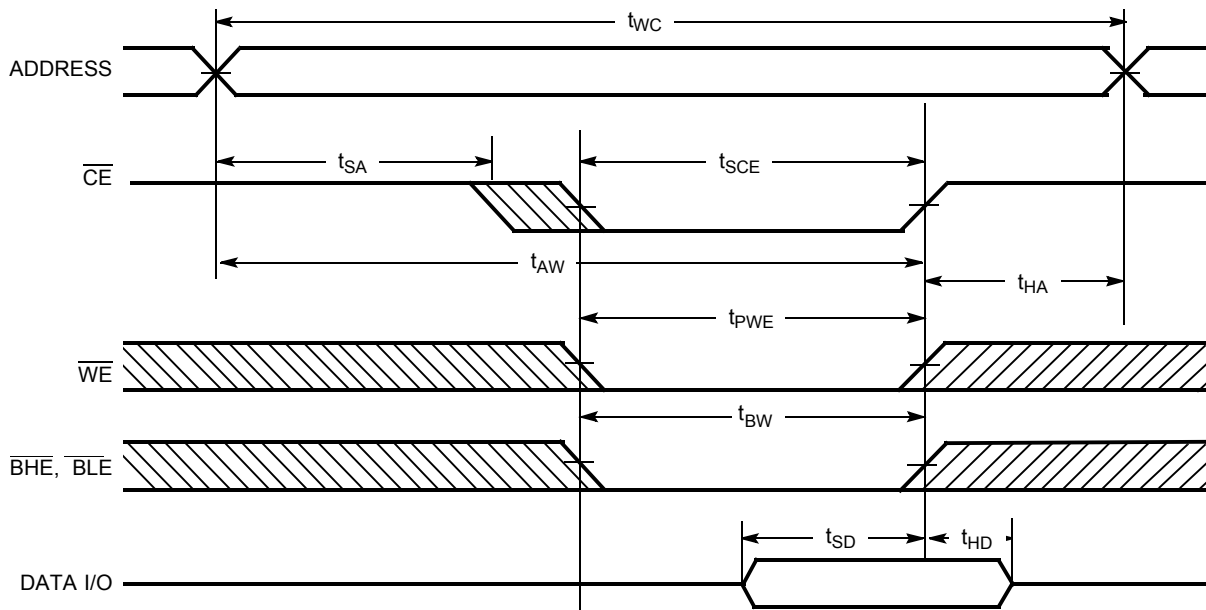
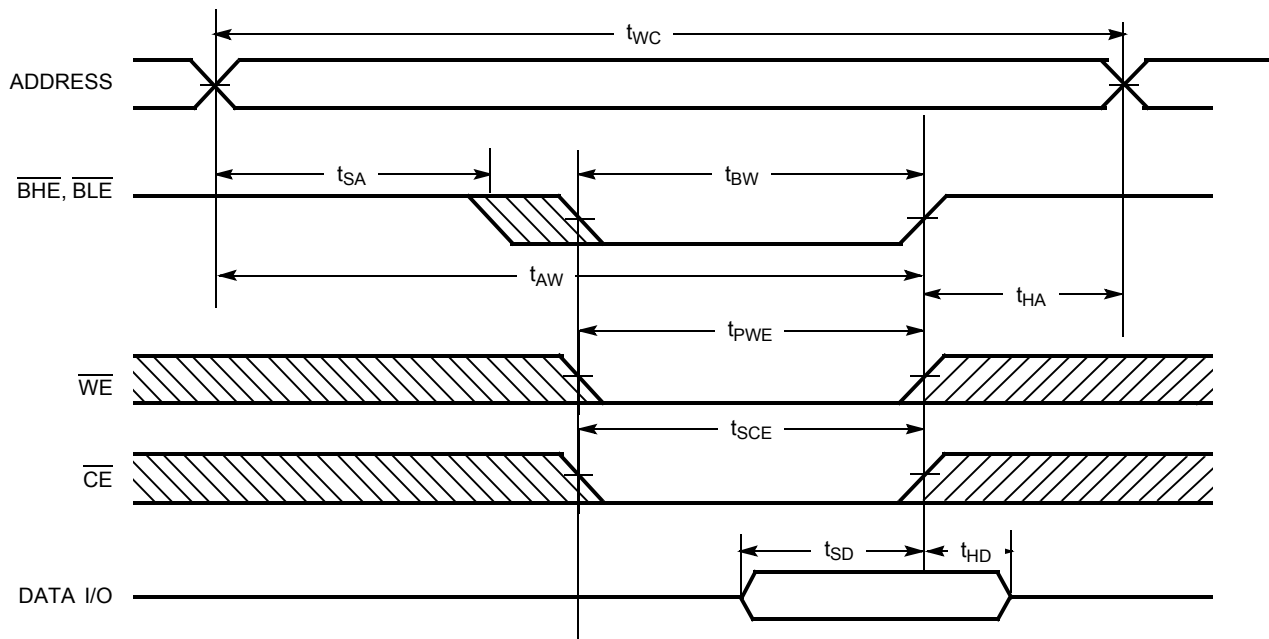
Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [13, 14]



Notes

12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL} .
13. $\overline{WE}$ is HIGH for Read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

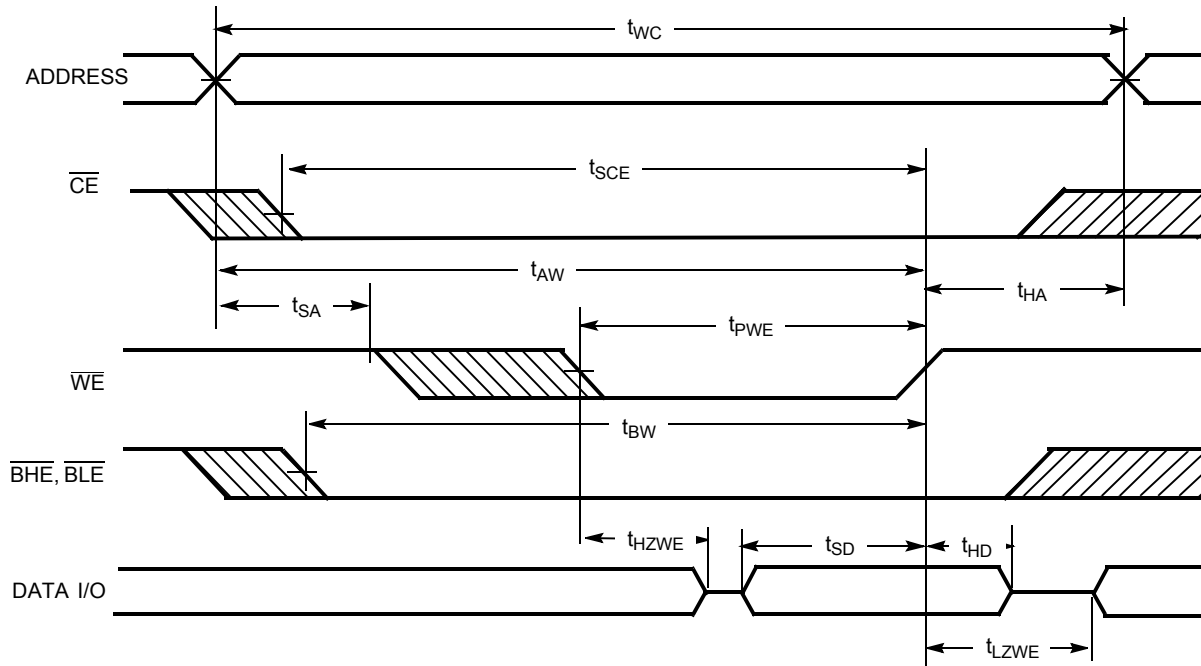
Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [15, 16]

Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes

15. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) ^[17]



Note

17. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{SD} and t_{HWE} .

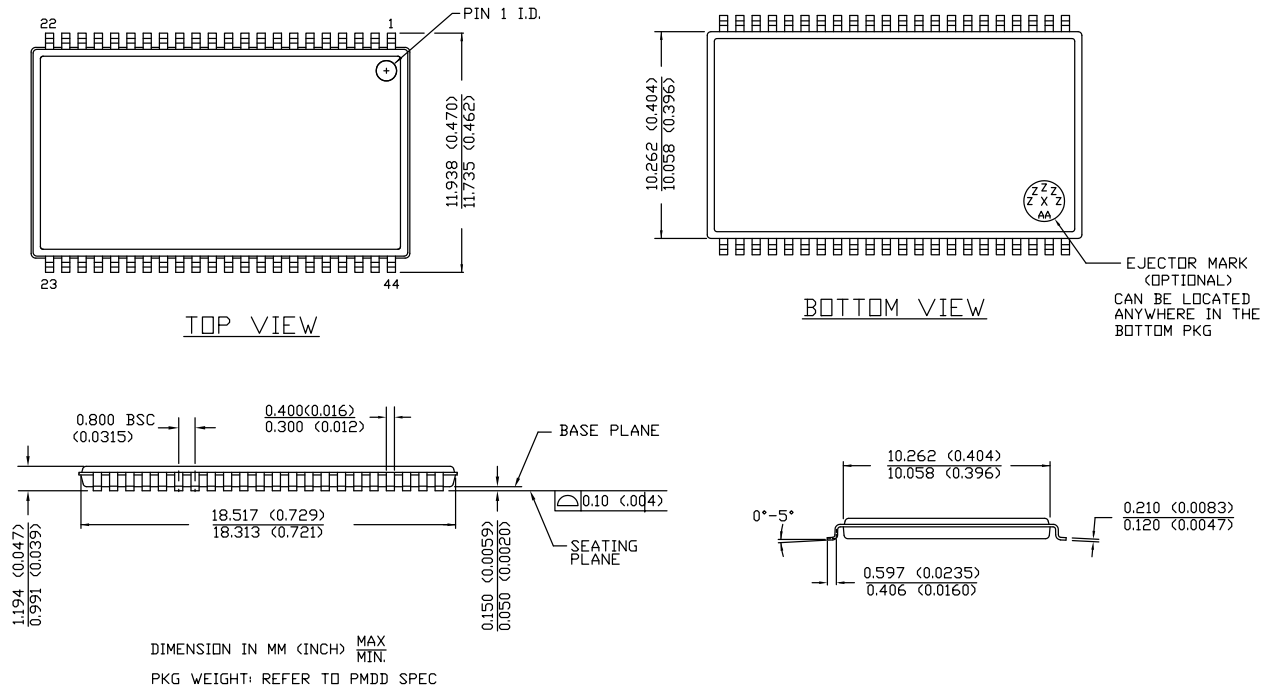
Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I _{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I _{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I _{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I _{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})



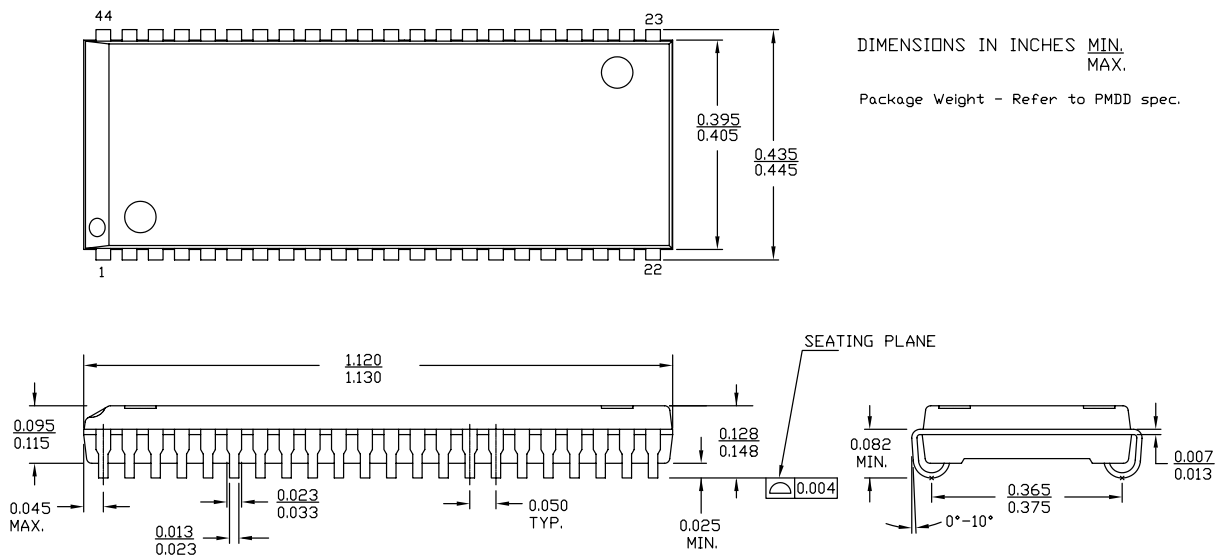
Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Figure 10. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 *E

Figure 11. 48-ball FBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150

NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021CV26, 1-Mbit (64 K × 16) Static RAM
Document Number: 38-05589

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	238454	See ECN	RKF	New data sheet for Automotive.
*A	335861	See ECN	SYT	Added 44-pin SOJ Package related information in all instances across the document. Updated Ordering Information : Updated part numbers (Added Lead-Free Product Information).
*B	493543	See ECN	NXR	Updated Electrical Characteristics : Changed description of I _{LX} parameter from "Input Load Current" to "Input Leakage Current". Removed I _{OS} parameter and its details. Updated Ordering Information : Updated part numbers.
*C	2897087	03/22/10	AJU	Updated Ordering Information : Removed obsolete parts. Updated Package Diagrams .
*D	3057593	10/13/2010	PRAS	Updated Ordering Information : Updated part numbers. Added Ordering Code Definitions . Updated Package Diagrams .
*E	3098812	12/01/2010	PRAS	Minor edits across the document. Added Acronyms and Units of Measure . Updated to new template.
*F	3277371	06/08/2011	AJU	Updated Pin Configurations (Included pin configurations for 44-pin SOJ and 48-ball FBGA packages).
*G	4141238	09/30/2013	VINI	Updated Package Diagrams : spec 51-85087 – Changed revision from *C to *E. spec 51-85082 – Changed revision from *C to *E. spec 51-85150 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*H	4567793	11/12/2014	VINI	Updated Functional Description : Added "For a complete list of related resources, click here ." at the end. Updated Switching Characteristics : Added Note 11 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 17 and referred the same note in Figure 8 . Completing Sunset Review.
*I	4573200	11/18/2014	VINI	Updated Ordering Information : Removed prune part numbers namely CY7C1021CV26-15VXE, CY7C1021CV26-15BAE, CY7C1021CV26-15BAET, and CY7C1021CV26-15VXET.
*J	5004033	11/05/2015	VINI	Updated to new template. Completing Sunset Review.

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