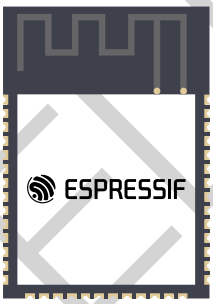
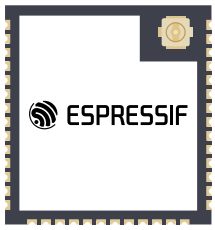
ESP32-S3-WROOM-2
ESP32-S3-WROOM-2U

Datasheet

2.4 GHz Wi-Fi (802.11 b/g/n) and Bluetooth® 5 (LE) module
Built around ESP32-S3R8V SoC, Xtensa® dual-core 32-bit LX7 microprocessor
Flash up to 32 MB, PSRAM up to 8 MB
33 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector



ESP32-S3-WROOM-2



ESP32-S3-WROOM-2U

Pre-release v0.1
Espressif Systems

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
www.espressif.com/sites/default/files/documentation/esp32-s3-wroom-2_wroom-2u_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S3R8V SoC embedded, Xtensa® dual-core 32-bit LX7 microprocessor, up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- Up to 8 MB PSRAM

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- 2 Mbps PHY
- Long range mode
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2

Peripherals

- GPIO, SPI, LCD, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB 1.1 OTG, USB Serial/JTAG controller, MCPWM, SDIO host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs

Integrated Components on Module

- 40 MHz crystal oscillator
- Up to 32 MB SPI flash

Antenna Options

- On-board PCB antenna (ESP32-S3-WROOM-2)
- External antenna via a connector (ESP32-S3-WROOM-2U)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C
- Dimensions: See Table 1

1.2 Description

ESP32-S3-WROOM-2 and ESP32-S3-WROOM-2U are two powerful, generic Wi-Fi + Bluetooth LE MCU modules that have a rich set of peripherals. They provide acceleration for neural network computing and signal processing workloads. They are an ideal choice for a wide variety of application scenarios related to AI and Artificial Intelligence of Things (AIoT), such as wake word detection and speech commands recognition, face

detection and recognition, smart home, smart appliances, smart control panel, smart speaker, etc.

ESP32-S3-WROOM-2 comes with a PCB antenna. ESP32-S3-WROOM-2U comes with an external antenna connector. They have ESP32-S3R8V SoC embedded. A selection of module variants are available for customers with flash memory of 16/32 MB and PSRAM memory of 8 MB.

The information in this datasheet is applicable to both modules. The ordering information for the two modules is as follows:

Table 1: Ordering Information

Ordering Code	Chip Embedded	Flash (MB)	PSRAM (MB)	Dimensions (mm)
ESP32-S3-WROOM-2-N16R8V	ESP32-S3R8V	16	8	18 × 25.5 × 3.1
ESP32-S3-WROOM-2-N32R8V	ESP32-S3R8V	32	8	
ESP32-S3-WROOM-2U-N16R8V	ESP32-S3R8V	16	8	18 × 19.2 × 3.2
ESP32-S3-WROOM-2U-N32R8V	ESP32-S3R8V	32	8	

At the core of the modules is an ESP32-S3R8V, an Xtensa® 32-bit LX7 CPU(with single precison FPU) that operates at up to 240 MHz. You can power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds.

ESP32-S3R8V integrates a rich set of peripherals including SPI, LCD, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, USB Serial/JTAG controller, MCPWM, SDIO host, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs, as well as up to 45 GPIOs. It also includes a full-speed USB 1.1 On-The-Go (OTG) interface to enable USB communication.

Note:
* For more information on ESP32-S3, please refer to *ESP32-S3 Series Datasheet*.

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications

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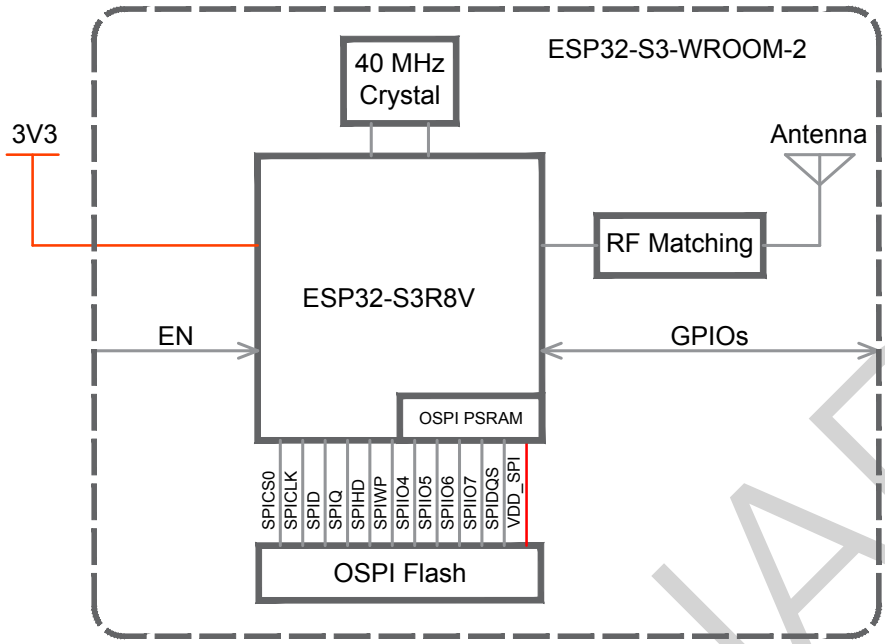

Figure 1: ESP32-S3-WROOM-2 Block Diagram

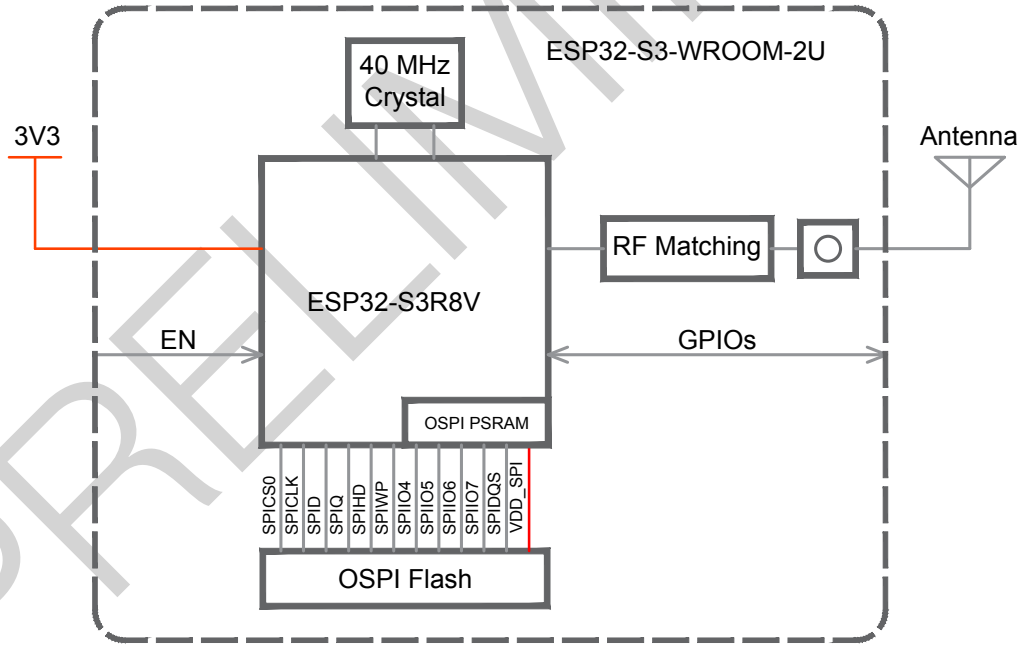

Figure 2: ESP32-S3-WROOM-2U Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 7.1 *Physical Dimensions*.

The pin diagram is applicable for ESP32-S3-WROOM-2 and ESP32-S3-WROOM-2U, but the latter has no keepout zone.

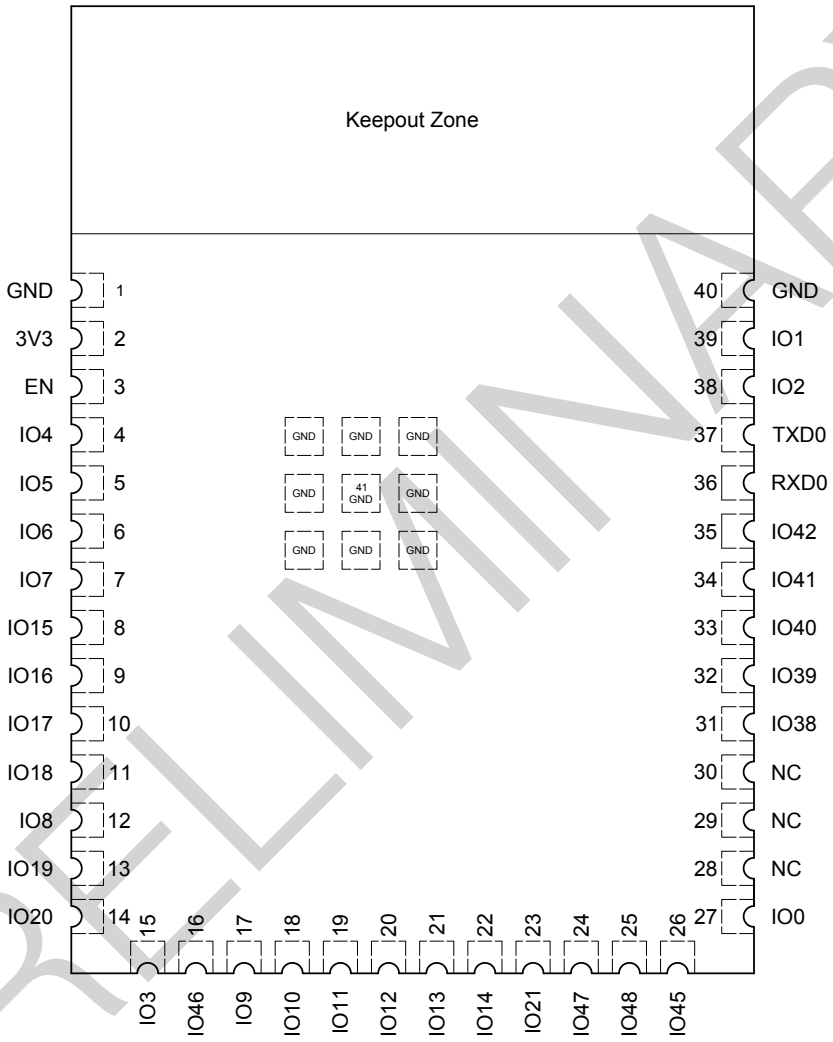

Figure 3: Pin Layout (Top View)

3.2 Pin Description

The module has 41 pins. See pin definitions in Table 2.

For explanations of pin names and function names, as well as configurations of peripheral pins, please refer to *ESP32-S3 Series Datasheet*.

Table 2: Pin Definitions

Name	No.	Type [1]	Function
GND	1	P	GND
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6
IO18	11	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7, SUBSPICS1
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO3	15	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO46	16	I/O/T	GPIO46
IO9	17	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
IO10	18	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
IO11	19	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
IO12	20	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
IO13	21	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7, SUBSPIQ
IO14	22	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS, SUBSPIWP
IO21	23	I/O/T	RTC_GPIO21, GPIO21
IO47	24	I/O/T	GPIO47, SPICLK_P, SUBSPICLK_P_DIFF
IO48	25	I/O/T	GPIO48, SPICLK_N, SUBSPICLK_N_DIFF
IO45	26	I/O/T	GPIO45
IO0	27	I/O/T	RTC_GPIO0, GPIO0
NC	28	-	NC
NC	29	-	NC
NC	30	-	NC
IO38	31	I/O/T	GPIO38, FSPIWP, SUBSPIWP
IO39	32	I/O/T	MTCK, GPIO39, CLK_OUT3, SUBSPICS1
IO40	33	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	34	I/O/T	MTDI, GPIO41, CLK_OUT1

Cont'd on next page

Table 2 – cont'd from previous page

Name	No.	Type [1]	Function
IO42	35	I/O/T	MTMS, GPIO42
RXD0	36	I/O/T	U0RXD, GPIO44, CLK_OUT2
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
GND	40	P	GND
EPAD	41	P	GND

[1] P: power supply; I: input; O: output; T: high impedance.

3.3 Strapping Pins

Note:
The content below is excerpted from Section Strapping Pins in *ESP32-S3 Series Datasheet*. For the strapping pin mapping between the chip and modules, please refer to Chapter 5 *Module Schematics*.

ESP32-S3 has four strapping pins:

- GPIO0
- GPIO45
- GPIO46
- GPIO3

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip's internal weak pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

GPIO3 is floating by default. When EFUSE_STRAP_JTAG_SEL is set, the strapping value of GPIO3 determines the source of the JTAG signal inside the CPU. In this case, the strapping value is controlled by the external circuit that cannot be in a high impedance state.

- When GPIO3 strapping value is 0, the JTAG signal comes from the on-chip JTAG pin.
- When GPIO3 strapping value is 1, the JTAG signal comes from the USB Serial/JTAG controller.

When EFUSE_STRAP_JTAG_SEL is 0, the JTAG signal comes from the USB Serial/JTAG controller.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S3.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed configuration of the strapping pins.

Table 3: Strapping Pins

VDD_SPI Voltage [1]			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [2]			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't care	0
Enabling/Disabling ROM Messages Print During Booting [3] [4]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the fourth note	See the fourth note
JTAG Signal Selection			
Pin	Default	EFUSE_STRAP_JTAG_SEL=0	EFUSE_STRAP_JTAG_SEL=1
GPIO3	N/A	USB Serial/JTAG	Strapping value: 0: PAD JTAG [5] 1: USB Serial/JTAG [5]

Note:

1. The functionality of strapping pin GPIO45 to select VDD_SPI voltage may be disabled by setting VDD_SPI_FORCE eFuse to 1. In such a case the voltage is selected with eFuse bit VDD_SPI_TIEH.
2. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
3. ROM boot messages can be printed over U0TXD (by default) or GPIO17, depending on the eFuse bit.
4. When both EFUSE_DIS_USB_DEVICE and USB_DIS_USB are 0, ROM boot messages will be printed to the USB Serial/JTAG controller. Otherwise, the messages will be printed to UART, controlled by GPIO46 and eFuse UART_PRINT_CONTROL. Specifically, when eFuse UART_PRINT_CONTROL value is:
   0, print is normal during boot and not controlled by GPIO46.
   1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
   2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
   3, print is disabled and not controlled by GPIO46.
5. PAD JTAG: JTAG signal comes from the on-chip JTAG pin;
   USB Serial/JTAG: JTAG signal comes from the USB Serial/JTAG controller.

Figure 4 shows the setup and hold times for the strapping pin before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 4.

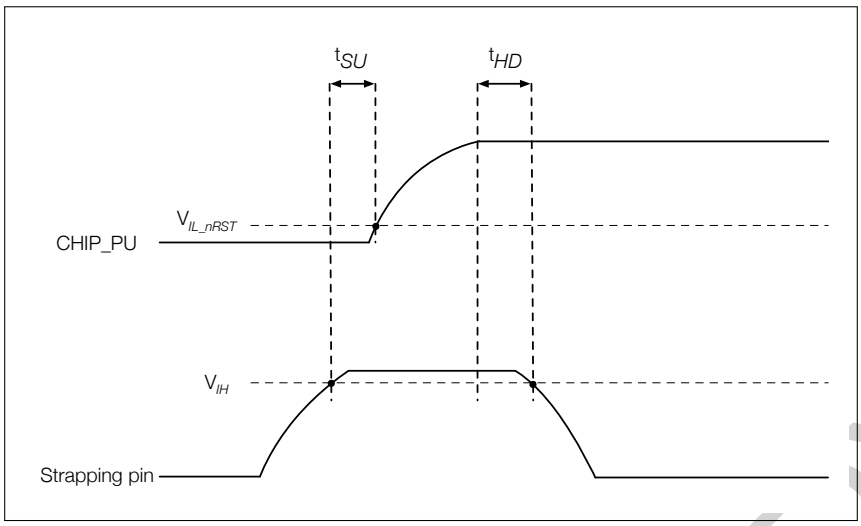

Figure 4: Setup and Hold Times for the Strapping Pin

Table 4: Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameter	Description	Min (μs)
t_{SU}	Setup time before CHIP_PU goes from low to high	0
t_{HD}	Hold time after CHIP_PU goes high	3

4 Electrical Characteristics

The values presented in this section are preliminary and may change with the final release of this datasheet.

4.1 Absolute Maximum Ratings

Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	105	°C

4.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	–40	—	85	°C
Humidity	Humidity condition	—	—	85	%RH

4.3 DC Characteristics (3.3 V, 25 °C)

Table 7: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ

Cont'd on next page

Table 7 – cont'd from previous page

Symbol	Parameter	Min	Typ	Max	Unit
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (EN voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage (EN voltage is within the specified range)	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

5 Module Schematics

This is the reference design of the module.

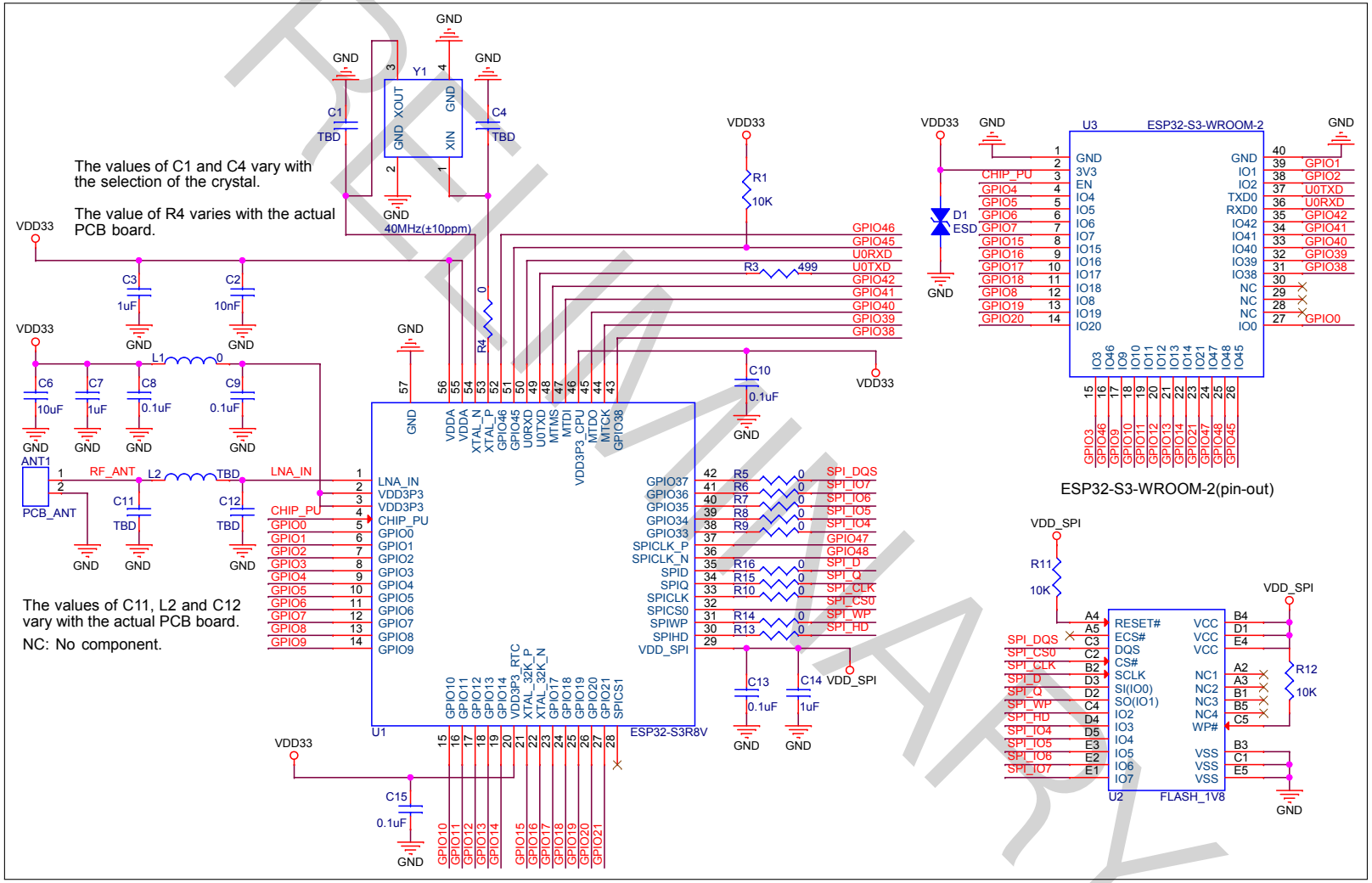

Figure 5: ESP32-S3-WROOM-2 Schematics

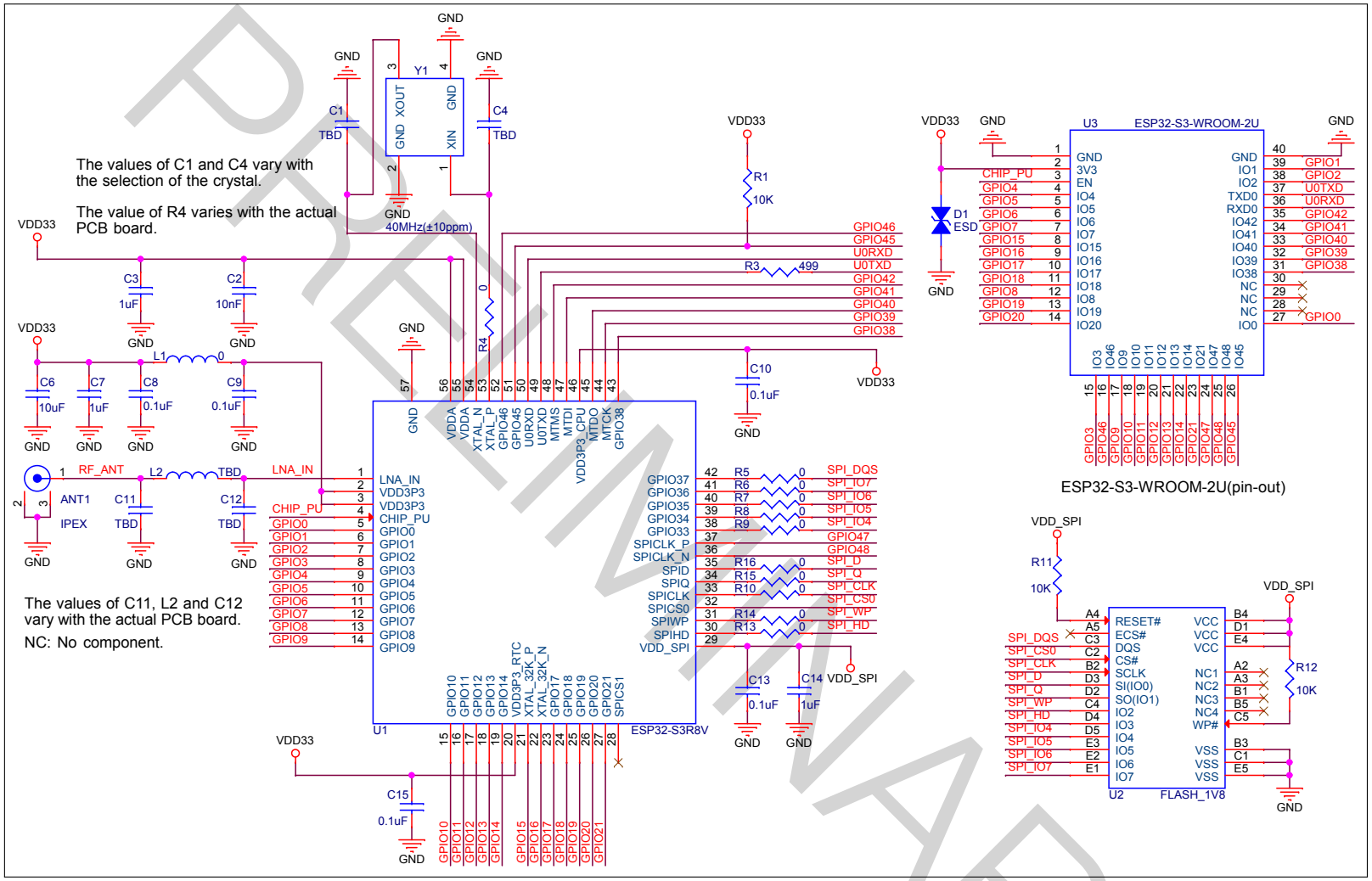

Figure 6: ESP32-S3-WROOM-2U Schematics

Note that the internal pull-up resistor (R1) for IO45 is populated in the module, as the flash in the module works at 1.8 V by default (output by VDD_SPI). Please make sure IO45 is not pulled low when the module is powered up by external circuit.

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

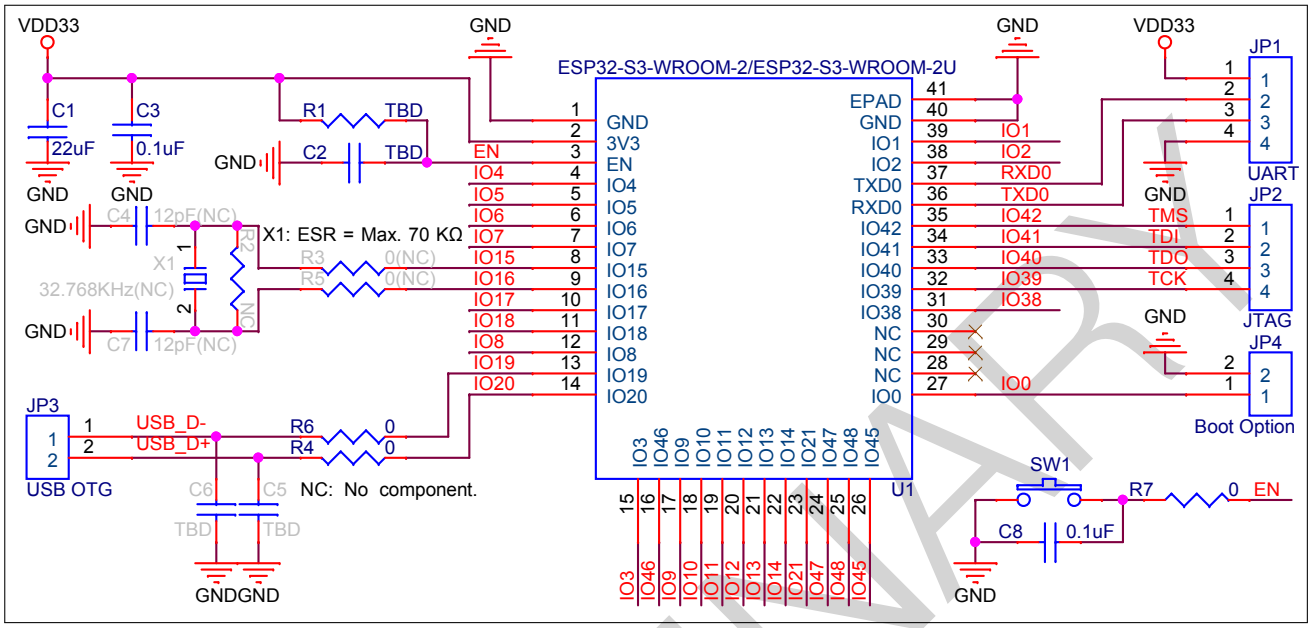

Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste.
- To ensure that the power supply to the ESP32-S3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32-S3 Series Datasheet*.

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

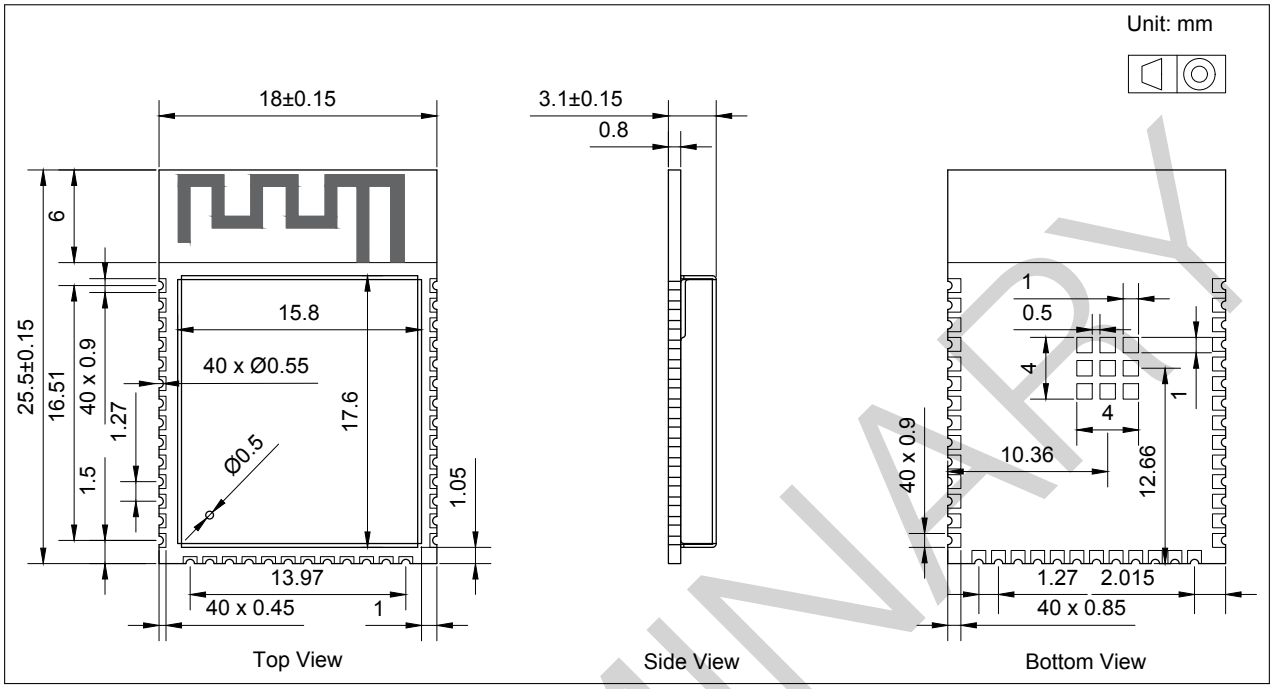

Figure 8: ESP32-S3-WROOM-2 Physical Dimensions

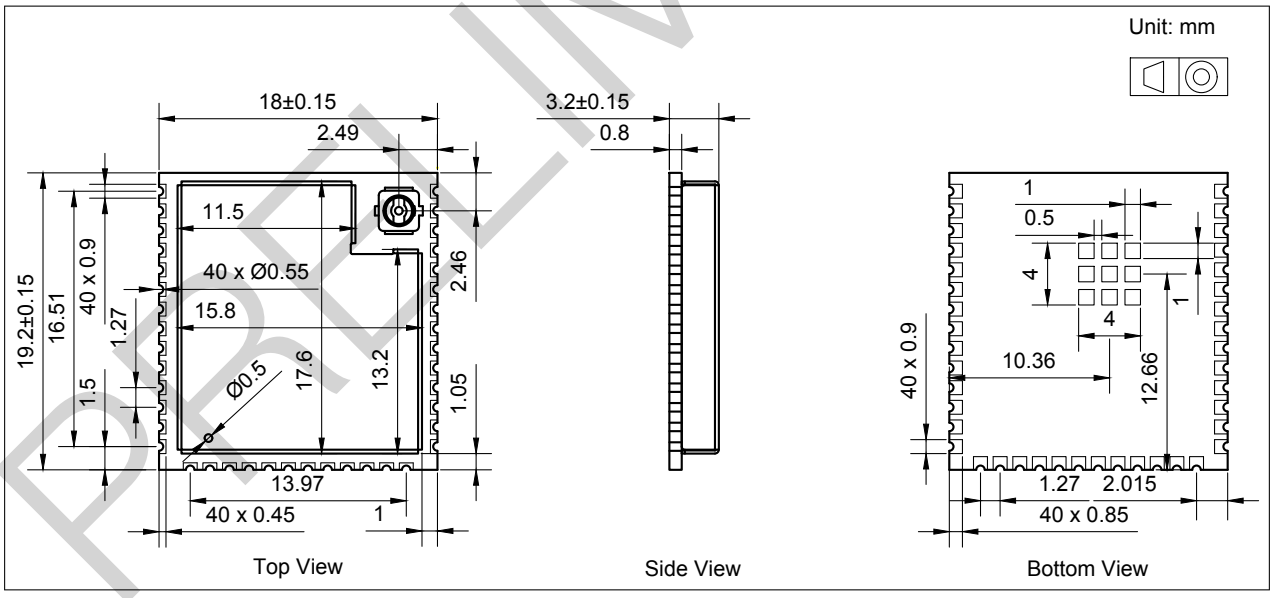

Figure 9: ESP32-S3-WROOM-2U Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *Espressif Module Package Information*.

7.2 Recommended PCB Land Pattern

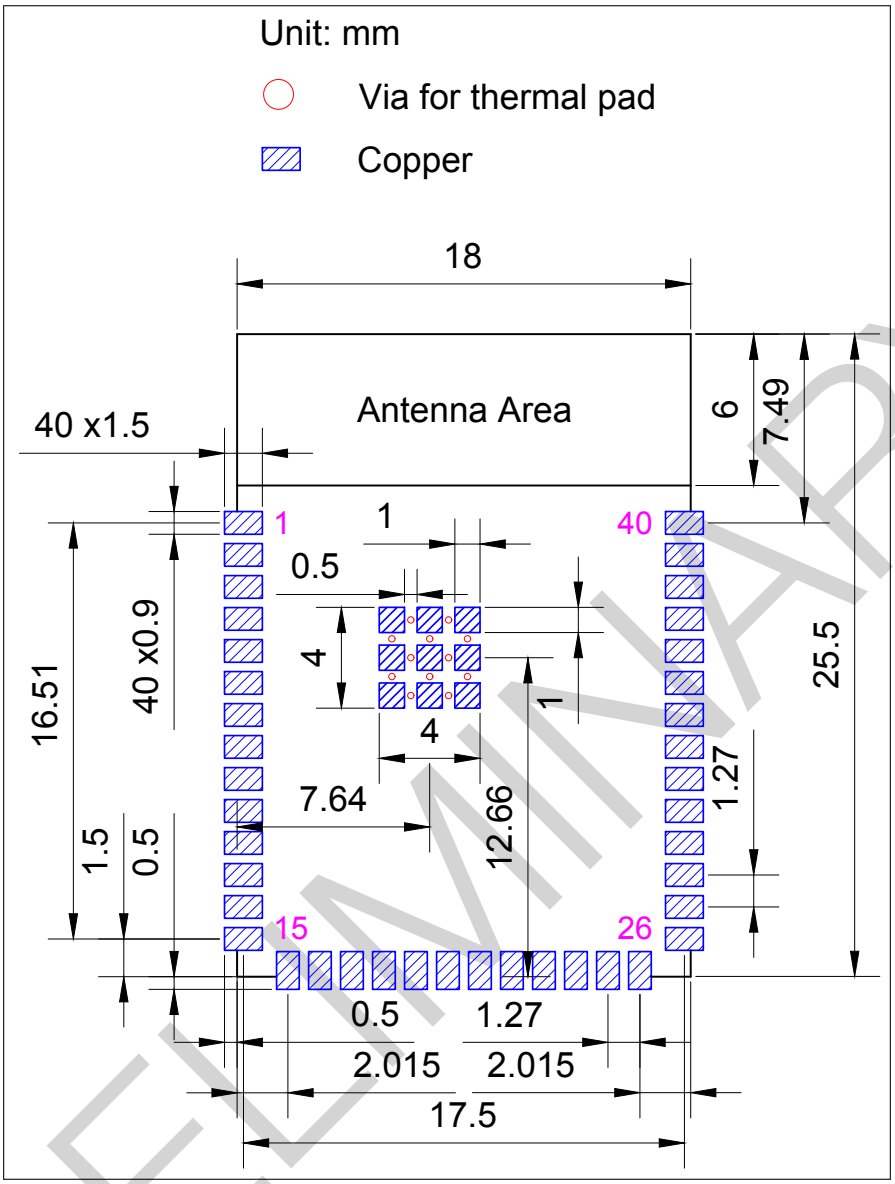

Figure 10: ESP32-S3-WROOM-2 Recommended PCB Land Pattern

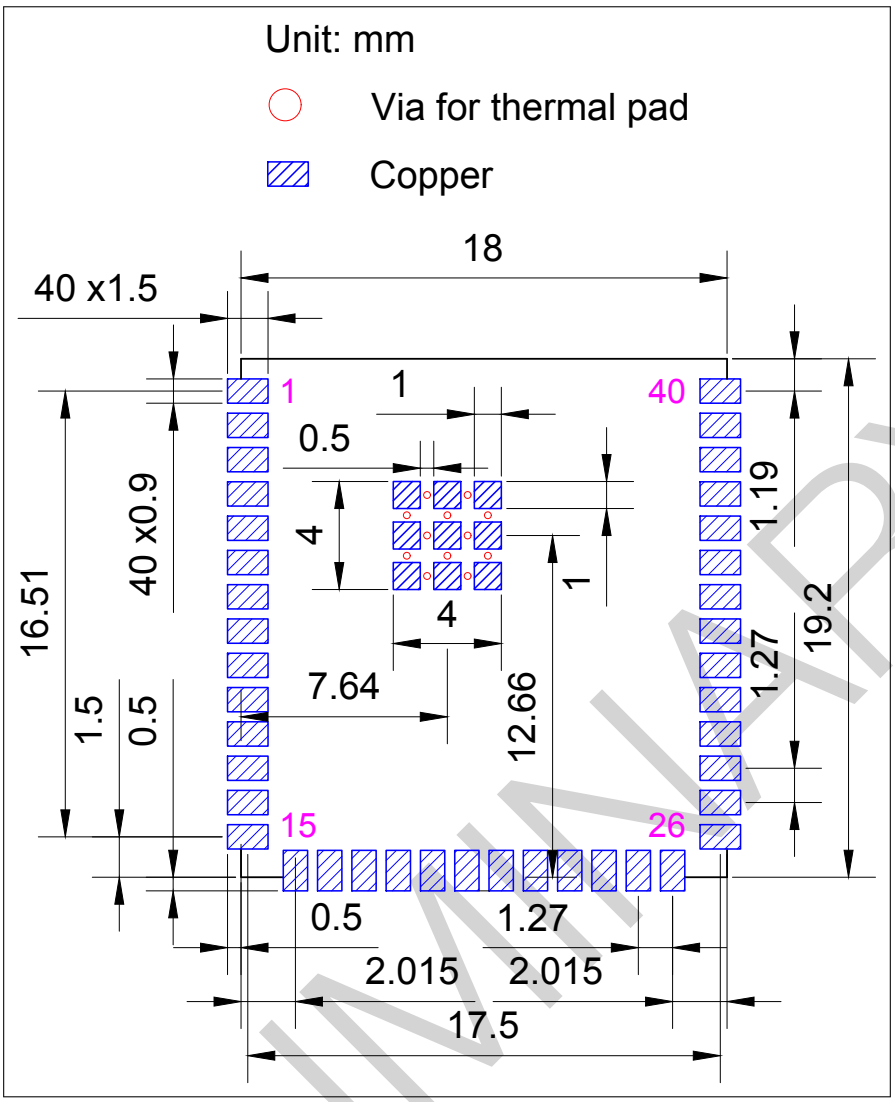

Figure 11: ESP32-S3-WROOM-2U Recommended PCB Land Pattern

7.3 Dimensions of External Antenna Connector

ESP32-S3-WROOM-2U uses the first generation external antenna connector as shown in Figure 12. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

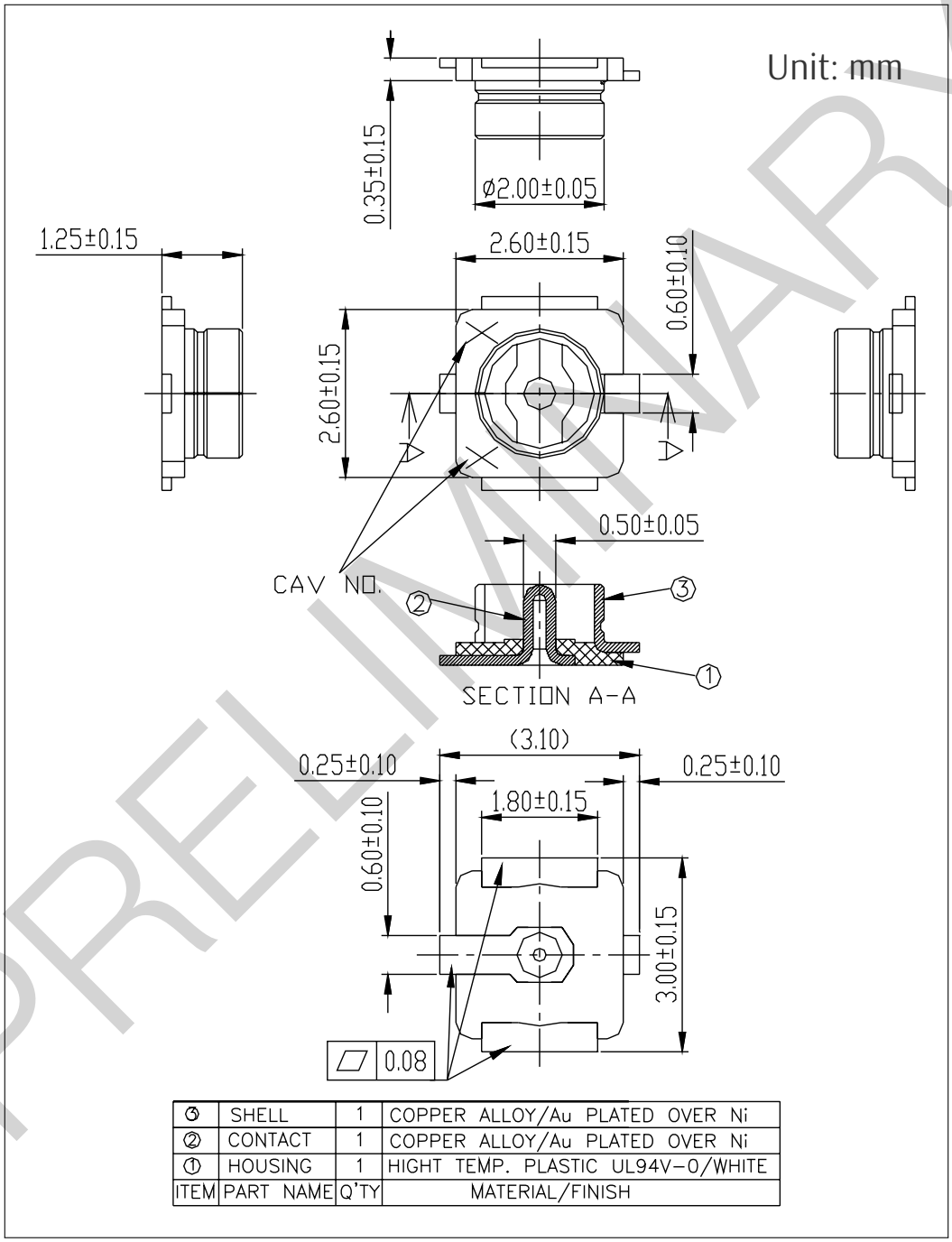

Figure 12: Dimensions of External Antenna Connector (IPEX Generation 1)

8 Product Handling

8.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and /90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and /60%RH. If the above conditions are not met, the module needs to be baked.

8.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

8.3 Reflow Profile

Solder the module in a single reflow.

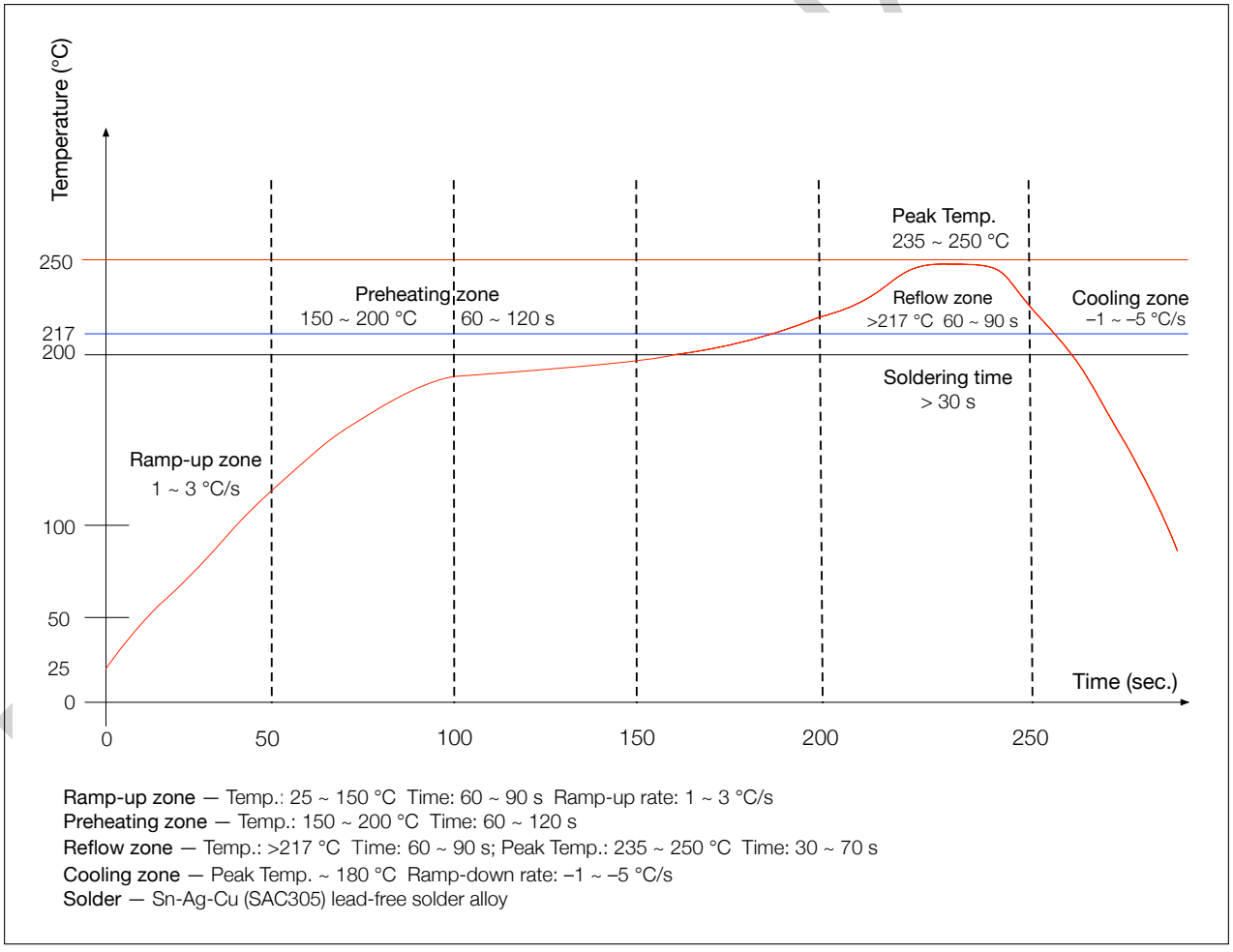

Figure 13: Reflow Profile

9 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- *Certificates*
  http://espressif.com/en/support/documents/certificates
- *Documentation Updates and Update Notification Subscription*
  http://espressif.com/en/support/download/documents

Developer Zone

- *ESP-IDF* and other development frameworks on GitHub.
  http://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  http://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
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- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
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Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
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- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  http://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2021-07-13	V0.1	Preliminary release

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