

Motion SPM® 45 Series

FND42060F2

General Description

FND42060F2 is an advanced Motion SPM 45 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's robust short-circuit-rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- 600 V – 20 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Built-In NTC Thermistor for Temperature Monitoring
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Optimized for 5 kHz Switching Frequency
- Isolation Rating: 4000 V_{rms}/min
- Remove Dummy Pin

Applications

- Motion Control – Home Appliance/Industrial Motor

Related Resources

- [AN-9070](#) – Motion SPM® 45 Series Users Guide
- [AN-9071](#) – Motion SPM® 45 Series Thermal Performance Information
- [AN-9072](#) – Motion SPM® 45 Series Mounting Guidance
- RD-344 – Reference Design (Three Shunt Solution)
- RD-345 – Reference Design (One Shunt Solution)

Integrated Power Functions

- 600 V-20 A IGBT inverter for three-phase DC/AC power conversion (Refer to Figure 3)



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SPMAA-C26
CASE MODFC

Figure 1. Package Overview
(Click to Activate 3D Content)

MARKING DIAGRAM

| |
|--------------|
| XXXXXXXXXXXX |
| ZZZ ATYWW |
| NNNNNNNN |

| | |
|------|------------------------------|
| XXXX | = Specific Device Code |
| ZZZ | = Lot ID |
| AT | = Assembly and Test Location |
| Y | = Year |
| WW | = Work Week |
| NNN | = Serial Number |

ORDERING INFORMATION

| Device | Package | Shipping |
|------------|-----------|---------------|
| FND42060F2 | SPMAA-J26 | 12 Units/Rail |

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out (UVLO) protection
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit, Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3/5 V logic, Schmitt-trigger input

PIN CONFIGURATION

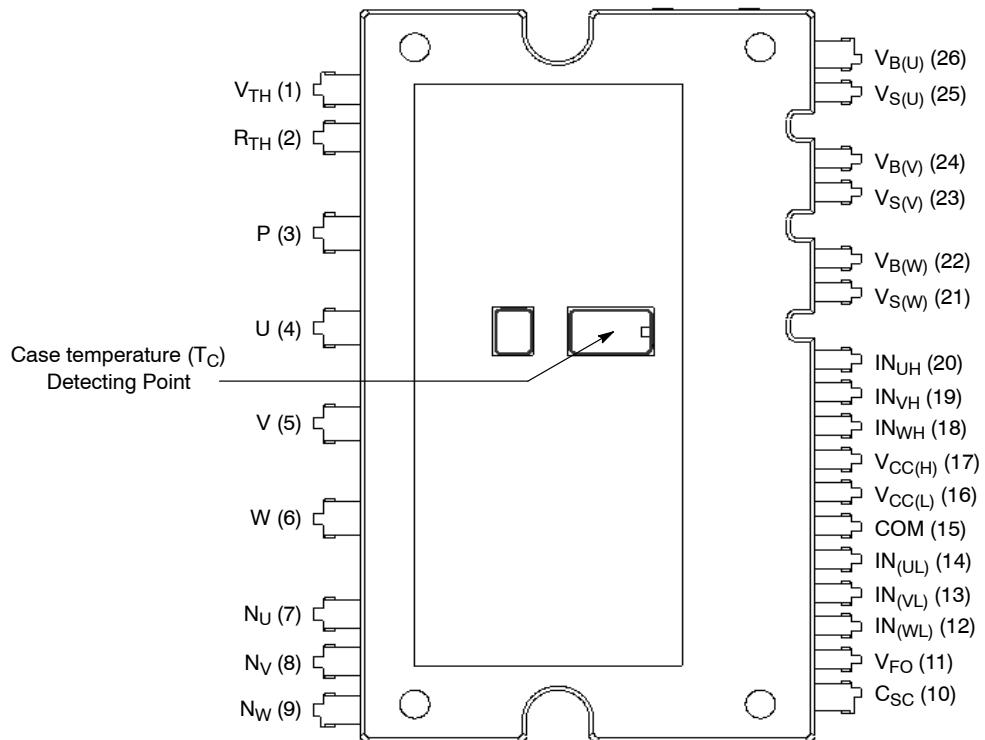


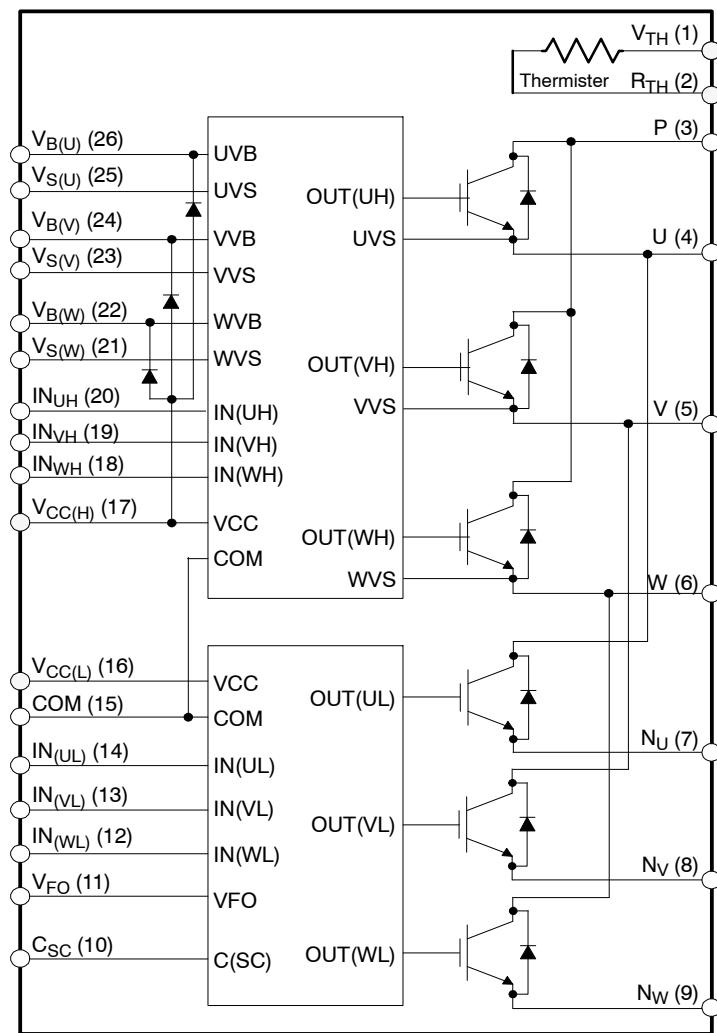
Figure 2. Top View

FND42060F2

PIN DESCRIPTIONS

| Pin Number | Pin Name | Pin Description |
|------------|-------------|---|
| 1 | V_{TH} | Thermistor Bias Voltage |
| 2 | R_{TH} | Series Resistor for the Use of Thermistor (Temperature Detection) |
| 3 | P | Positive DC-Link Input |
| 4 | U | Output for U-Phase |
| 5 | V | Output for V-Phase |
| 6 | W | Output for W-Phase |
| 7 | N_U | Negative DC-Link Input for U-Phase |
| 8 | N_V | Negative DC-Link Input for V-Phase |
| 9 | N_W | Negative DC-Link Input for W-Phase |
| 10 | C_{SC} | Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input |
| 11 | V_{FO} | Fault Output |
| 12 | $IN_{(WL)}$ | Signal Input for Low-Side W-Phase |
| 13 | $IN_{(VL)}$ | Signal Input for Low-Side V-Phase |
| 14 | $IN_{(UL)}$ | Signal Input for Low-Side U-Phase |
| 15 | COM | Common Supply Ground |
| 16 | $V_{CC(L)}$ | Low-Side Common Bias Voltage for IC and IGBTs Driving |
| 17 | $V_{CC(H)}$ | High-Side Common Bias Voltage for IC and IGBTs Driving |
| 18 | $IN_{(WH)}$ | Signal Input for High-Side W-Phase |
| 19 | $IN_{(VH)}$ | Signal Input for High-Side V-Phase |
| 20 | $IN_{(UH)}$ | Signal Input for High-Side U-Phase |
| 21 | $V_{S(W)}$ | High-Side Bias Voltage Ground for W-Phase IGBT Driving |
| 22 | $V_{B(W)}$ | High-Side Bias Voltage for W-Phase IGBT Driving |
| 23 | $V_{S(V)}$ | High-Side Bias Voltage Ground for V-Phase IGBT Driving |
| 24 | $V_{B(V)}$ | High-Side Bias Voltage for V-Phase IGBT Driving |
| 25 | $V_{S(U)}$ | High-Side Bias Voltage Ground for U-Phase IGBT Driving |
| 26 | $V_{B(U)}$ | High-Side Bias Voltage for U-Phase IGBT Driving |

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:

1. Inverter high-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Figure 3. Internal Block Diagram

FND42060F2

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------------------------|--|---|---------------------|-----------|
| INVERTER PART | | | | |
| V_{PN} | Supply Voltage | Applied between P– N_U , N_V , N_W | 450 | V |
| $V_{PN(\text{Surge})}$ | Supply Voltage (Surge) | Applied between P– N_U , N_V , N_W | 500 | V |
| V_{CES} | Collector–Emitter Voltage | | 600 | V |
| $\pm I_C$ | Each IGBT Collector Current | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ | 20 | A |
| $\pm I_{CP}$ | Each IGBT Collector Current (Peak) | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width | 40 | A |
| P_C | Collector Dissipation | $T_C = 25^\circ\text{C}$ per Chip | 50 | W |
| T_J | Operating Junction Temperature | (Note 2) | -40 ~ 150 | °C |
| CONTROL PART | | | | |
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(H)}$, $V_{CC(L)}$ – COM | 20 | V |
| V_{BS} | High–Side Control Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | 20 | V |
| V_{IN} | Input Signal Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM | -0.3 ~ $V_{CC}+0.3$ | V |
| V_{FO} | Fault Output Supply Voltage | Applied between V_{FO} – COM | -0.3 ~ $V_{CC}+0.3$ | V |
| I_{FO} | Fault Output Current | Sink Current at V_{FO} pin | 1 | mA |
| V_{SC} | Current Sensing Input Voltage | Applied between C_{SC} – COM | -0.3 ~ $V_{CC}+0.3$ | V |
| BOOTSTRAP DIODE PART | | | | |
| V_{RRM} | Maximum Repetitive Reverse Voltage | | 600 | V |
| I_F | Forward Current | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ | 0.50 | A |
| I_{FP} | Forward Current (Peak) | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width | 1.50 | A |
| T_J | Operating Junction Temperature | | -40 ~ 150 | °C |
| TOTAL SYSTEM | | | | |
| $V_{PN(\text{PROT})}$ | Self–Protection Supply Voltage Limit (Short–Circuit Protection Capability) | $V_{CC} = V_{BS} = 13.5 \text{ V} \sim 16.5 \text{ V}$ $T_J = 150^\circ\text{C}$, Non–repetitive, $< 2 \mu\text{s}$ | 400 | V |
| T_{STG} | Storage Temperature | | -40 ~ 125 | °C |
| V_{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 minute, Connect Pins to Heat Sink Plate (Note 3) | 4000 | V_{rms} |

1. The maximum junction temperature rating of the power chips integrated within the Motion SPM 45 product is 150°C .
2. For the measurement point of case temperature (T_C). Please refer to Figure 2.
3. For the Recommend Heat–Sink Design, Please refer to Figure 11. if do not follow Recommend Heat–Sink Design, Viso is 2000 V_{rms} .

THERMAL RESISTANCE

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------------|-------------------------------------|------|------|------|------|
| $R_{th(j-c)Q}$ | Junction to Case Thermal Resistance | Inverter IGBT Part (per 1/6 module) | - | - | 2.5 | °C/W |
| $R_{th(j-c)F}$ | | Inverter FWDi Part (per 1/6 module) | - | - | 3.6 | °C/W |

ELECTRICAL CHARACTERISTICS – INVERTER PART ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|----------------------|--|--|---|------|------|------|---------------|
| $V_{CE(\text{SAT})}$ | Collector – Emitter Saturation Voltage | $V_{CC} = V_{BS} = 15 \text{ V}$, $V_{IN} = 5 \text{ V}$ | $I_C = 20 \text{ A}$, $T_J = 25^\circ\text{C}$ | – | 1.85 | 2.35 | V |
| V_F | FWDi Forward Voltage | $V_{IN} = 0 \text{ V}$ | $I_F = 20 \text{ A}$, $T_J = 25^\circ\text{C}$ | – | 1.95 | 2.45 | V |
| HS | t_{ON} | Switching Times | $V_{PN} = 300 \text{ V}$, $V_{CC} = V_{BS} = 15 \text{ V}$, $I_C = 20 \text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0 \text{ V} \leftrightarrow 5 \text{ V}$, Inductive Load (Note 4) | 0.45 | 0.75 | 1.25 | μs |
| | $t_{C(ON)}$ | | | – | 0.20 | 0.45 | μs |
| | t_{OFF} | | | – | 0.70 | 1.20 | μs |
| | $t_{C(OFF)}$ | | | – | 0.15 | 0.40 | μs |
| | t_{rr} | | | – | 0.15 | – | μs |
| LS | t_{ON} | | $V_{PN} = 300 \text{ V}$, $V_{CC} = V_{BS} = 15 \text{ V}$, $I_C = 20 \text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0 \text{ V} \leftrightarrow 5 \text{ V}$, Inductive Load (Note 4) | 0.45 | 0.75 | 1.25 | μs |
| | $t_{C(ON)}$ | | | – | 0.20 | 0.45 | μs |
| | t_{OFF} | | | – | 0.75 | 1.25 | μs |
| | $t_{C(OFF)}$ | | | – | 0.15 | 0.40 | μs |
| | t_{rr} | | | – | 0.15 | – | μs |
| I_{CES} | Collector-Emitter Leakage Current | $V_{CE} = V_{CES}$ | – | – | 5 | mA | |

4. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

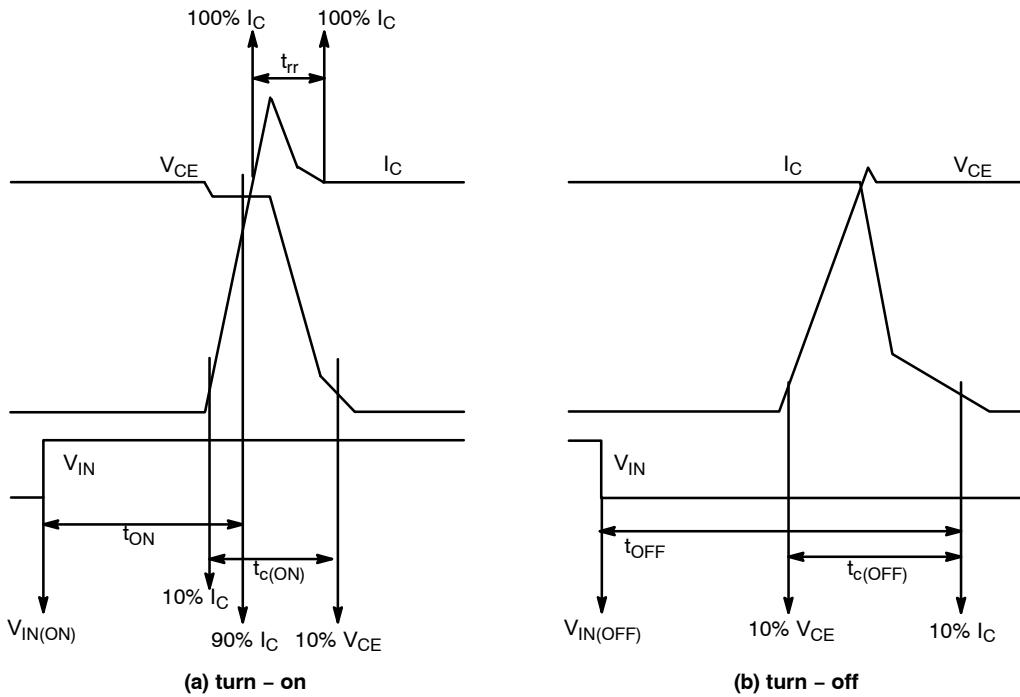


Figure 4. Switching Time Definition

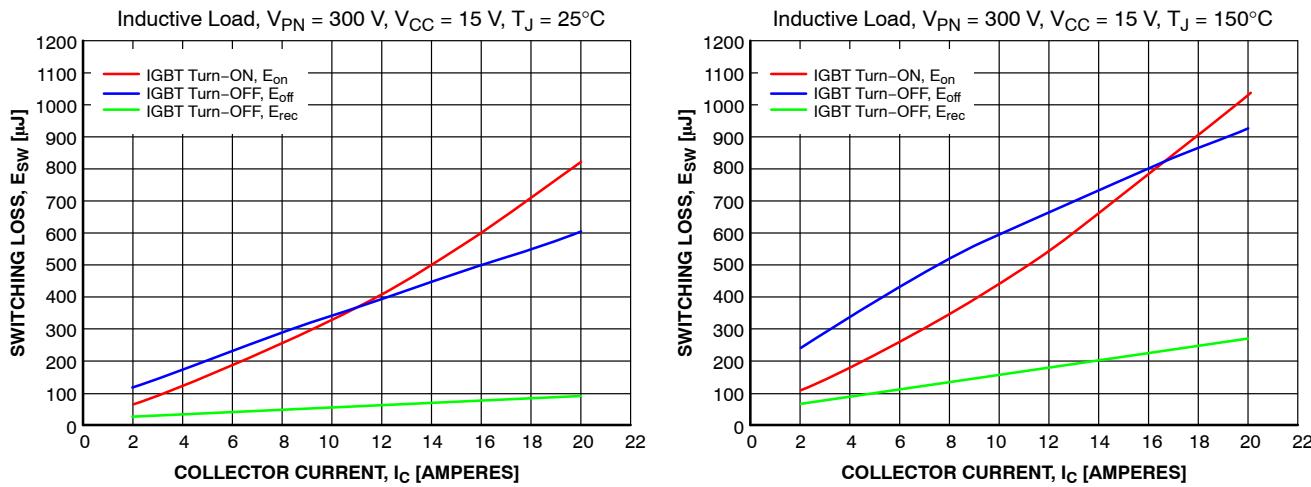


Figure 5. Switching Loss Characteristics (Typical)

CONTROL PART

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---------------|---|--|---|------|------|------------|---------------|
| I_{QCCH} | Quiescent V_{CC} Supply Current | $V_{CC(H)} = 15$ V, $IN_{(UH,VH,WH)} = 0$ V | $V_{DD(H)} - COM$ | — | — | 0.10 | mA |
| I_{QCCL} | | $V_{CC(L)} = 15$ V, $IN_{(UL,VL,WL)} = 0$ V | $V_{CC(L)} - COM$ | — | — | 2.65 | mA |
| I_{PCCH} | Operating V_{CC} Supply Current | $V_{CC(L)} = 15$ V, $f_{PWM} = 20$ kHz, duty = 50%, Applied to one PWM Signal Input for High-Side | $V_{CC(H)} - COM$ | — | — | 0.15 | mA |
| I_{PCCL} | | $V_{CC(L)} = 15$ V, $f_{PWM} = 20$ kHz, duty = 50%, Applied to one PWM Signal Input for Low-Side | $V_{CC(L)} - COM$ | — | — | 4.00 | mA |
| I_{QBS} | Quiescent V_{BS} Supply Current | $V_{BS} = 15$ V, $IN_{(UH,VH,WH)} = 0$ V | $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$, | — | — | 0.30 | mA |
| I_{PBS} | Operating V_{BS} Supply Current | $V_{DD} = V_{BS} = 15$ V, $f_{PWM} = 20$ kHz, duty = 50%, Applied to one PWM Signal Input for High-Side | $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$, | — | — | 2.00 | mA |
| V_{FOH} | Fault Output Voltage | $V_{SC} = 0$ V, V_{FO} Circuit: 10 k Ω to 5 V Pull-up | 4.5 | — | — | — | V |
| V_{FOL} | | $V_{SC} = 1$ V, V_{FO} Circuit: 10 k Ω to 5 V Pull-up | — | — | 0.5 | — | V |
| $V_{SC(ref)}$ | Short Circuit Trip Level | $V_{CC} = 15$ V (Note 5) | 0.45 | 0.50 | 0.55 | — | V |
| UV_{CCD} | Supply Circuit Under-Voltage Protection | Detection Level | 10.5 | — | 13.0 | — | V |
| UV_{CCR} | | Reset Level | 11.0 | — | 13.5 | — | V |
| UV_{BSD} | | Detection Level | 10.0 | — | 12.5 | — | V |
| UV_{BSR} | | Reset Level | 10.5 | — | 13.0 | — | V |
| t_{FOD} | Fault-Out Pulse Width | | 30 | — | — | — | μs |
| $V_{IN(ON)}$ | ON Threshold Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM | — | — | 2.6 | — | V |
| $V_{IN(OFF)}$ | OFF Threshold Voltage | | 0.8 | — | — | — | V |
| R_{TH} | Resistance of Thermister | $@ T_{TH} = 25^\circ\text{C}$ (Note 6) | — | 47 | — | k Ω | |
| | | $@ T_{TH} = 100^\circ\text{C}$ | — | 2.9 | — | k Ω | |

5. Short-circuit current protection os functioning only at the low-sides.

6. T_{TH} is the temperature of thermister itself. To know case temperature (T_C), please make the experiment considering your application.

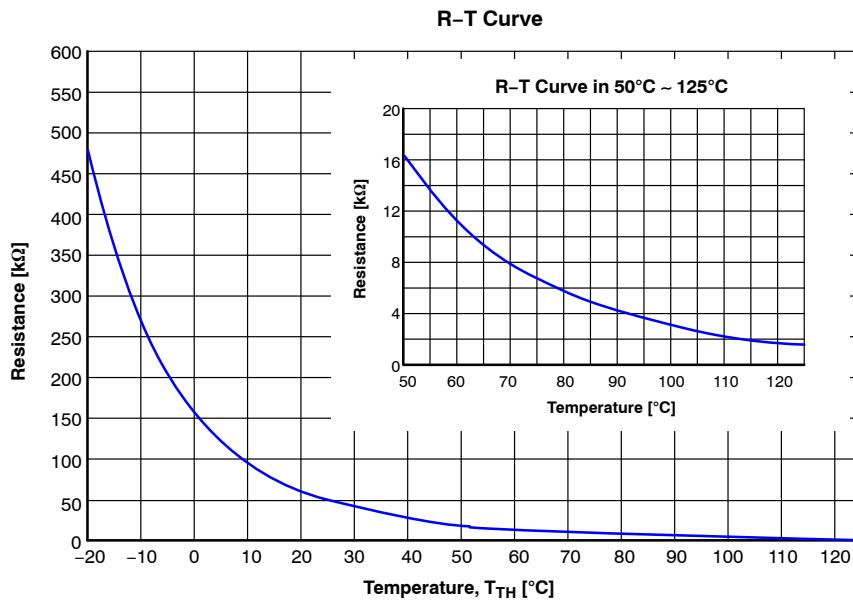
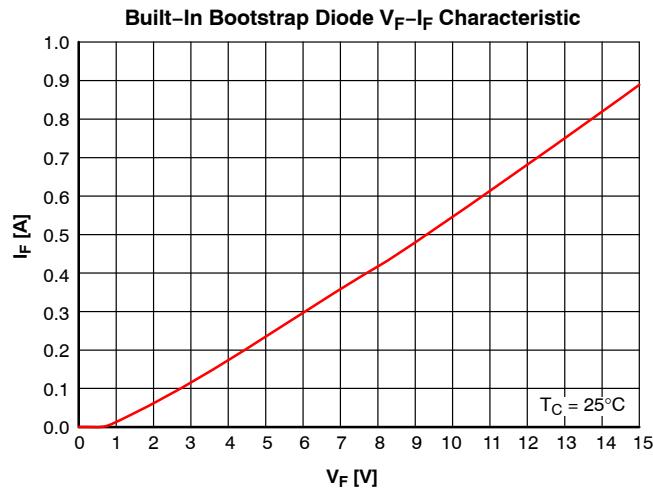


Figure 6. R-T Curve of the Built-In Thermistor

BOOTSTRAP DIODE PART

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------|-----------------------|--|------|------|------|------|
| V_F | Forward Voltage | $I_F = 0.1 \text{ A}$, $T_C = 25^\circ\text{C}$ | – | 2.5 | – | V |
| t_{rr} | Reverse-Recovery Time | $I_F = 0.1 \text{ A}$, $T_C = 25^\circ\text{C}$ | – | 80 | – | ns |



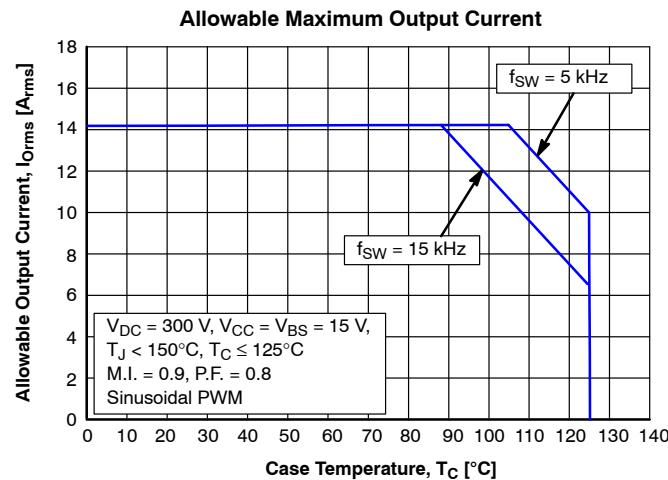
NOTE: Built-in bootstrap diode includes around 15Ω resistance characteristic.

Figure 7. Built-In Bootstrap Diode Characteristics

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|--|---|------|------|------|------------|
| V_{PN} | Supply Voltage | Applied between P – N_U , N_V , N_W | – | 300 | 400 | V |
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(H)}$ – COM, $V_{CC(L)}$ – COM | 13.5 | 15.0 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied between $V_{B(U)} – V_{S(U)}$, $V_{B(V)} – V_{S(V)}$, $V_{B(W)} – V_{S(W)}$ | 13.0 | 15.0 | 18.5 | V |
| dV_{CC}/dt , dV_{BS}/dt | Control Supply Variation | | –1 | – | 1 | V/ μ s |
| t_{dead} | Blanking Time for Preventing Arm-Short | For Each Input Signal | 1.5 | – | – | μ s |
| f_{PWM} | PWM Input Signal | $-40^\circ C < T_J < 150^\circ C$ | – | – | 20 | kHz |
| V_{SEN} | Voltage for Current Sensing | Applied between N_U , N_V , N_W – COM (Including Surge Voltage) | –4 | – | 4 | V |
| $P_{WIN(ON)}$ | Minimum Input Pulse Width | (Note 7) | 0.7 | – | – | μ s |
| $P_{WIN(OFF)}$ | | | 0.7 | – | – | |

7. This product might not make response if input pulse width is less than the recommended value.



NOTE: This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition

Figure 8. Allowable Maximum Output Current

MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Conditions | Value | | | Unit |
|-----------------|-------------------------------------|-------|-------|------|---------|
| | | Min. | Typ. | Max. | |
| Device Flatness | See Figure 9 | 0 | – | +120 | μ m |
| Mounting Torque | Mounting Screw: M3 See Figure 10 | 0.6 | 0.7 | 0.8 | N•m |
| | | 6.2 | 7.1 | 8.1 | kg•cm |
| Weight | | – | 11.00 | – | g |

FND42060F2

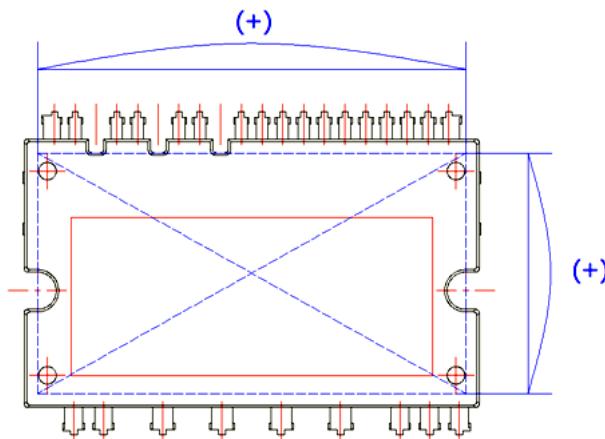


Figure 9. Flatness Measurement Position

Pre-Screwing: 1 à 2

Final Screwing: 2 à 1

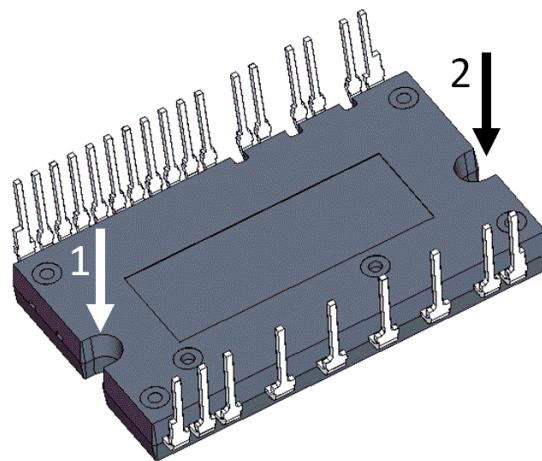


Figure 10. Mounting Screws Torque Order

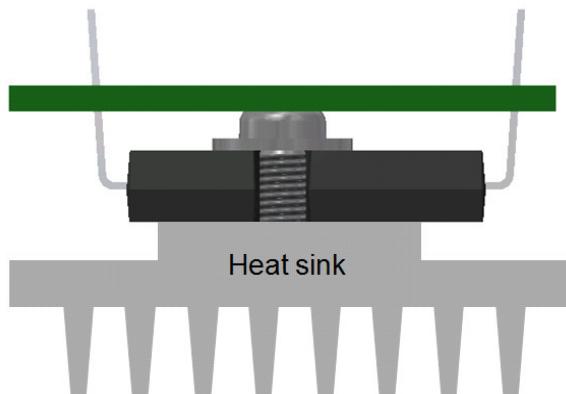
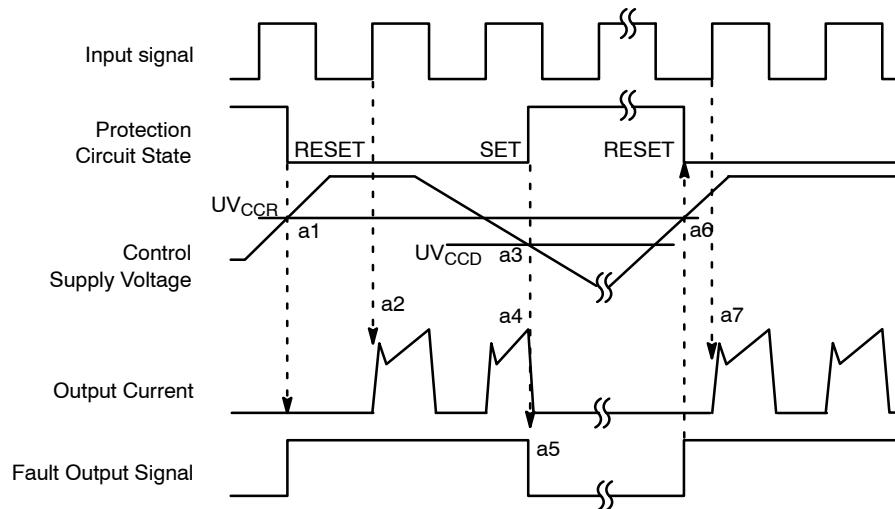


Figure 11. Recommended Heat-Sink Design

NOTES:

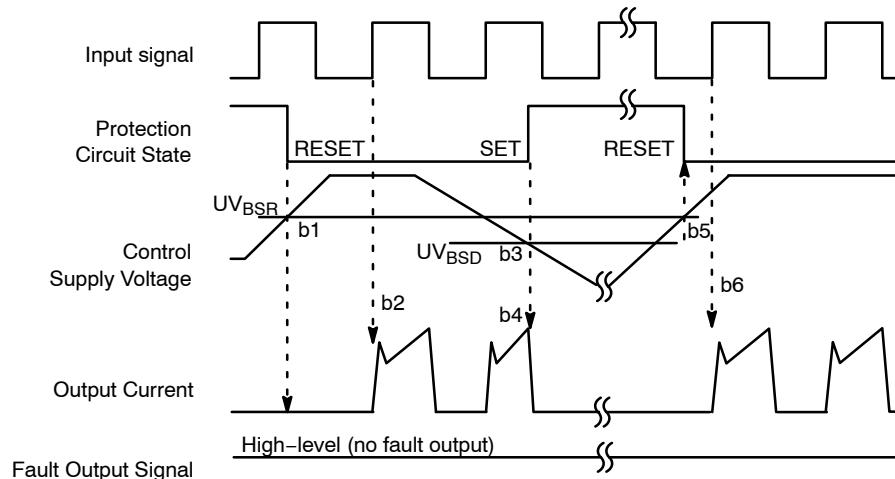
8. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat-sink destruction.
9. Avoid one side tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the SPM 45 package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

TIME CHARTS OF PROTECTIVE FUNCTION



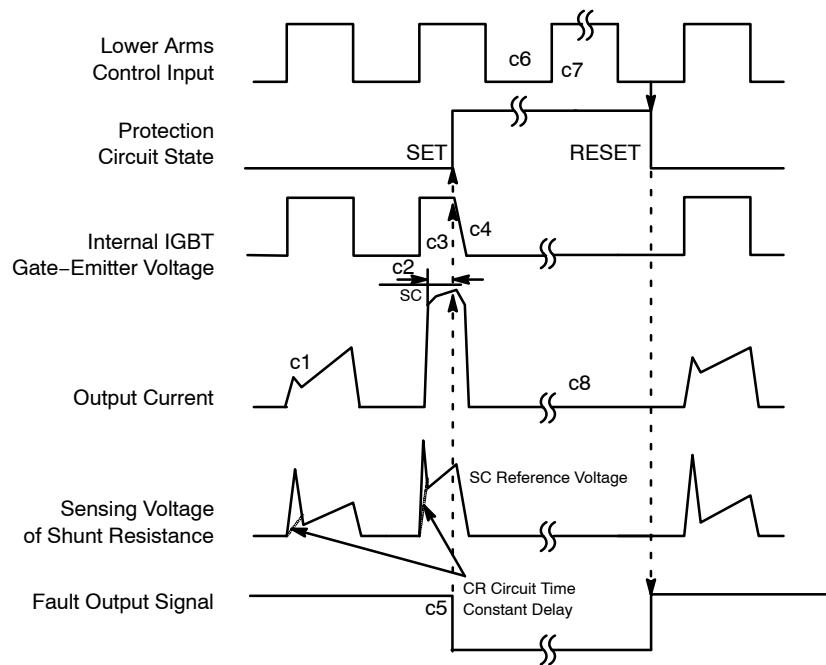
- a1: Control supply voltage rises: after the voltage rises UV_{CCR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UV_{CCD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts.
- a6: Under voltage reset (UV_{CCR}).
- a7: Normal operation: IGBT ON and carrying current.

Figure 12. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UV_{BSD}).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UV_{BSR}).
- b6: Normal operation: IGBT ON and carrying current..

Figure 13. Under-Voltage Protection (High-Side)



(with the external sense resistance and CR connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short-circuit current detection (SC trigger).

c3: Hard IGBT gate interrupt.

c4: IGBT turns OFF.

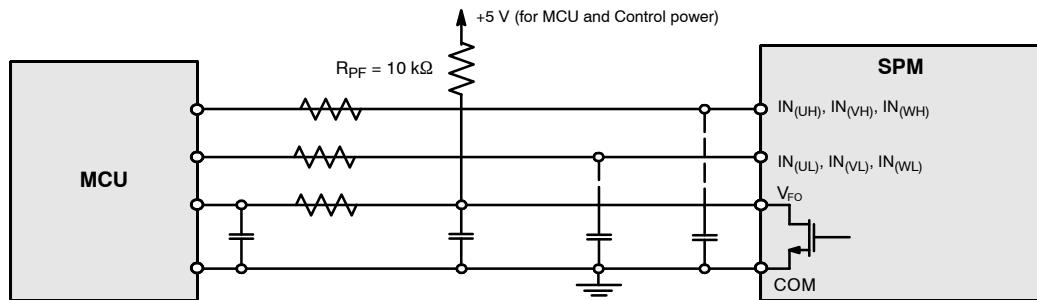
c5: Input "LOW": IGBT OFF state.

c6: Input "HIGH": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: IGBT OFF state.

Figure 14. Short-Circuit Protection (Low-Side Operation Only)

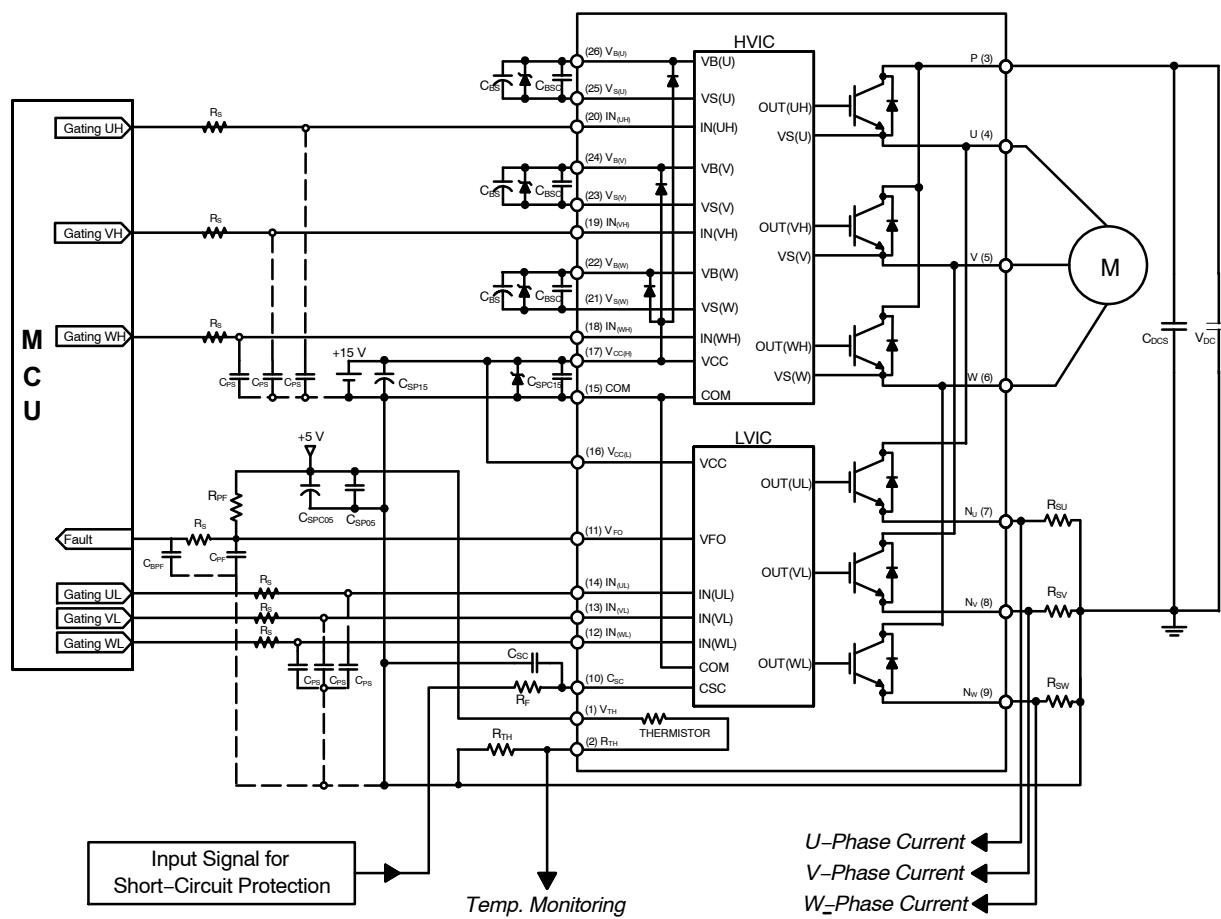
INPUT/OUTPUT INTERFACE CIRCUIT



NOTE:

10. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 45 product integrates a 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the signal voltage drop at input terminal.

Figure 15. Recommended MCU I/O Interface Circuit



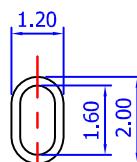
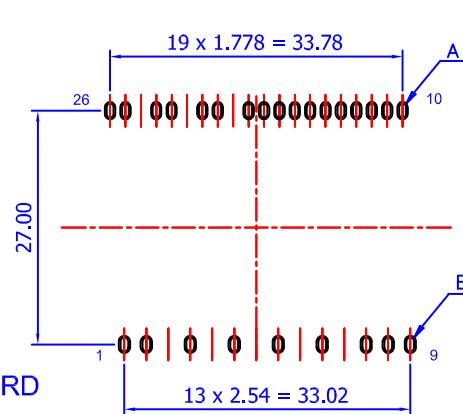
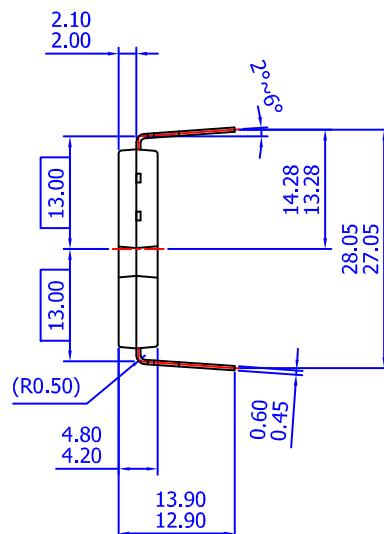
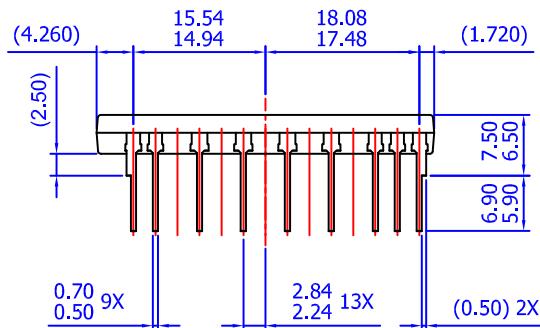
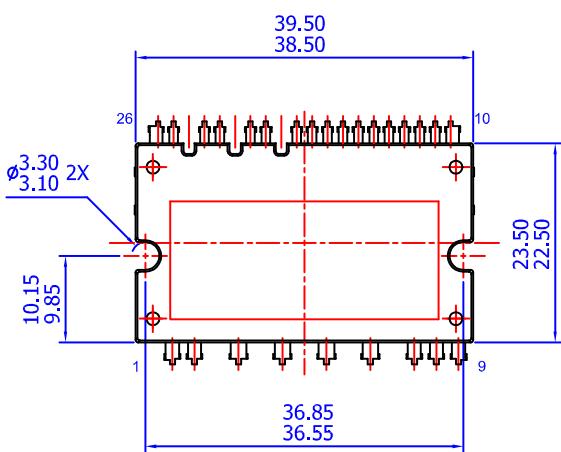
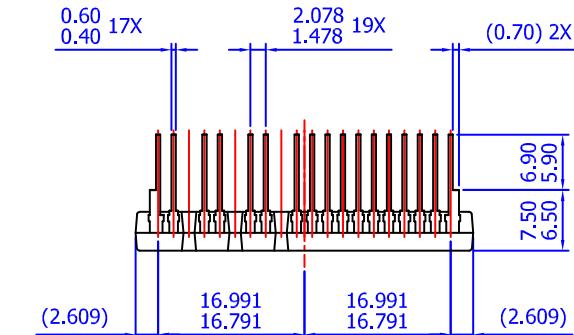
NOTES:

11. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2~3 cm).
12. By virtue of integrating an application-specific type of HVIC inside the Motion SPM 45 product, direct coupling to MCU terminals without any optocoupler or transformer isolation is possible.
13. V_{FO} output is open-drain type. The signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 1 mA (please refer to Figure 15).
14. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation. R_SC_{PS} time constant should be selected in the range 50 ~ 150 ns (recommended R_S = 100 Ω, C_{PS} = 1 nF).
15. To prevent errors of the protection function, the wiring around R_{FCSC} time constant in the range 1.5 ~ 2 μs.
16. The connection between control GND line and power GND line which includes the N_U, N_V, N_W must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
17. Each capacitor should be mounted as close to the pins of the Motion SPM 45 product as possible.
18. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μs between the P and GND pins is recommended.
19. Relays are used in almost every systems of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
20. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended zener diode is 22 V/1 W. which has the lower zener impedance characteristic than about 15 Ω).
21. Please choose the electrolytic capacitor with good temperature characteristic in C_{BS}. Also choose 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics in C_{SPSC}.
22. For the detailed information, please refer to the [AN-9070](#), [AN-9071](#), [AN-9072](#), RD-344 and RD-345.

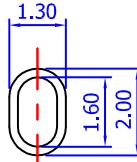
Figure 16. Typical Application Circuit

SPMAA-C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE
CASE MODFC
ISSUE O

DATE 31 JAN 2017



DETAIL A
(SCALE N/A)



DETAIL B
(SCALE N/A)

LAND PATTERN RECOMMENDATIONS

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