User's Guide

TPS62134x Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of Texas Instrument's TPS62134x evaluation modules (EVMs). The TPS62134xEVM-595 facilitates the evaluation of the TPS62134x Step-Down Converter with Low Power Mode Input and Output Voltage Selection device. The device outputs a user-selectable output voltage between 0.8 V and 1.05 V with a low-power mode from input voltages between 3 V and 17 V. These devices are compatible with the Intel® Skylake platform's special power requirements for the VccIO, VccPRIM_CORE, and VccEDRAM / VccEOPIO rails. This user's guide includes setup instructions for the hardware, a printed-circuit board layout for the EVM, a schematic diagram, a bill of materials, and test results for the EVM.

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1 Introduction

The TPS62134x is a synchronous, step-down converter in a 3×3-mm, 16-pin QFN package. Four different versions are available and each has their own EVM: TPS62134AEVM-595 (PWR595-001), TPS62134BEVM-595 (PWR595-002), TPS62134CEVM-595 (PWR595-003), and TPS62134DEVM-595 (PWR595-004). The versions differ in their output voltage setpoints and low-power mode output voltage. The TPS62134A is compatible with the Intel Skylake platform's VccIO rail. The TPS62134B and TPS62134D are compatible with the Intel Skylake platform's VccPRIM_CORE rail. The TPS62134C is compatible with the Intel Skylake platform's VccEDRAM / VccEOPIO rail.

1.1 Performance Specification

Table 1-1 provides a summary of the TPS62134xEVM-595 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1-1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input voltage		3		17	V
Output voltage setpoint	TPS62134AEVM-595, $\overline{LPM}$ = High	0.85		0.975	V
Output voltage setpoint	TPS62134BEVM-595, $\overline{LPM}$ = High	0.8		0.95	V
Output voltage setpoint	TPS62134CEVM-595, $\overline{LPM}$ = High	0.8		1.05	V
Output voltage setpoint	TPS62134DEVM-595, $\overline{LPM}$ = High	0.85		1	V
Output current	V_{IN} ≥ 5 V	0		3.2	A
		0		3	A
Soft-start time	Ramp time of V_{OUT}, V_{OUT} = 0.95 V		180		µs

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate any version of the integrated circuit (IC). Additional input and output capacitors can also be added. Finally, the loop response of the IC can be measured.

1.2.1 Input and Output Capacitors

C9 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.

C5, C6, C7, and C8 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response. The total output capacitance must remain within the recommended range in the data sheet (SLVSC20) for proper operation.

1.2.2 Loop Response Measurement

The loop response of the TPS62134xEVM-595 can be measured with two simple changes to the circuitry. First, install a 10-Ω, 0603-sized resistor across the pads of R2 in the middle of the back of the PCB. Second, cut the plane between the via near the VOS pin and the output capacitor C2 and the inductor. This change is shown in Figure 1-1. With these changes, an ac signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added resistor. The results of this test are shown in Figure 3-2.

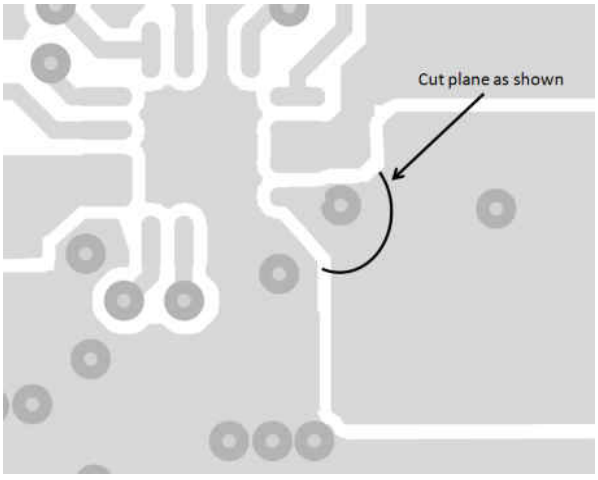

Figure 1-1. Loop Response Measurement Modification

2 Setup

This section describes how to properly use the TPS62134xEVM-595.

2.1 Input/Output Connector Descriptions

J1 – VIN	Positive input connection from the input supply for the EVM
J2 – S+/S–	Input voltage sense connections. Measure the input voltage at this point.
J3 – GND	Return connection from the input supply for the EVM
J4 – VOUT	Output voltage connection
J5 – S+/S–	Output voltage sense connections. Measure the output voltage at this point.
J6 – GND	Output return connection
J7 – PG/GND	The PG output appears on pin 1 of this header with a convenient ground on pin 2
J8 – SS/GND	The SS pin voltage appears on pin 2 of this header with a convenient ground on pin 1
J9 – Vdd/GND	An externally applied voltage must be applied on pin 2 of this header with a convenient ground on pin 1. This voltage must remain between 0.8 V and 6 V. This voltage level sets the logic high level for the VID0, VID1, and $\overline{\text{LPM}}$ pins as well as the PG pin pull-up voltage.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.
JP2 – VID0	VID0 pin input jumper. Place the supplied jumper across HIGH and VID0 to set the VID0 pin high. Place the jumper across LOW and VID0 to set the VID0 pin low.
JP3 – VID1	VID1 pin input jumper. Place the supplied jumper across HIGH and VID1 to set the VID1 pin high. Place the jumper across LOW and VID1 to set the VID1 pin low.
JP4 – $\overline{\text{LPM}}$	$\overline{\text{LPM}}$ pin input jumper. Place the supplied jumper across HIGH and $\overline{\text{LPM}}$ to disable the low power mode. Place the jumper across LOW and $\overline{\text{LPM}}$ to enable the low power mode.
JP5 – PG Pullup Voltage	PG pin pullup voltage jumper. Place the supplied jumper on JP5 to connect the PG pin pullup resistor to Vdd. Alternatively, the jumper can be removed and a different voltage can be supplied on pin 1 to pull up the PG pin to a different level. This externally applied voltage must remain below 7 V.

2.2 Setup

To operate the EVM, set jumpers JP1 through JP5 to the desired positions per Section 2.1. Connect the input supply to J1 and J3 and connect the load to J4 and J6. Connect a second input supply to J9.

3 TPS62134xEVM-595 Test Results

The TPS62134xEVM-595 was used to take the data in the TPS62134x data sheet. See the device data sheet (SLVSC20) for the performance of this EVM.

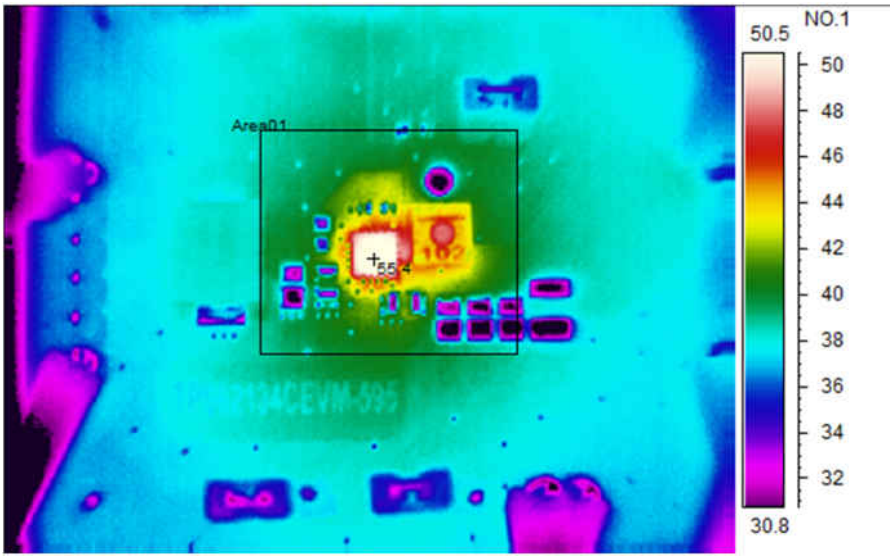

Figure 3-1. Thermal Performance (V_{IN} = 17 V, V_{OUT} = 1.05 V, Load = 3.2 A)

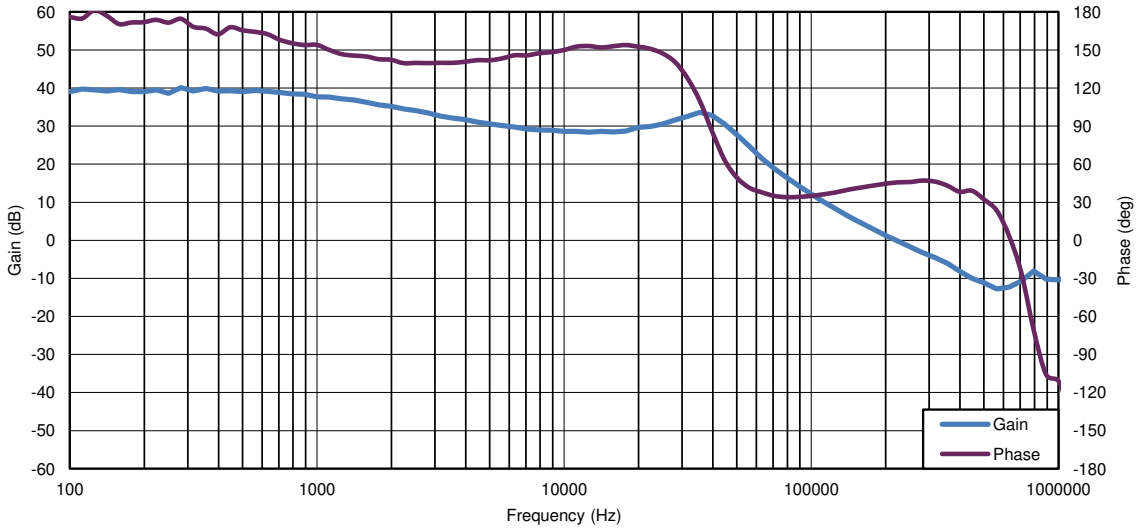

Figure 3-2. Loop Measurement (V_{IN} = 12 V, V_{OUT} = 1 V, Load = 3 A)

4 Board Layout

This section provides the TPS62134xEVM-595 board layout and illustrations.

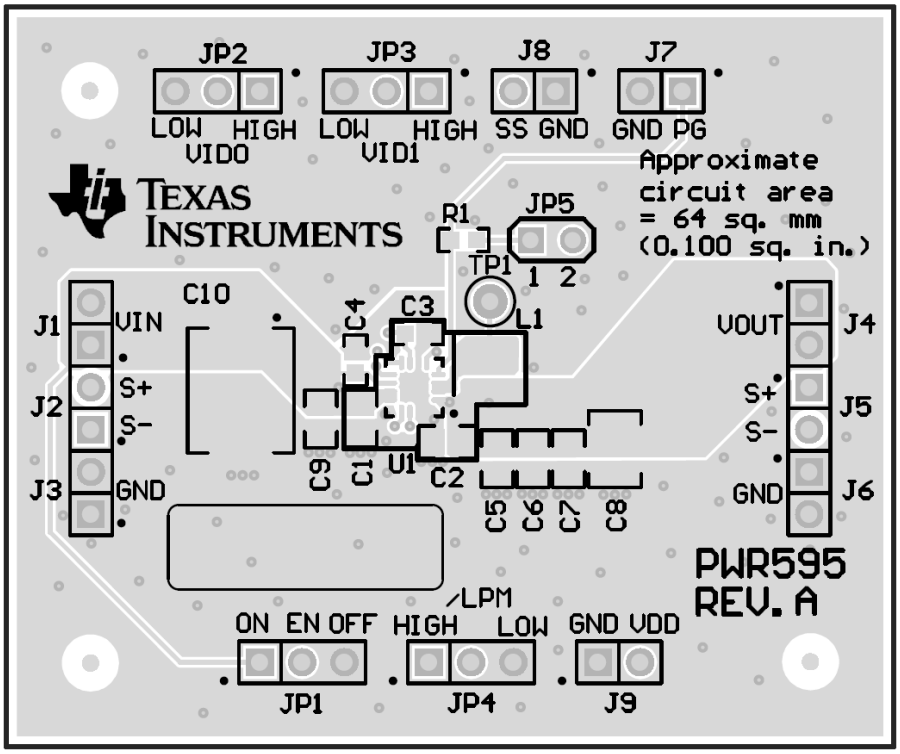

Figure 4-1. Assembly Layer

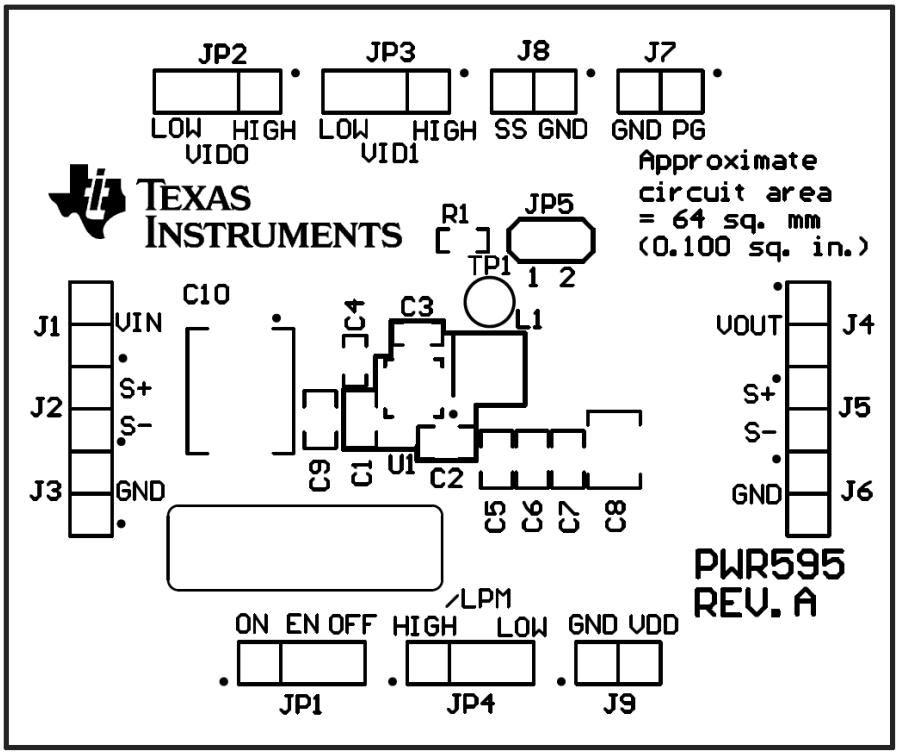

Figure 4-2. Top Silk Layer

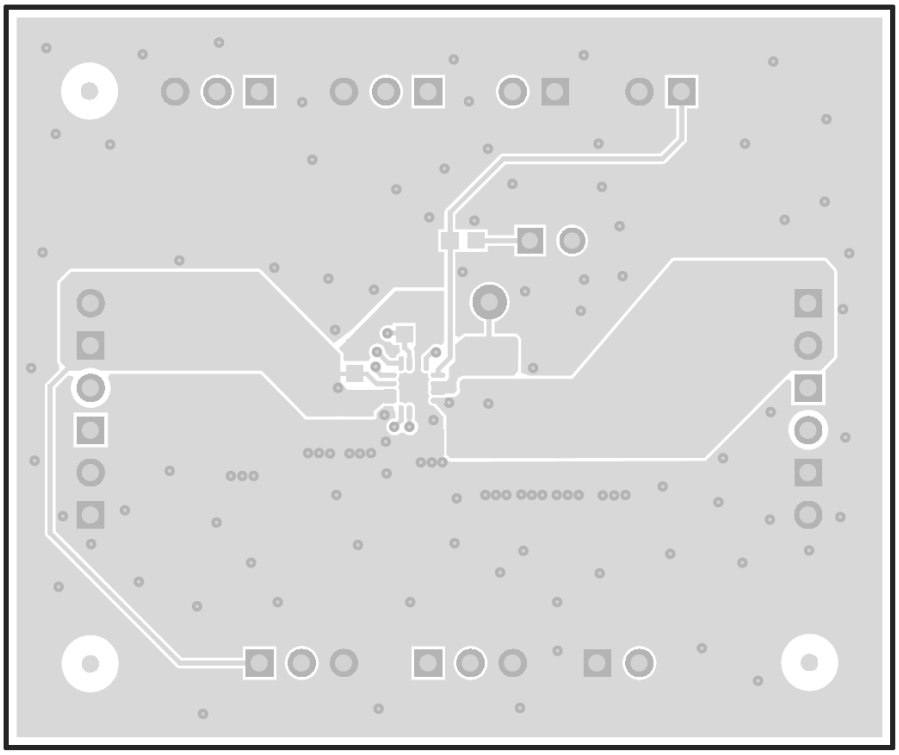

Figure 4-3. Top Layer

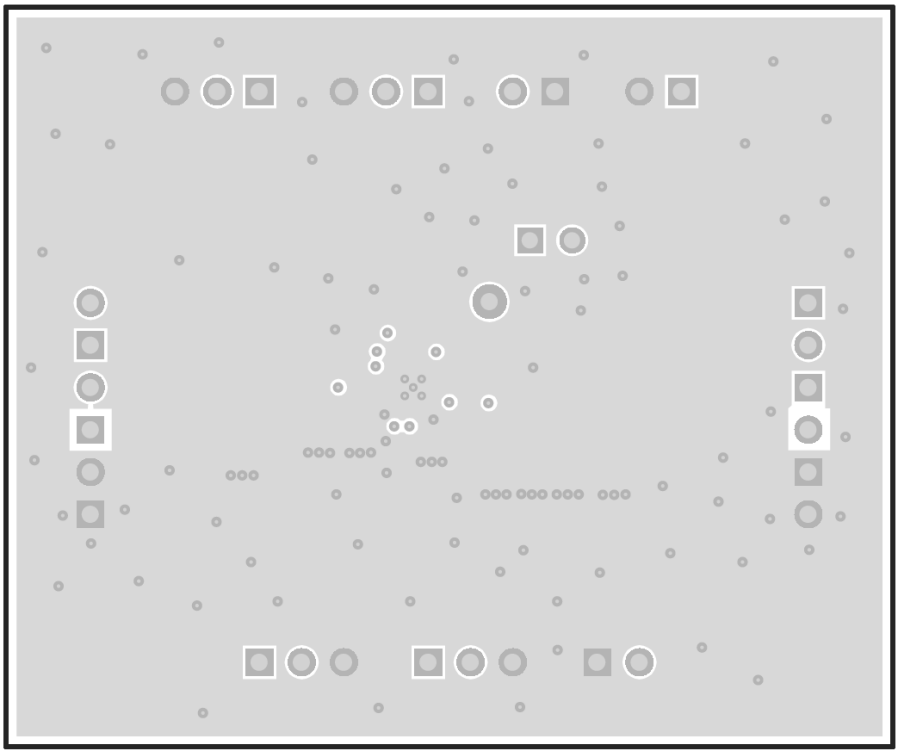

Figure 4-4. Internal Layer 1

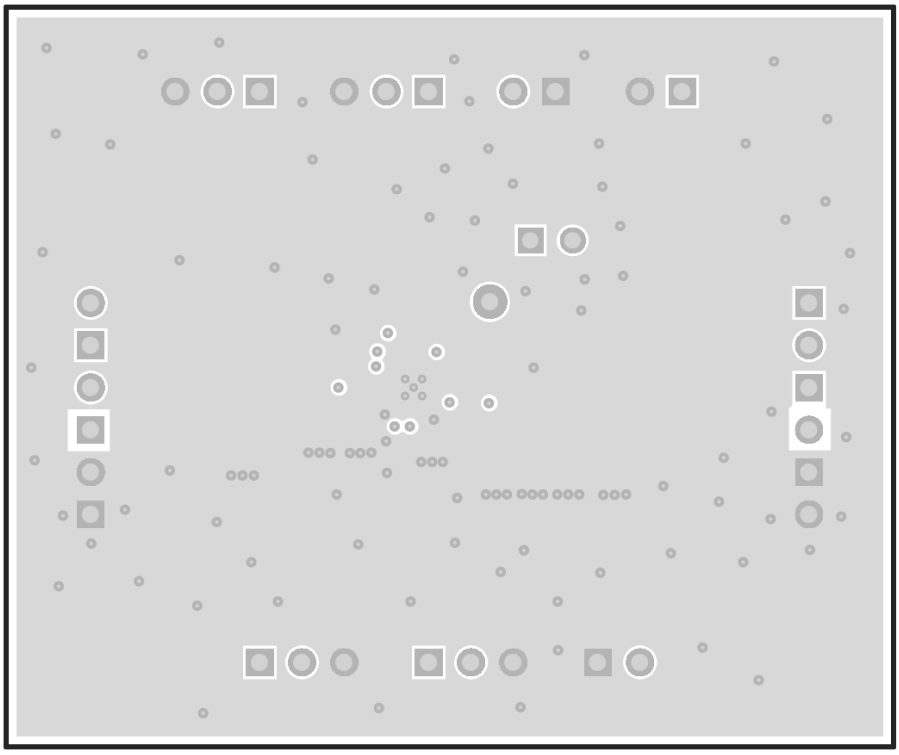

Figure 4-5. Internal Layer 2

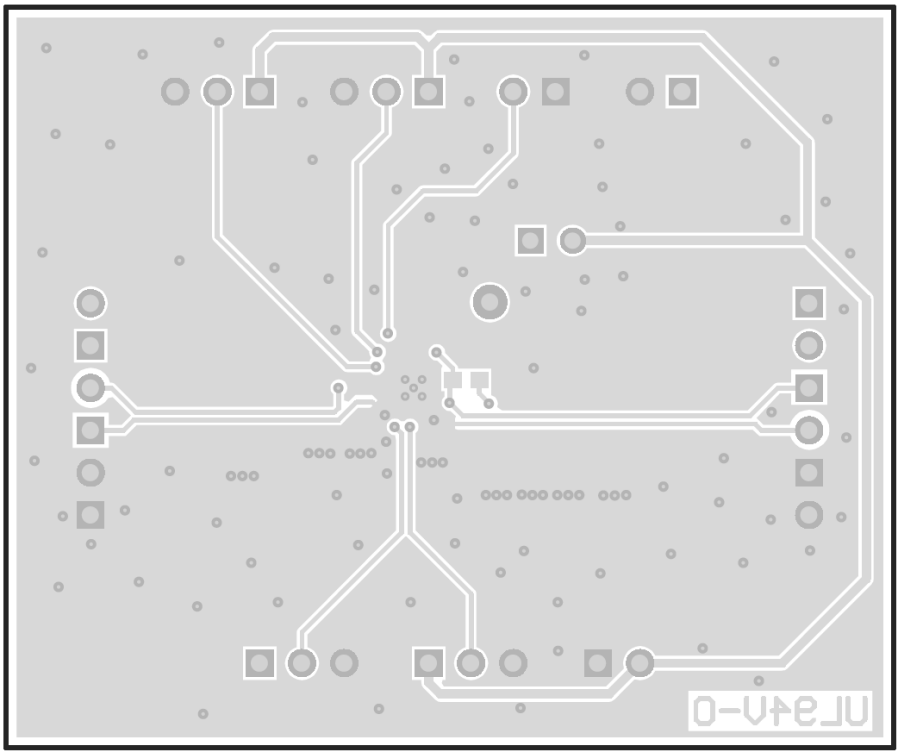

Figure 4-6. Bottom Layer

5 Schematic and Bill of Materials

This section provides the TPS62134xEVM-595 schematic and bill of materials.

5.1 Schematic

Figure 5-1 illustrates the TPS62134xEVM-595 schematic.

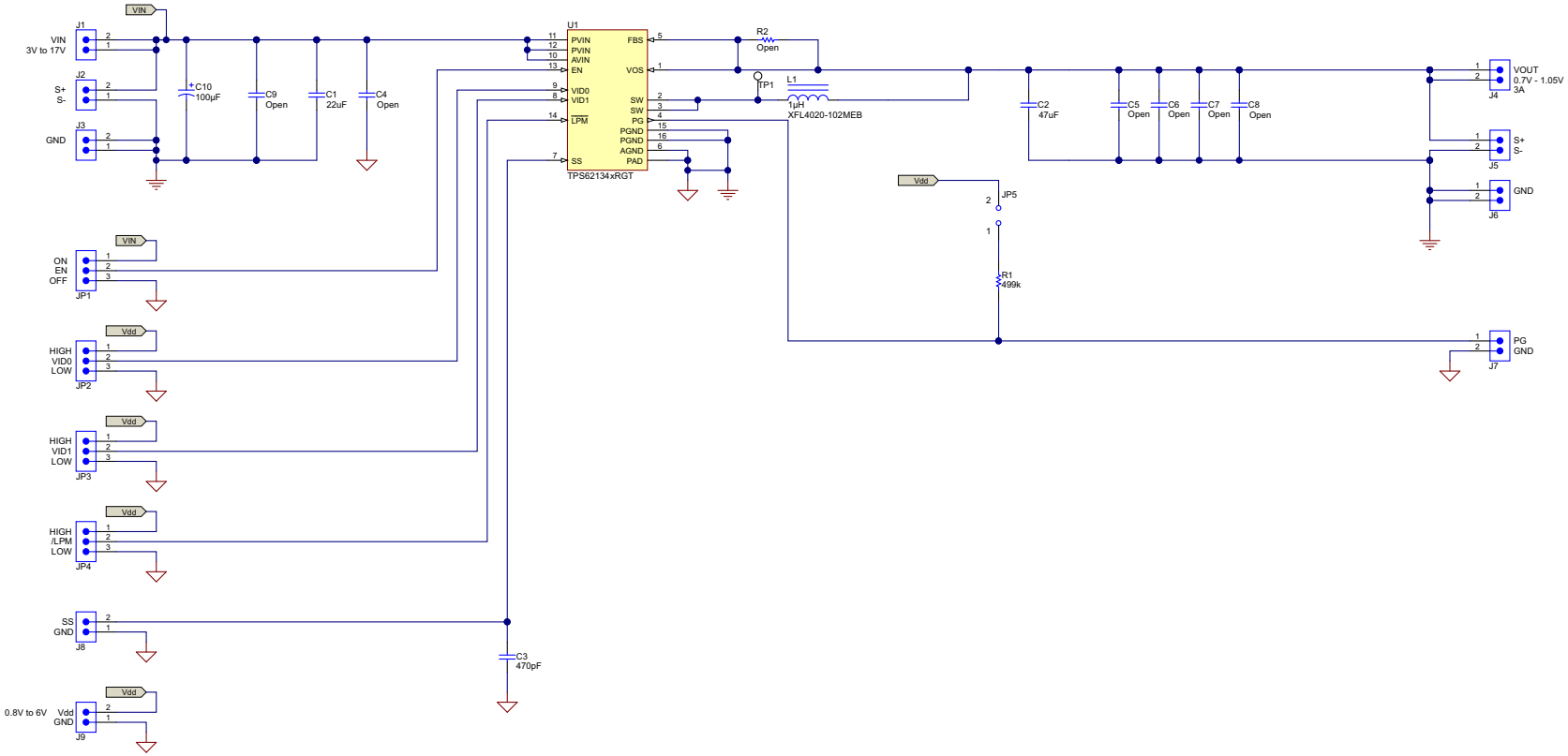

Figure 5-1. TPS62134xEVM-595 Schematic

5.2 Bill of Materials

Table 5-1 lists the BOM for this EVM.

Table 5-1. TPS62134xEVM-595 Bill of Materials

Count				Ref Des	Value	Description	Size	Part Number	MFR
PWR595-001	PWR595-002	PWR595-003	PWR595-004						
1	1	1	1	C1	22uF	Capacitor, Ceramic, 25V, X5R, 20%	0805	GRM21BR61E226ME44	Murata
1	1	1	1	C2	47uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	GRM21BR60J476ME15	Murata
1	1	1	1	C3	470pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	GRM188R71H471KA01D	Murata
1	1	1	1	C10	100uF	Capacitor, Tantalum, 25V, ±10%, 100 mOhm	7361	TPSV107K025R0100	AVX
1	1	1	1	L1	1uH	Inductor, Power, 5.4 A, 10.8 mOhm	4 mm x 4 mm	XFL4020-102MEB	Coilcraft
1	1	1	1	R1	499k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	0	0	0	U1	TPS62134A	IC, 17-V Input, Step-down Converter with Low Power Mode Input for Intel Skylake Platform	3 mm x 3 mm	TPS62134ARGT	TI
0	1	0	0	U1	TPS62134B	IC, 17-V Input, Step-down Converter with Low Power Mode Input for Intel Skylake Platform	3 mm x 3 mm	TPS62134BRGT	TI
0	0	1	0	U1	TPS62134C	IC, 17-V Input, Step-down Converter with Low Power Mode Input for Intel Skylake Platform	3 mm x 3 mm	TPS62134CRGT	TI
0	0	0	1	U1	TPS62134D	IC, 17-V Input, Step-down Converter with Low Power Mode Input for Intel Skylake Platform	3 mm x 3 mm	TPS62134DRGT	TI

The TPS62134xEVM-595 may be populated with TPS62134x (U1) devices that do not contain the correct top side markings on the top of the device itself. These devices are still fully tested TPS62134x devices and meet the specified electrical characteristics of the data sheet.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2015) to Revision B (June 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated user's guide title	2

Changes from Revision * (November 2014) to Revision A (March 2015)	Page
• Added "TPS62134DEVM-595 (PWR595-004)." to Section 1	2
• Added "TPS62134DEVM-595," to Table 1-1	3
• Added column "PWR595-004" to Table 5-1	10

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