

# SN54HC365, SN74HC365 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

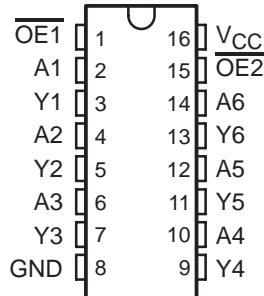
SCLS308D – JANUARY 1996 – REVISED OCTOBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines, Buffer-Memory Address Registers, or Drive Up To 15 LSTTL Loads
- True Outputs
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 10$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

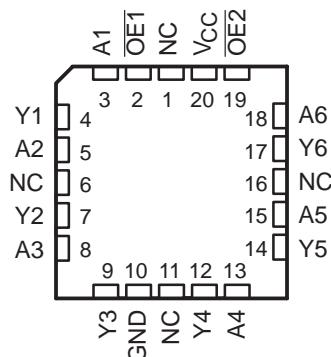
## description/ordering information

These hex buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC365 devices contain six independent buffers/drivers with dual-gated output-enable ( $\overline{OE}_1$  and  $\overline{OE}_2$ ) inputs. When  $\overline{OE}_1$  and  $\overline{OE}_2$  are both low, the devices pass noninverted data from the A inputs to the Y outputs. If either (or both) output-enable terminal(s) is high, the outputs are in the high-impedance state.

SN54HC365 . . . J OR W PACKAGE  
SN74HC365 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC365 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC365N	SN74HC365N
	SOIC – D	Tube of 40	SN74HC365D	HC365
		Reel of 2500	SN74HC365DR	
		Reel of 250	SN74HC365DT	
	SOP – NS	Reel of 2000	SN74HC365NSR	HC365
	TSSOP – PW	Reel of 90	SN74HC365PW	HC365
		Reel of 2000	SN74HC365PWR	
		Reel of 250	SN74HC365PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC365J	SNJ54HC365J
	CFP – W	Tube of 150	SNJ54HC365W	SNJ54HC365W
	LCCC – FK	Tube of 55	SNJ54HC365FK	SNJ54HC365FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

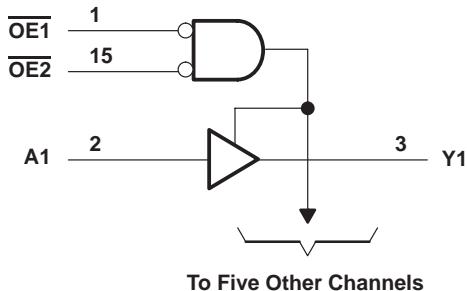
# SN54HC365, SN74HC365 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS308D – JANUARY 1996 – REVISED OCTOBER 2003

## FUNCTION TABLE (each buffer/driver)

INPUTS			OUTPUT
OE1	OE2	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

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HEX BUFFERS AND LINE DRIVERS  
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**recommended operating conditions (see Note 3)**

			SN54HC365			SN74HC365			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5			0.5		V
		V <sub>CC</sub> = 4.5 V		1.35			1.35		
		V <sub>CC</sub> = 6 V		1.8			1.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
Δt/ΔV	Input transition rise/fall time	V <sub>CC</sub> = 2 V		1000			1000		ns
		V <sub>CC</sub> = 4.5 V		500			500		
		V <sub>CC</sub> = 6 V		400			400		
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85		°C	

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC365		SN74HC365		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		1.9		V	
			4.5 V	4.4	4.499	4.4		4.4			
			6 V	5.9	5.999	5.9		5.9			
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3	3.7		3.84			
			6 V	5.48	5.8	5.2		5.34			
		I <sub>OL</sub> = 20 μA	2 V		0.002	0.1	0.1		0.1		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		4.5 V		0.001	0.1	0.1		0.1		
			6 V		0.001	0.1	0.1		0.1		
			I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26	0.4	0.33		
			I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26	0.4	0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V		±0.01	±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160	160	80	80	μA	
C <sub>i</sub>		2 V to 6 V		3	10	10	10	10	10	pF	

**SN54HC365, SN74HC365  
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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC365	SN74HC365	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V	50	95	145	120	120	ns
			4.5 V	12	19	29	24	24	
			6 V	10	16	25	20	20	
t <sub>en</sub>	OE	Y	2 V	100	190	285	238	238	ns
			4.5 V	26	38	57	48	48	
			6 V	21	32	48	41	41	
t <sub>dis</sub>	OE	Y	2 V	50	175	265	240	240	ns
			4.5 V	21	35	53	48	48	
			6 V	19	30	45	41	41	
t <sub>t</sub>		Any	2 V	28	60	90	75	75	ns
			4.5 V	8	12	18	15	15	
			6 V	6	10	15	13	13	

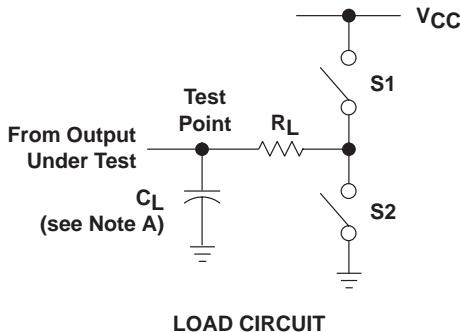
**switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC365	SN74HC365	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V	70	120	180	150	150	ns
			4.5 V	17	24	36	30	30	
			6 V	14	20	31	25	25	
t <sub>en</sub>	OE	Y	2 V	140	230	345	285	285	ns
			4.5 V	30	46	69	57	57	
			6 V	28	39	59	48	48	
t <sub>t</sub>		Any	2 V	45	210	315	265	265	ns
			4.5 V	17	42	63	53	53	
			6 V	13	36	53	45	45	

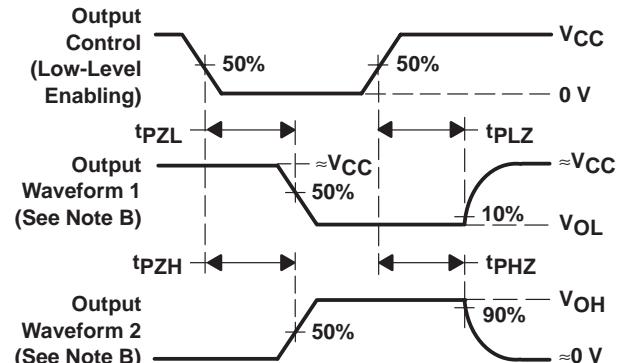
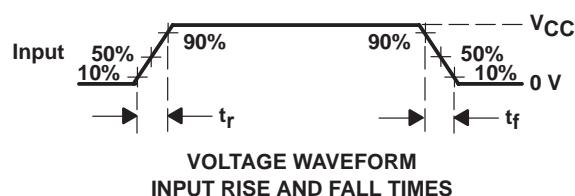
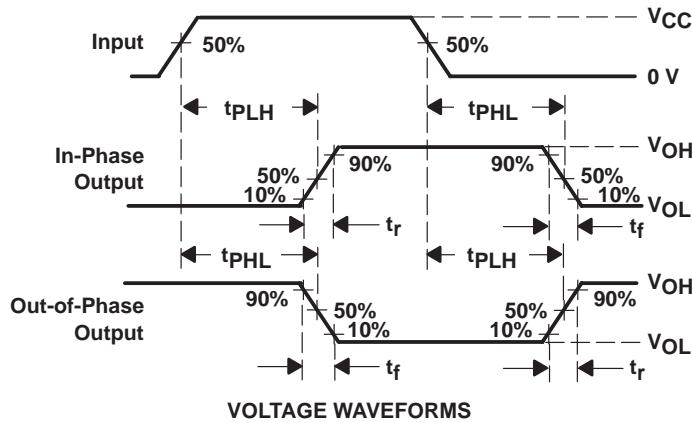
**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF	Open	Closed
		or 150 pF	Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
		or 150 pF	Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8500101EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8500101EA SNJ54HC365J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/65706BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65706BEA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/65706BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65706BEA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54HC365J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC365J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365DRE4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85		<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC365N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC365N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC365PWTE4	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC365	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54HC365J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8500101EA SNJ54HC365J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3) MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC365, SN74HC365 :**

- Catalog : [SN74HC365](#)
- Military : [SN54HC365](#)

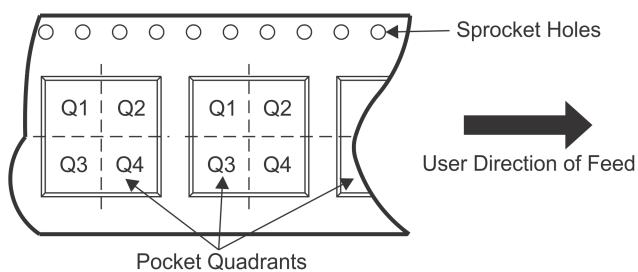
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


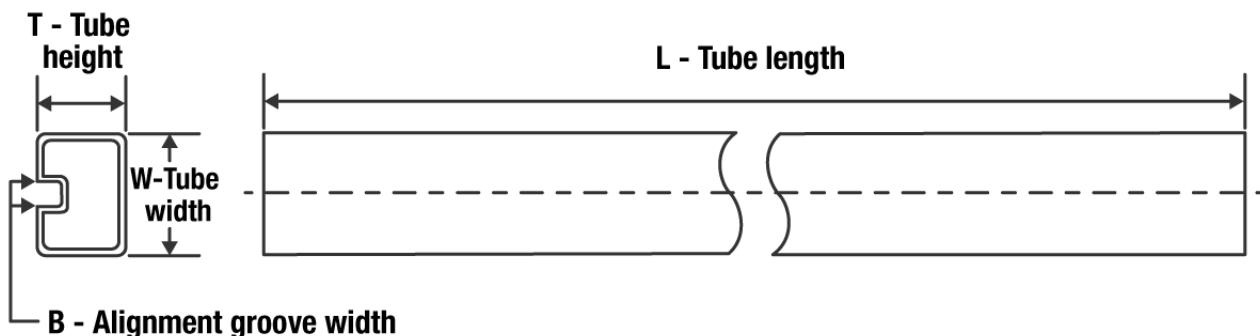
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC365DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC365NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC365PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC365PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC365DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC365NSR	SO	NS	16	2000	853.0	449.0	35.0
SN74HC365PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74HC365PWT	TSSOP	PW	16	250	853.0	449.0	35.0

**TUBE**


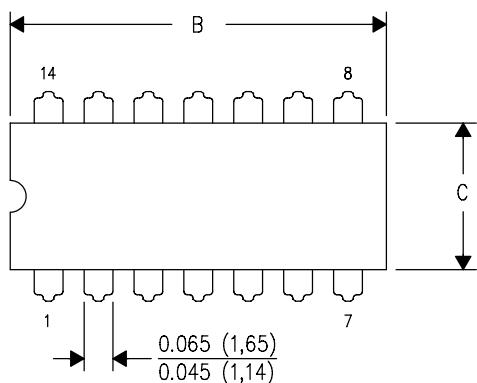
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC365D	D	SOIC	16	40	507	8	3940	4.32
SN74HC365N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC365N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC365NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC365NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC365PW	PW	TSSOP	16	90	530	10.2	3600	3.5

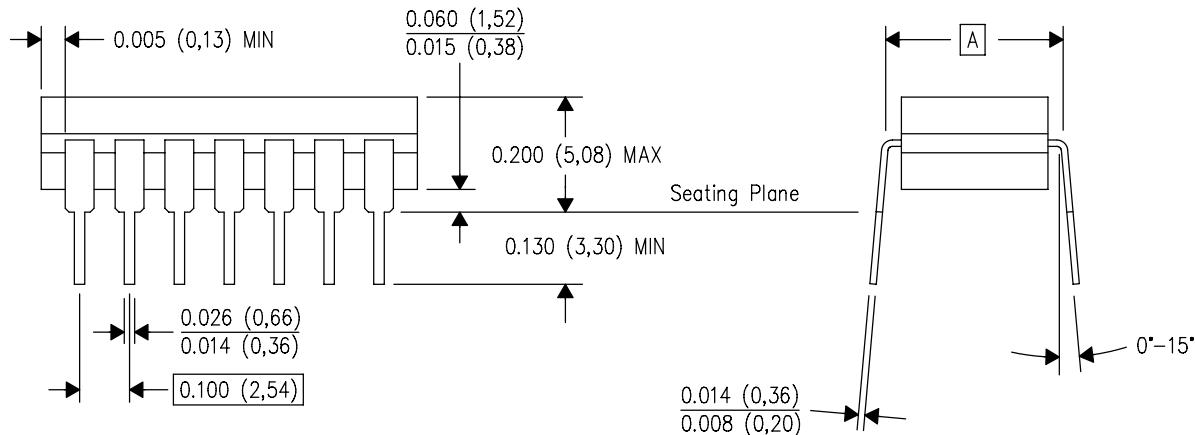
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



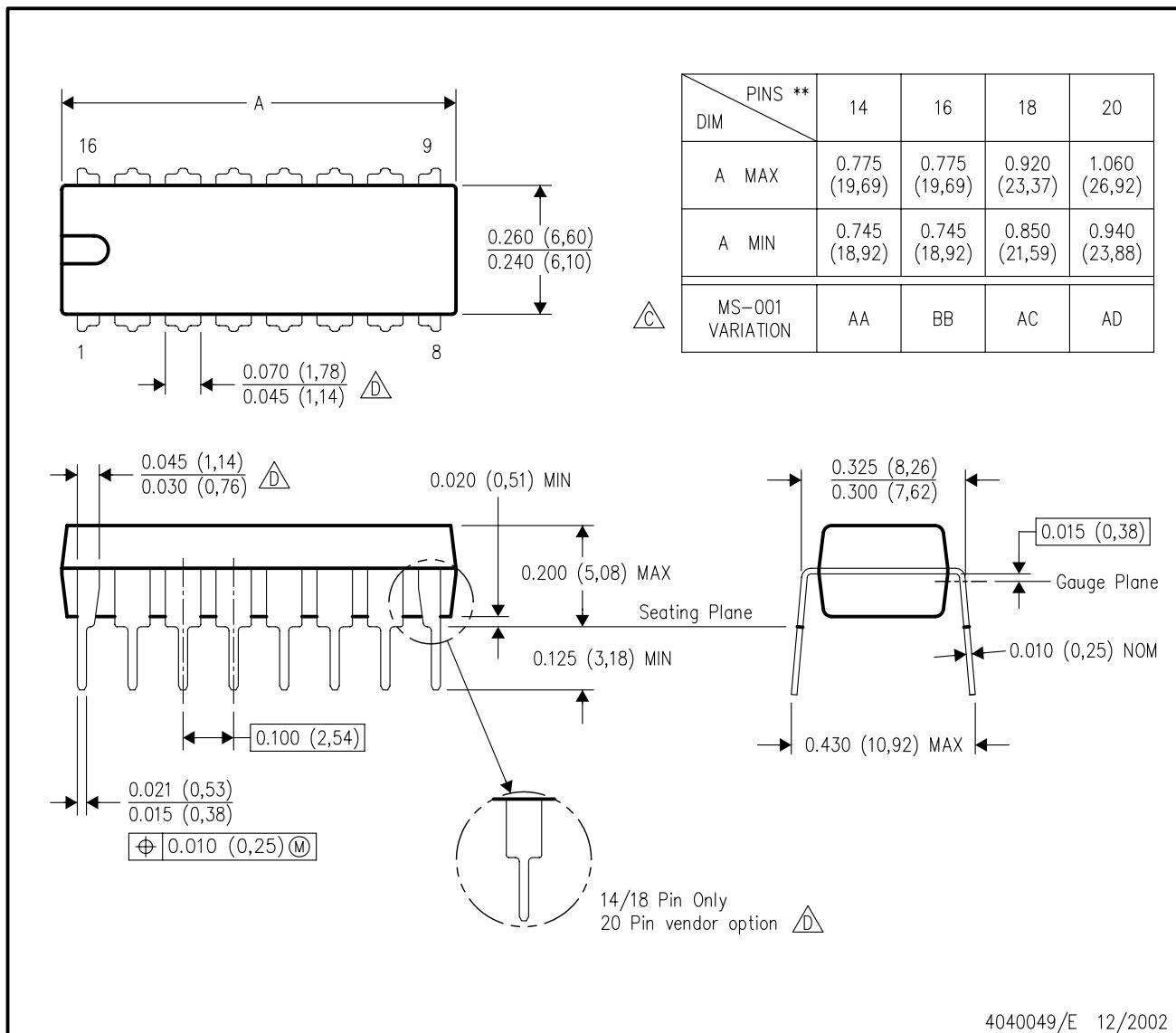
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

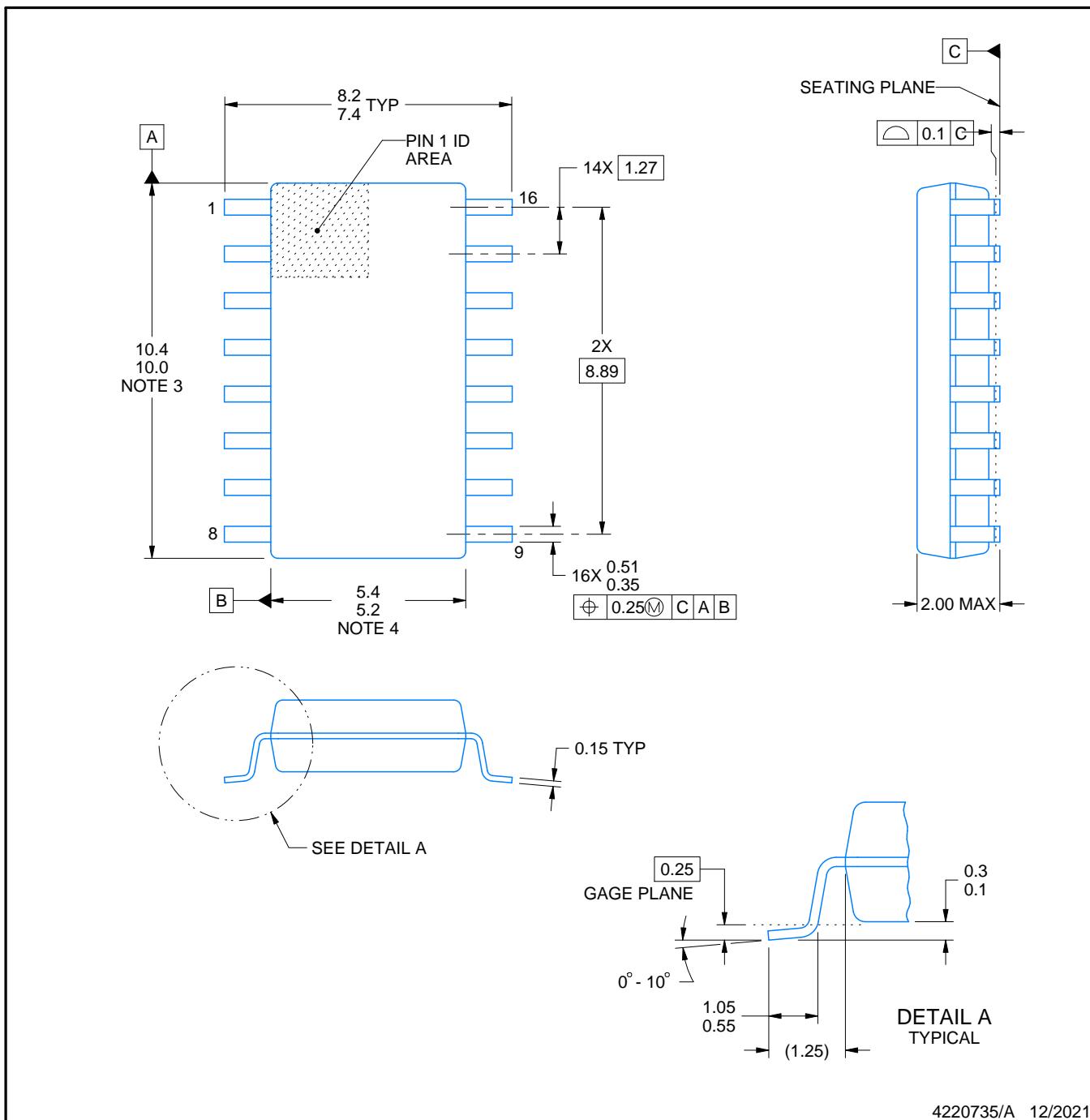
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## SOP - 2.00 mm max height

SOP



4220735/A 12/2021

### NOTES:

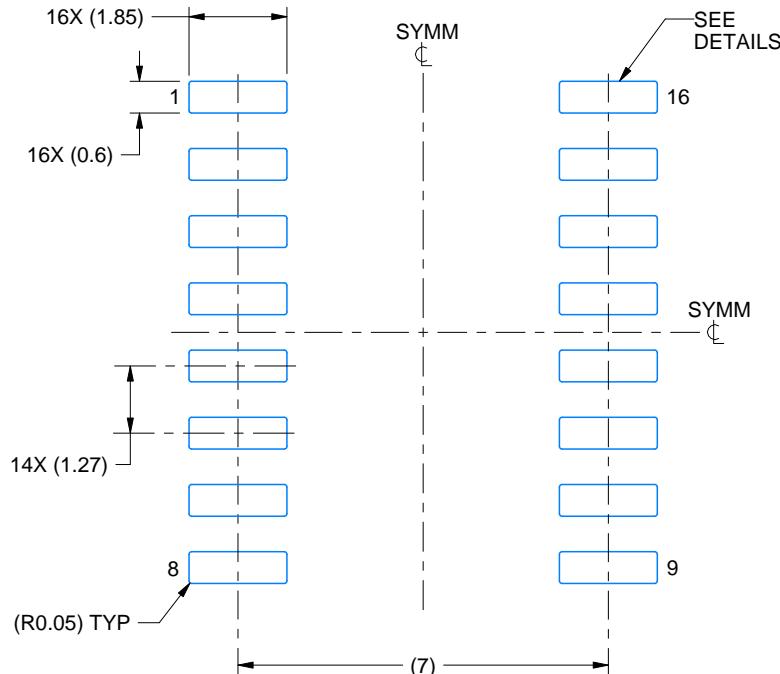
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

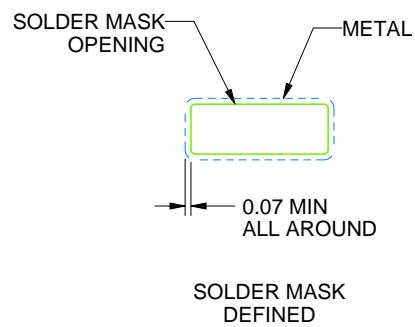
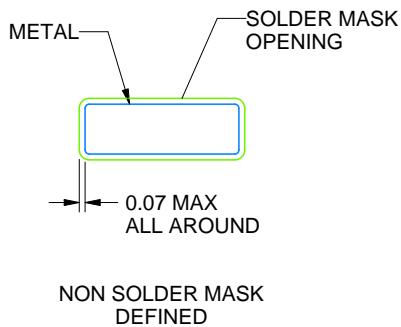
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

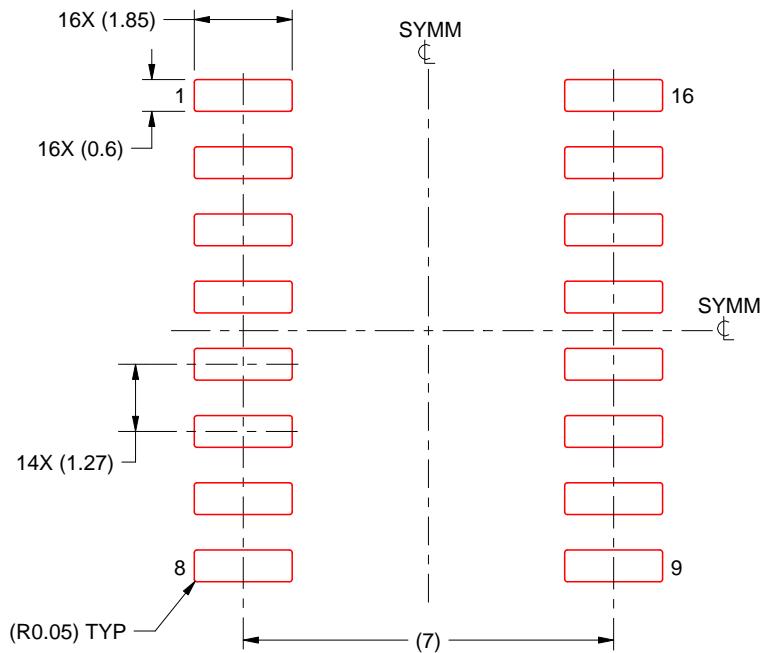
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

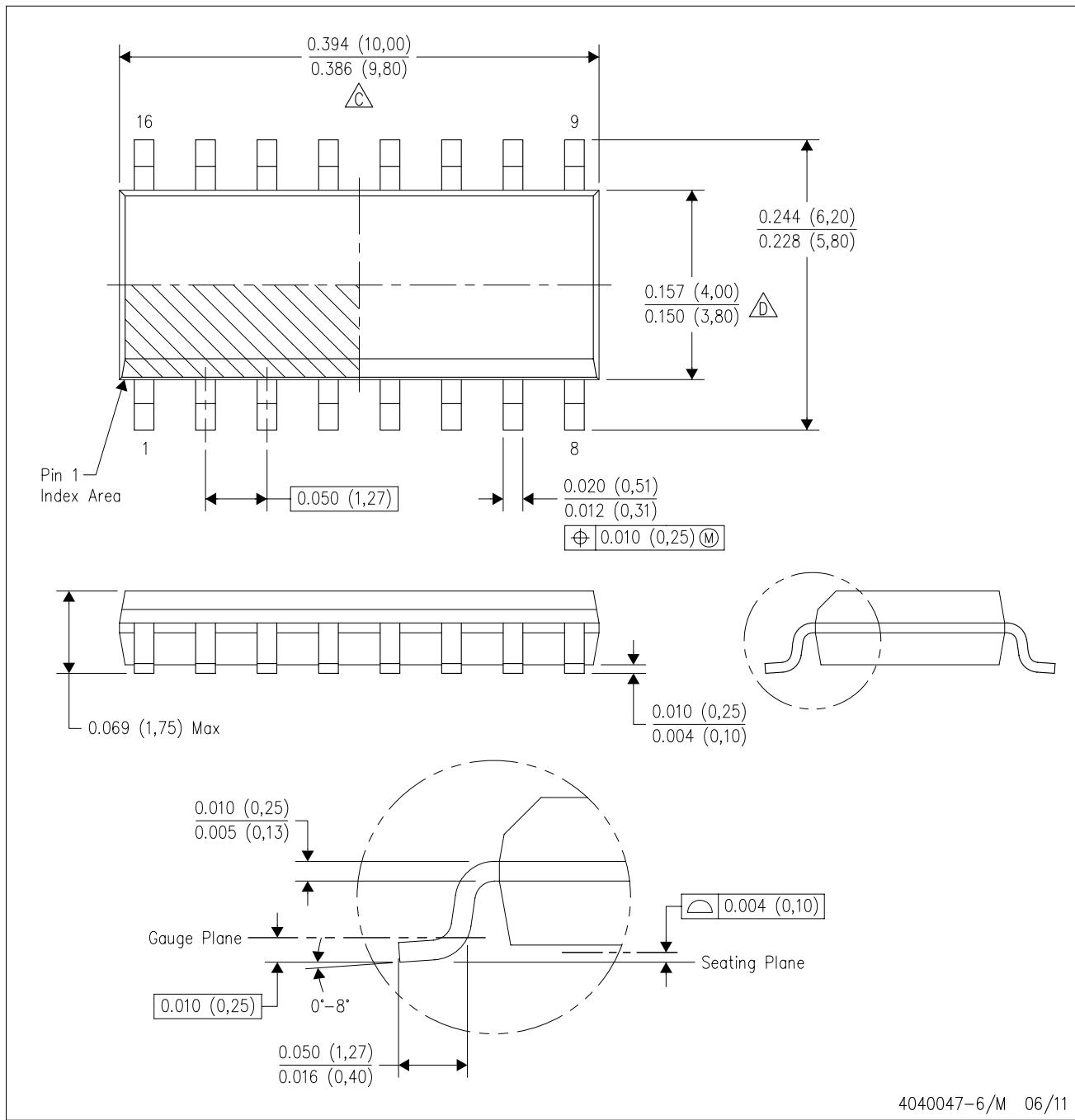
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

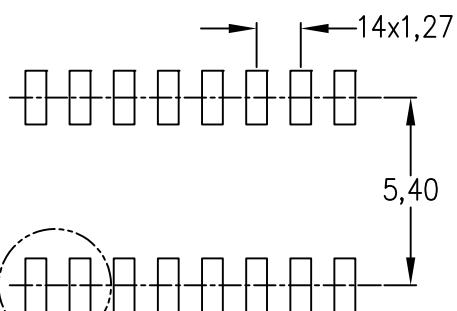
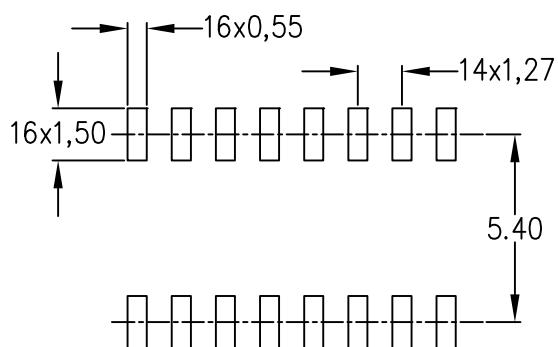
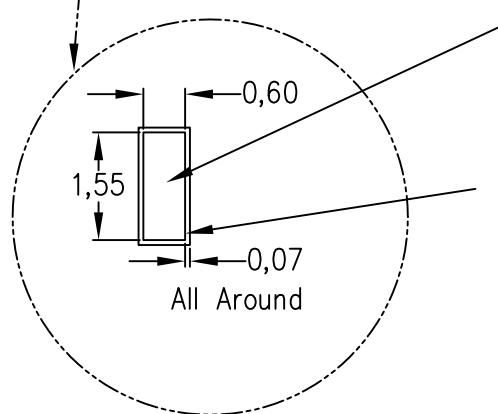
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

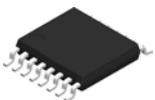
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

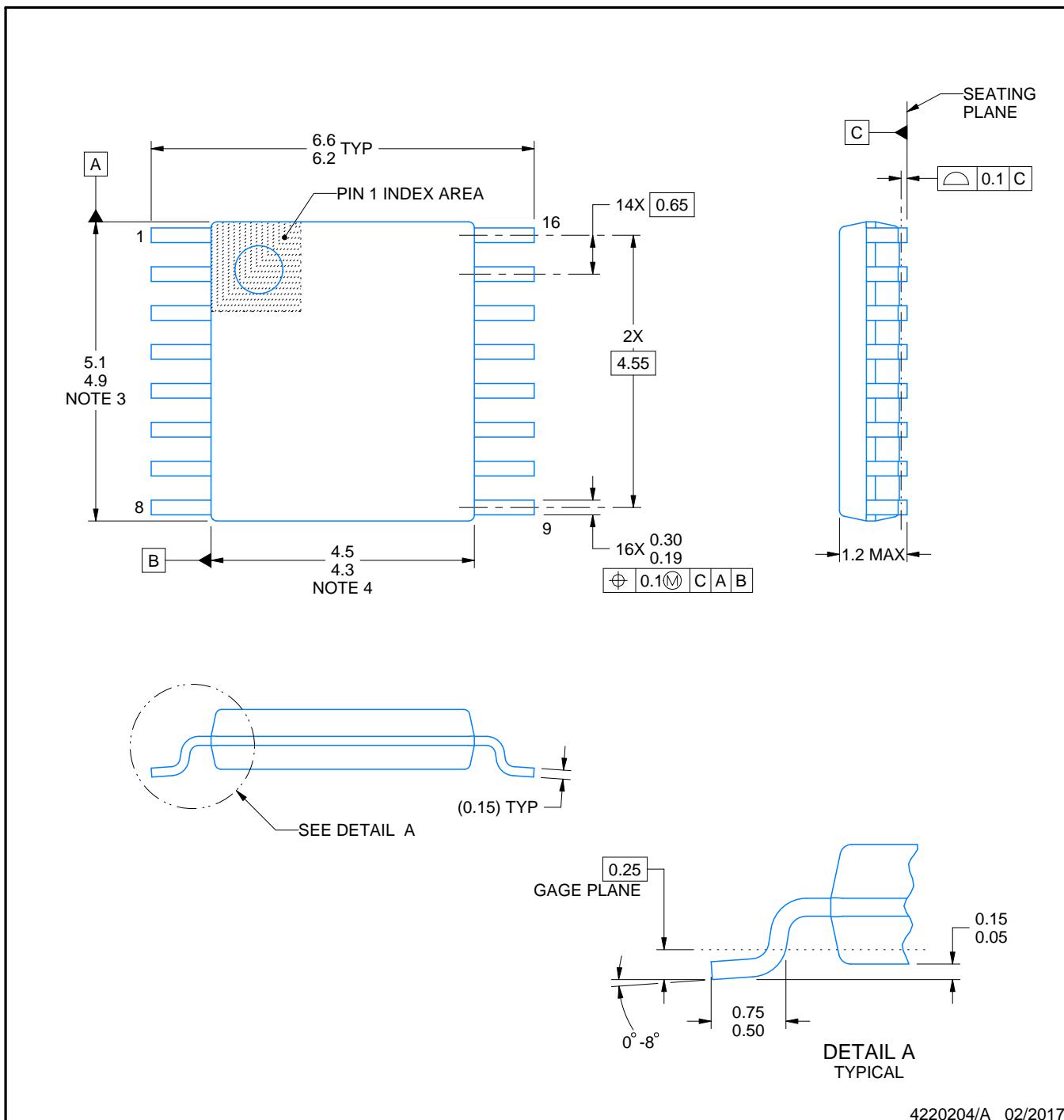
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

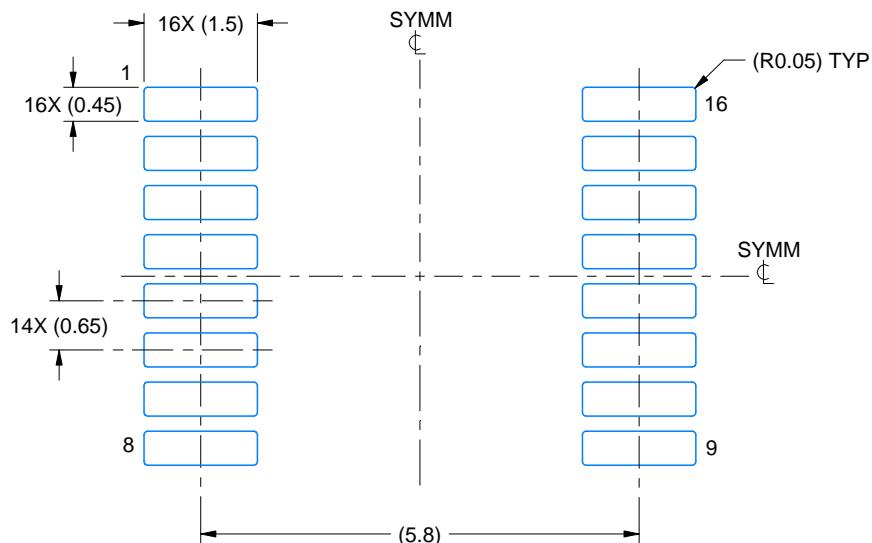
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

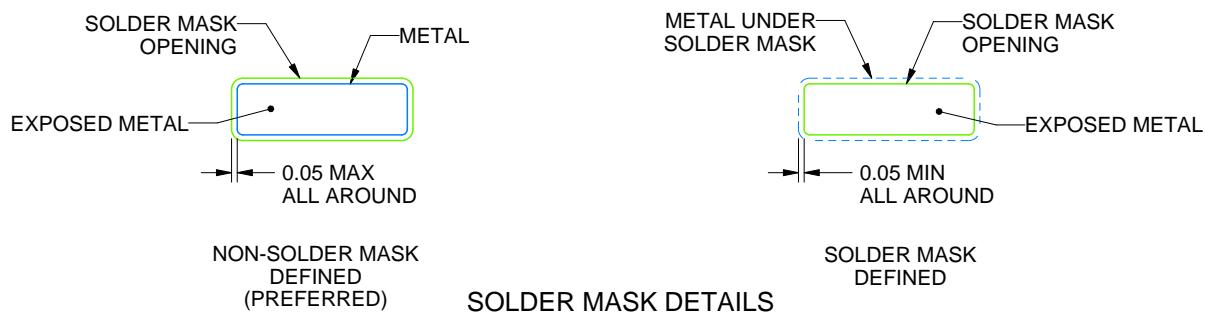
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

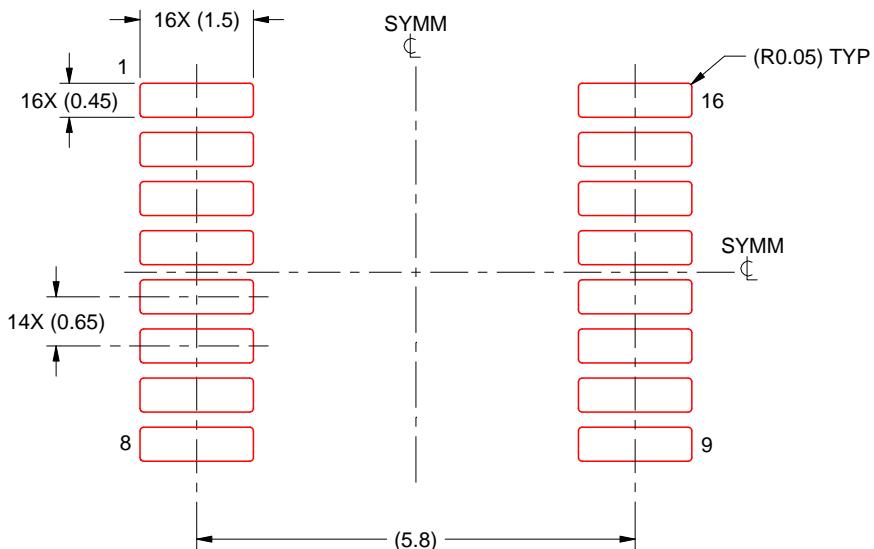
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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