

- **High-Performance Operation:**
Propagation Delay
C Suffix . . . 15 ns Max
M Suffix . . . 20 ns Max
- **Functionally Equivalent, but Faster Than**
PAL16L8A, PAL16R4A, PAL16R6A, and
PAL16R8A
- **Power-Up Clear on Registered Devices (All**
Register Outputs Are Set High, but Voltage
Levels at the Output Pins Go Low)
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to
Plastic and Ceramic DIPs
- **Dependable Texas Instruments Quality and**
Reliability

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

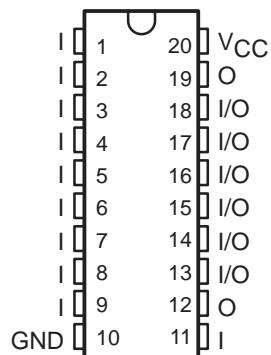
These devices are covered by U.S. Patent 4,410,987.

IMPACT is a trademark of Texas Instruments.

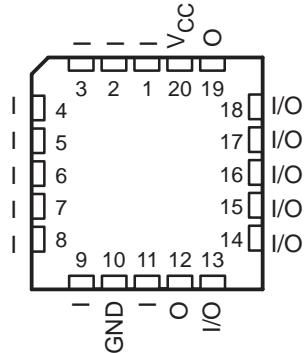
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



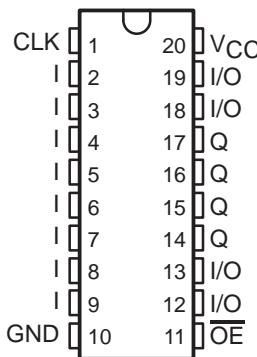
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M SUFFIX . . . FK PACKAGE
(TOP VIEW)



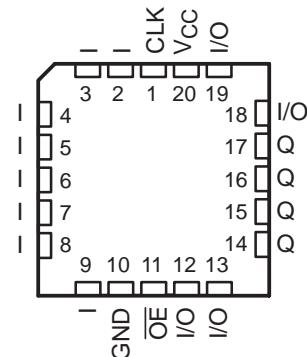
**TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
 HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS**

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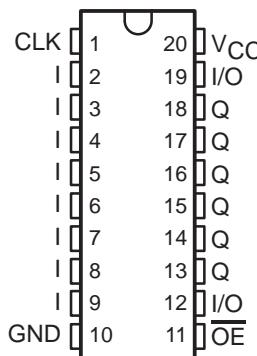
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 (TOP VIEW)



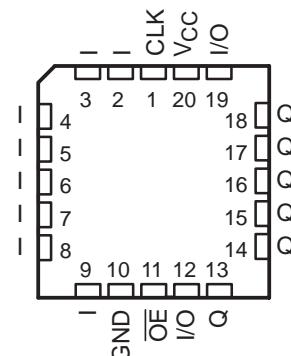
TIBPAL16R4'
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 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



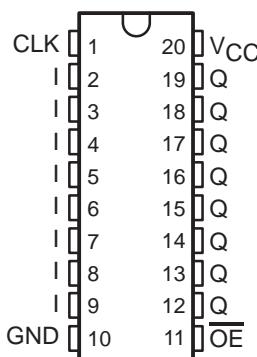
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 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



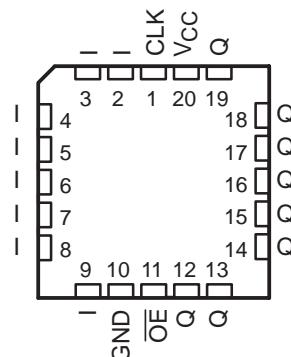
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 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



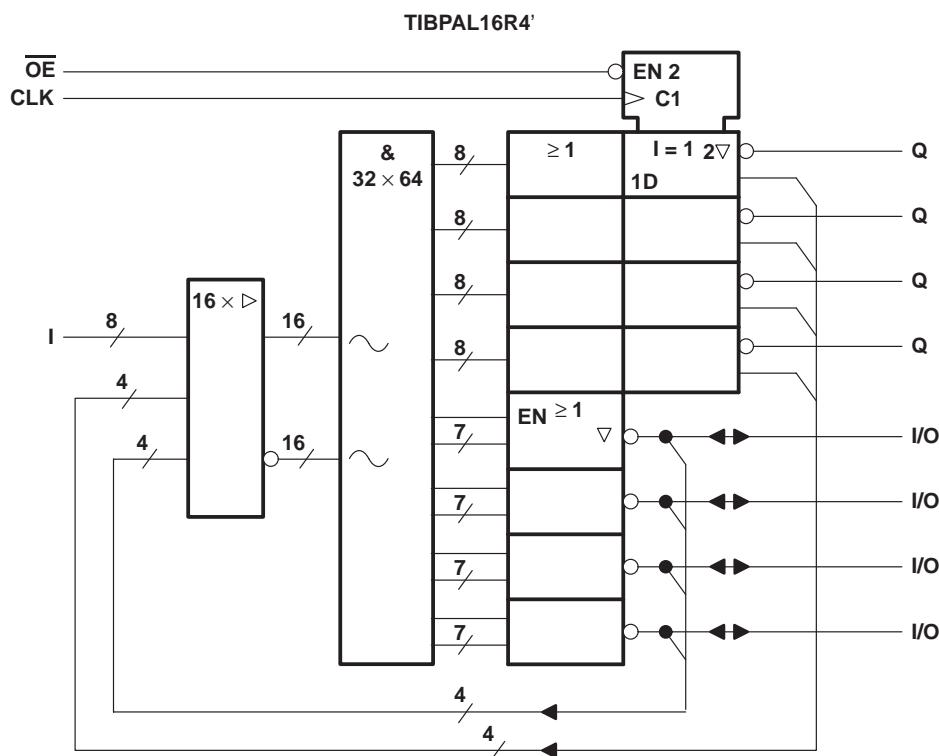
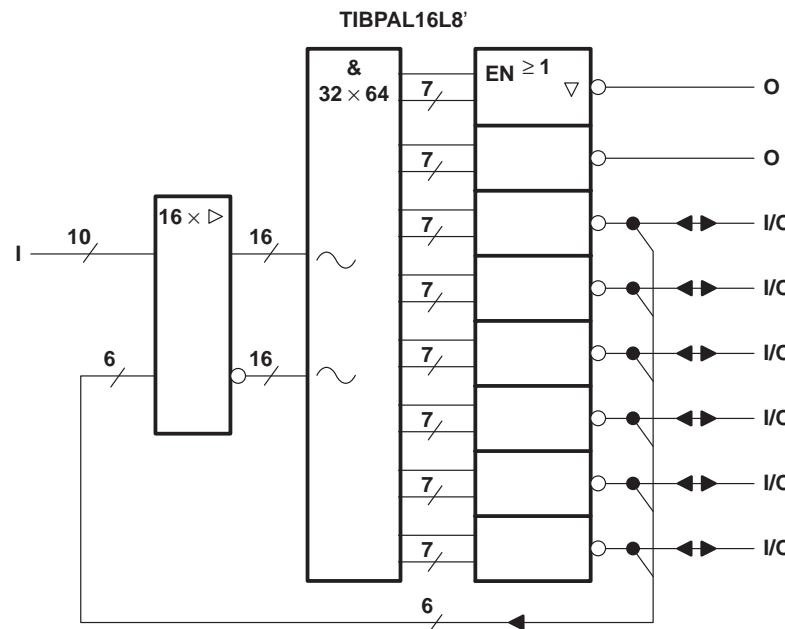
TIBPAL16R8'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



TIBPAL16R8'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



functional block diagrams (positive logic)



~ denotes fused inputs

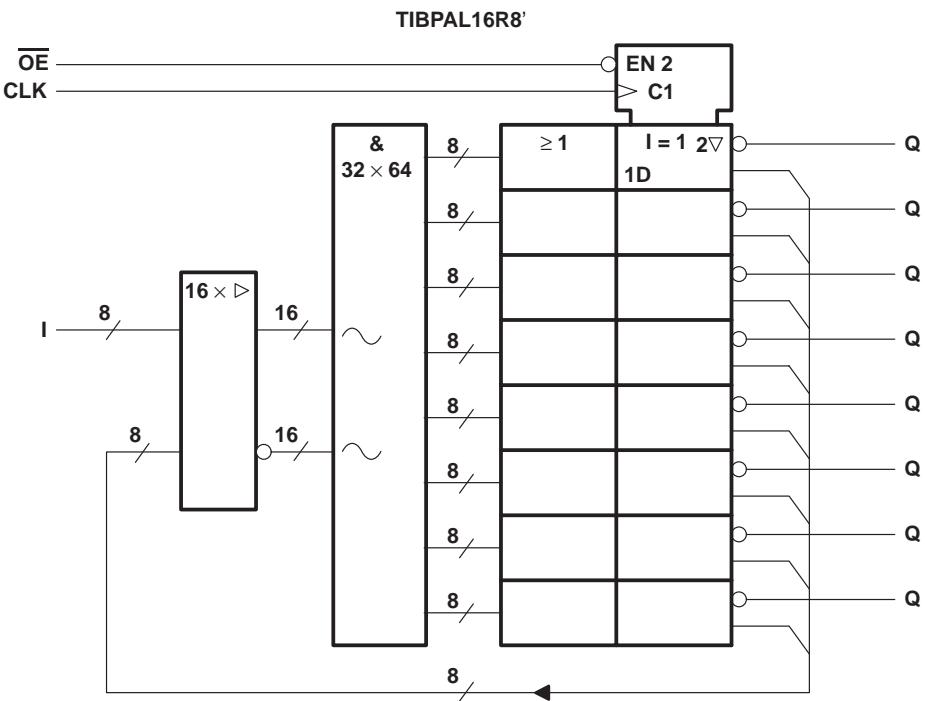
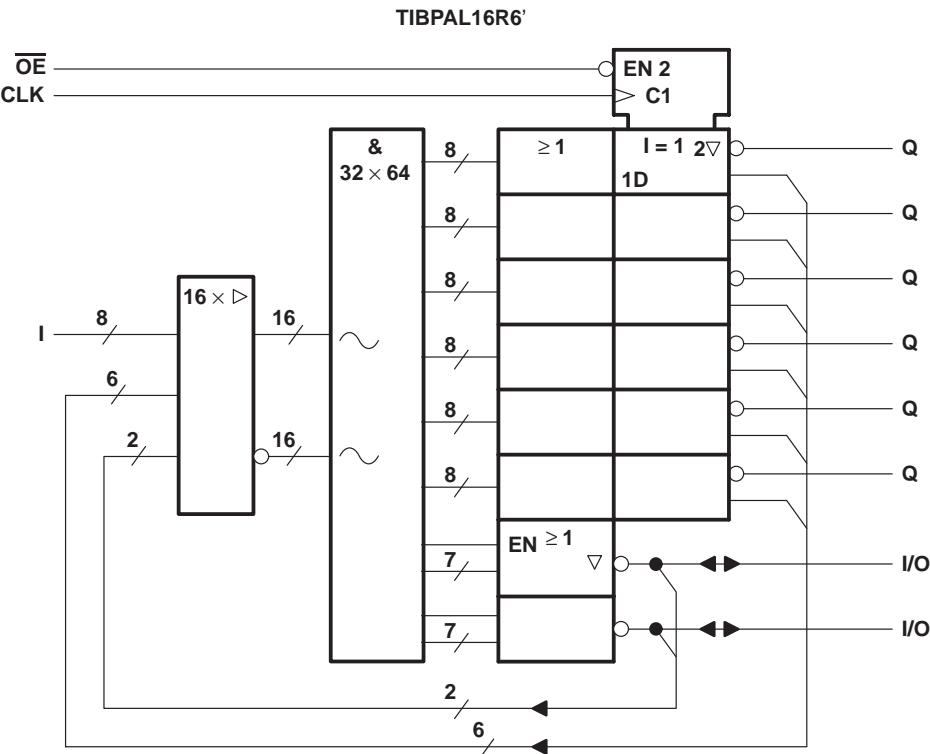
TIBPAL 16R6-15C, TIBPAL 16R8-15C

TIBPAL 16R6-20M, TIBPAL 16R8-20M

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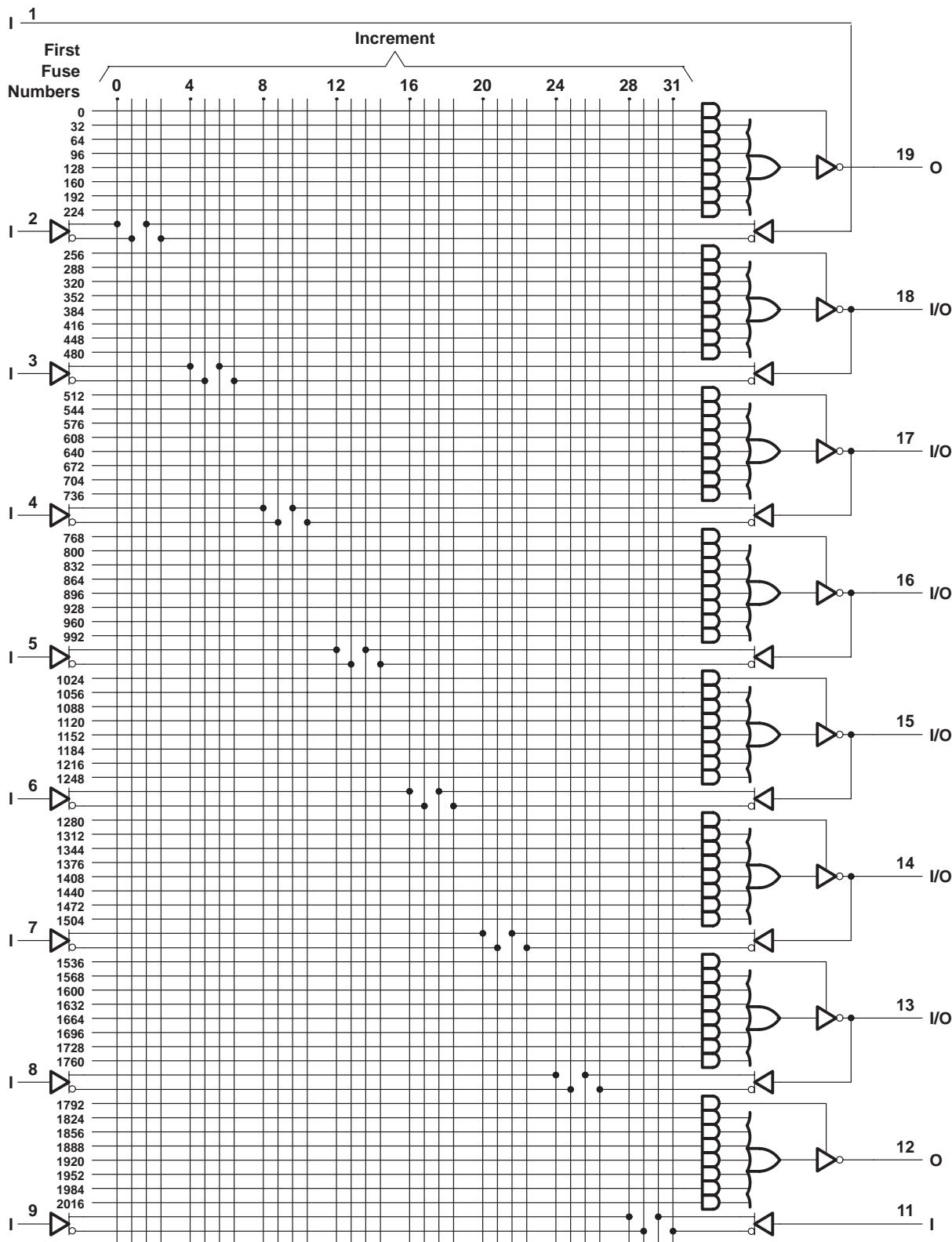
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functional block diagrams (positive logic)



~ denotes fused inputs

logic diagram (positive logic)



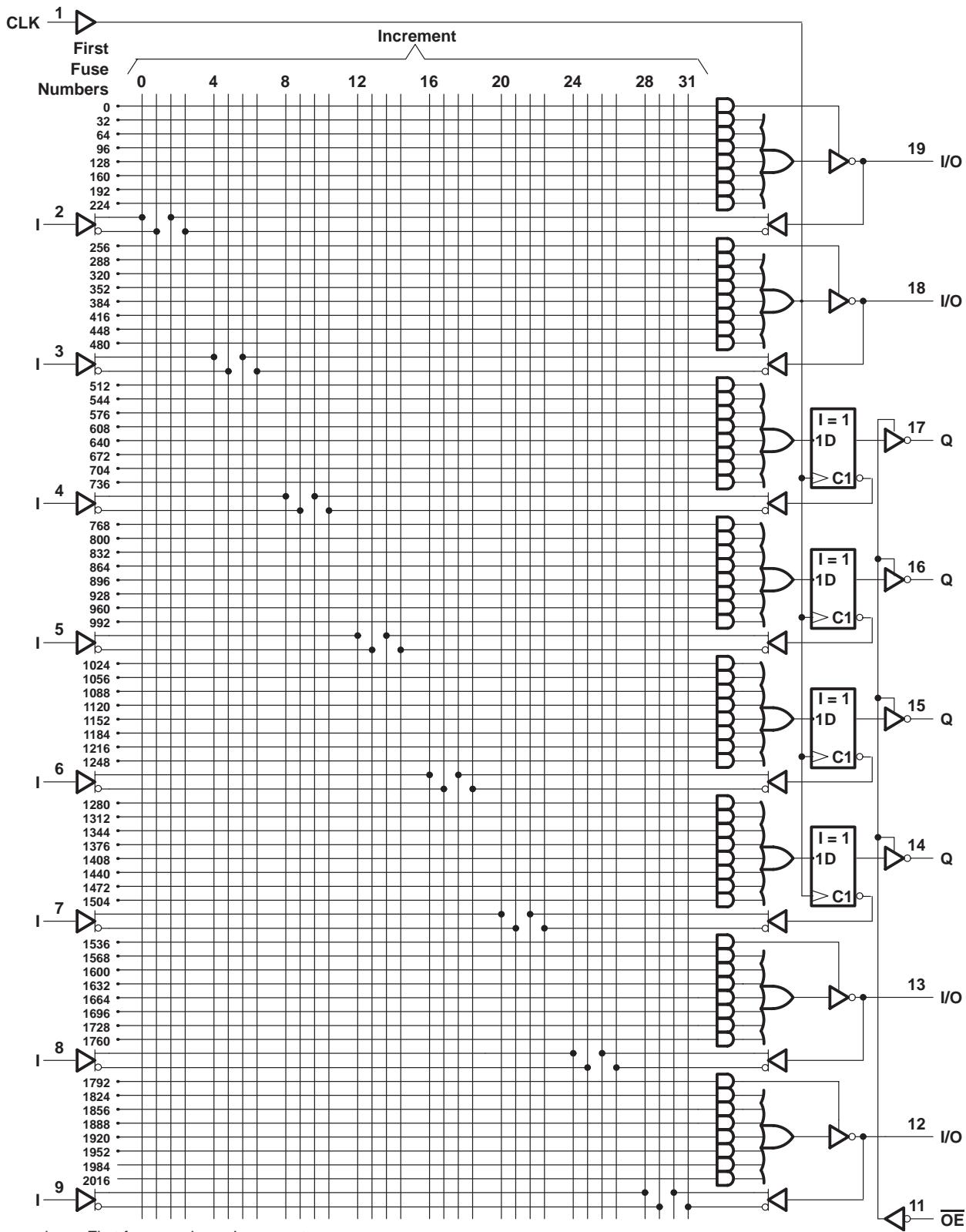
TIBPAL 16R4-15C

TIBPAL 16R4-20M

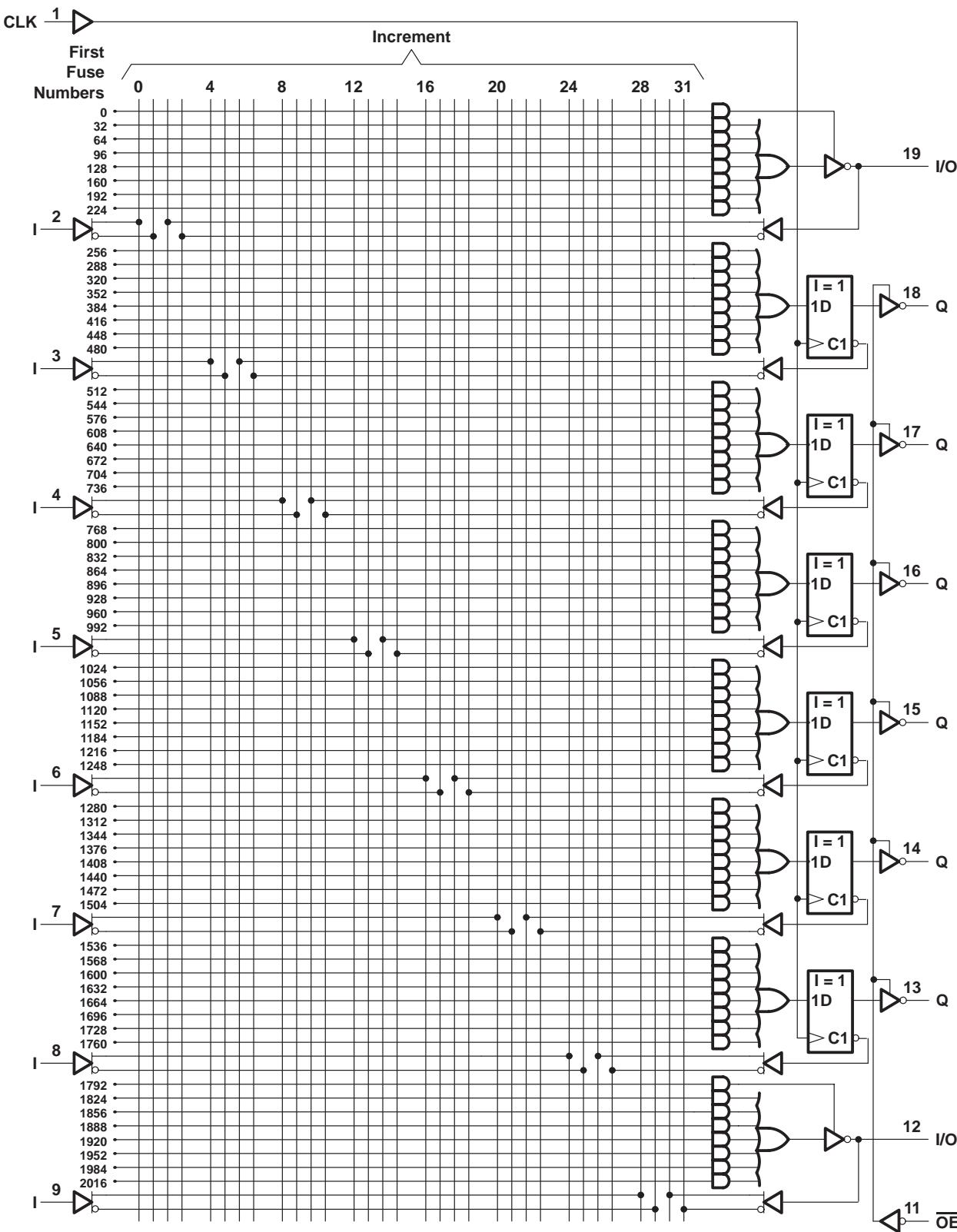
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logic diagram (positive logic)



logic diagram (positive logic)



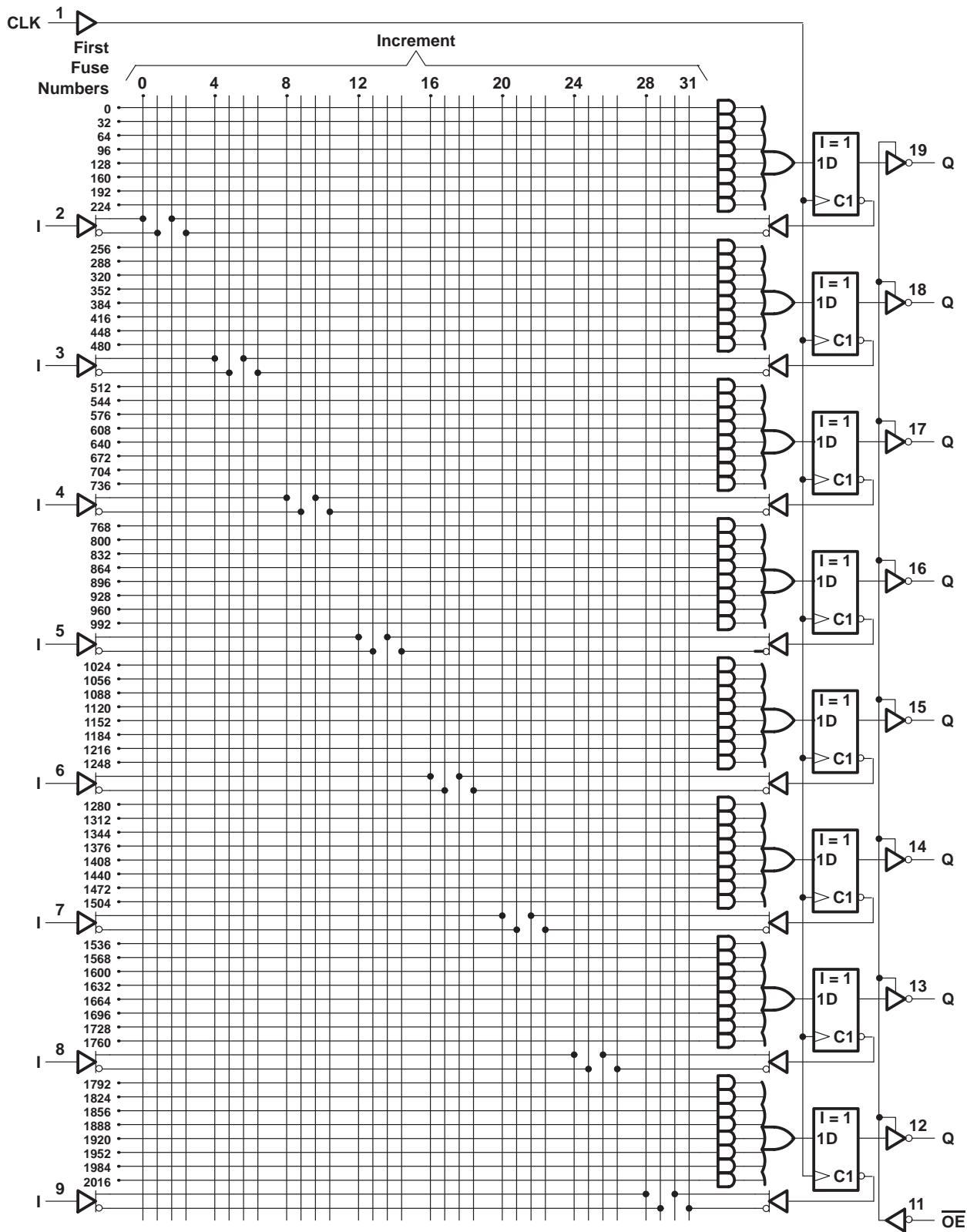
TIBPAL 16R8-15C

TIBPAL 16R8-20M

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logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range, T_{stg}	-65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	8		ns
		Low	9		
t_{SU}	Setup time, input or feedback before clock↑		15		ns
t_h	Hold time, input or feedback after clock↑		0		ns
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH}		$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -3.2 \text{ mA}$	2.4	3.3		V
V_{OL}		$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 24 \text{ mA}$	0.35	0.5		V
I_{OZH}	Outputs	$V_{CC} = 5.25 \text{ V}$, $V_O = 2.7 \text{ V}$		20		μA
	I/O ports			100		
I_{OZL}	Outputs	$V_{CC} = 5.25 \text{ V}$, $V_O = 0.4 \text{ V}$		-20		μA
	I/O ports			-250		
I_I		$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$		0.1		mA
I_{IH}		$V_{CC} = 5.25 \text{ V}$, $V_I = 2.7 \text{ V}$		20		μA
I_{IL}		$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.2		mA
I_O^{\ddagger}		$V_{CC} = 5.25 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-125		mA
I_{CC}		$V_{CC} = 5.25 \text{ V}$, $V_I = 0$, Outputs open	140	180		mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.‡ The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS} .
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}			$R1 = 500 \Omega$, $R2 = 500 \Omega$, See Figure 3	50			MHz
t_{pd}	I, I/O	O, I/O		10	15		ns
t_{pd}	CLK↑	Q		8	12		ns
t_{en}	OE↓	Q		8	12		ns
t_{dis}	OE↑	Q		7	10		ns
t_{en}	I, I/O	O, I/O		10	15		ns
t_{dis}	I, I/O	O, I/O		10	15		ns

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Clock frequency	0		41.6	MHz
t_w	Pulse duration, clock (see Note 2)	High	10		ns
		Low	11		
t_{SU}	Setup time, input or feedback before clock↑		20		ns
t_h	Hold time, input or feedback after clock↑		0		ns
T_A	Operating free-air temperature	-55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.5	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -2 mA		2.4	3.2	V
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25	0.4	V
I _{OZH}	Outputs	V _{CC} = 5.5 V, V _O = 2.7 V			20	µA
	I/O ports				100	
I _{OZL}	Outputs	V _{CC} = 5.5 V, V _O = 0.4 V			-20	µA
	I/O ports				-250	
I _I	Pin 1, 11	V _{CC} = 5.5 V, V _I = 5.5 V			0.2	mA
	All others				0.1	
I _{IH}	Pin 1, 11	V _{CC} = 5.5 V, V _I = 2.7 V			50	µA
	I/O ports				100	
	All others				20	
I _{IL}	I/O ports	V _{CC} = 5.5 V, V _I = 0.4 V			-0.25	mA
	All others				-0.2	
I _{OS} ‡		V _{CC} = 5.5 V, V _O = 0.5 V		-30	-250	mA
I _{CC}		V _{CC} = 5.5 V, V _I = 0, Outputs open		140	190	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 4	41.6			MHz
t _{pd}	I, I/O	O, I/O			10	20	ns
t _{pd}	CLK↑	Q			8	15	ns
t _{en}	OE↓	Q			8	15	ns
t _{dis}	OE↑	Q			7	15	ns
t _{en}	I, I/O	O, I/O			10	20	ns
t _{dis}	I, I/O	O, I/O			10	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming information

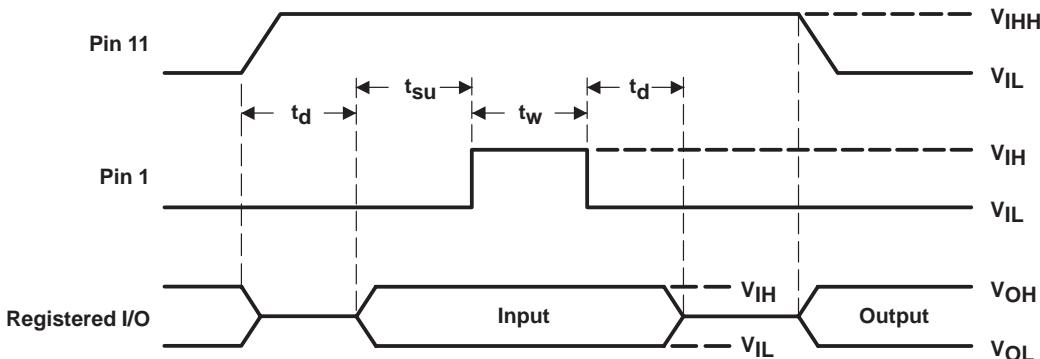
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644-5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL} , raise Pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

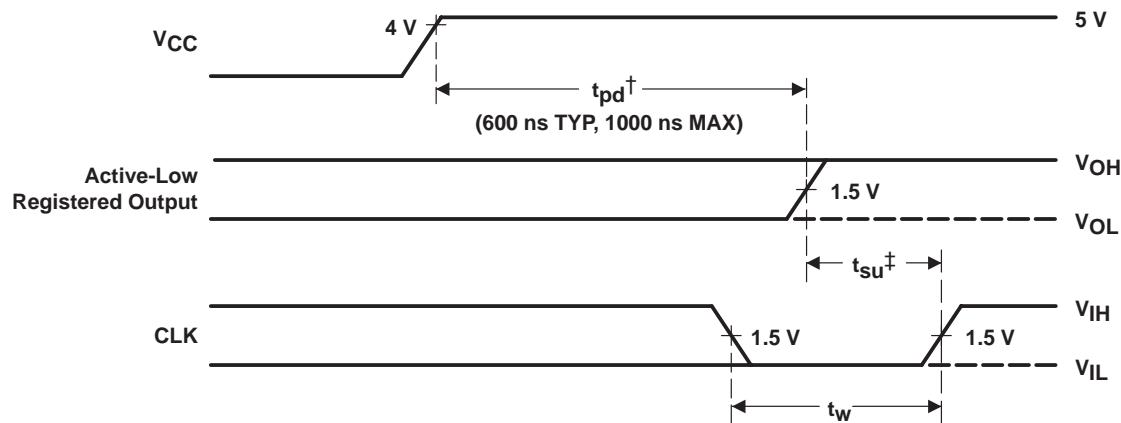


NOTE 3: $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 V

Figure 1. Preload Waveforms

power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

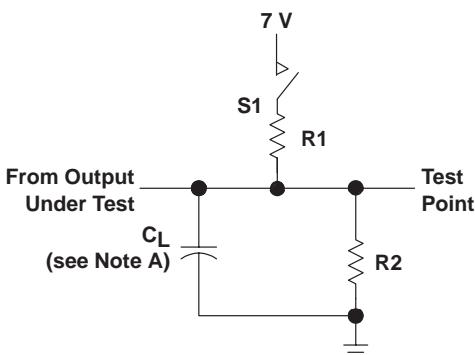


† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

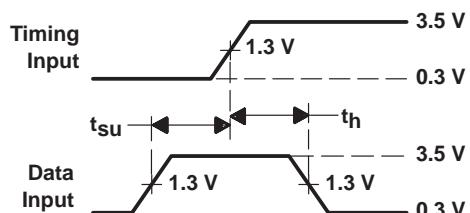
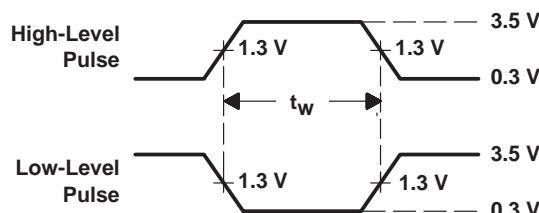
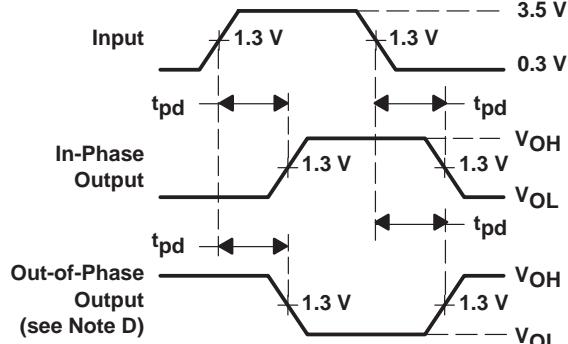
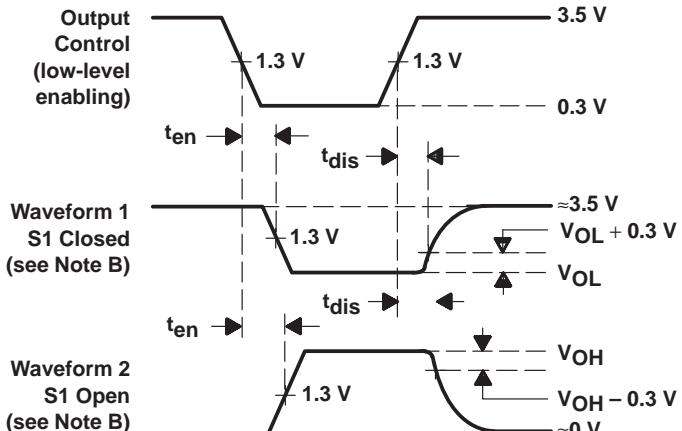
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PULSE DURATIONSVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

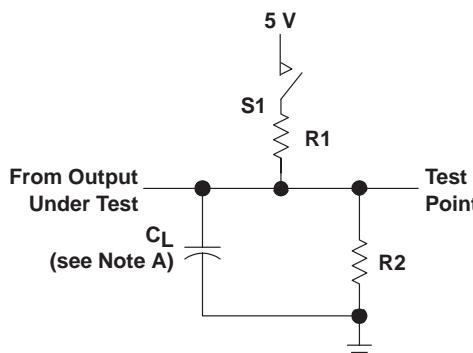
NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed.
 When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

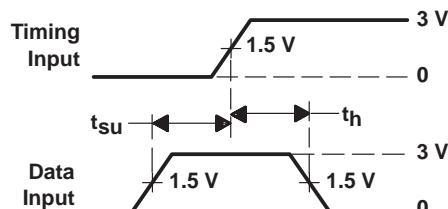
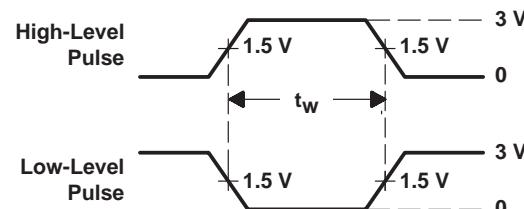
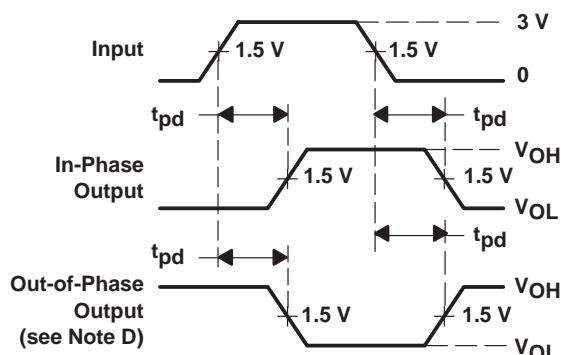
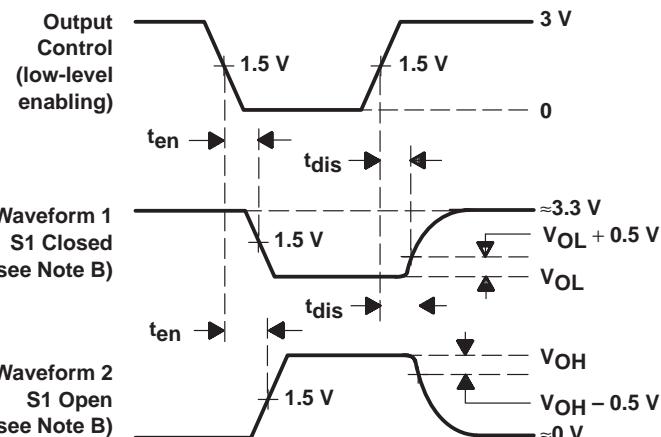
TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PULSE DURATIONSVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:

- C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses have the following characteristics: PRR \leq 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
- When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-85155012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155012A TIBPAL16 L8-20MFKB	Samples
5962-8515501RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515501RA TIBPAL16L8-20M JB	Samples
5962-8515501SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515501SA TIBPAL16L8-20M WB	Samples
5962-85155022A	NRND	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155022A TIBPAL16 R8-20MFKB	
5962-8515502RA	NRND	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515502RA TIBPAL16R8-20M JB	
5962-85155032A	NRND	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155032A TIBPAL16 R6-20MFKB	
5962-8515503RA	NRND	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515503RA TIBPAL16R6-20M JB	
5962-8515503SA	NRND	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515503SA TIBPAL16R6-20M WB	
5962-85155042A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155042A TIBPAL16 R4-20MFKB	Samples
5962-8515504RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515504RA TIBPAL16R4-20M JB	Samples
5962-8515504SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515504SA TIBPAL16R4-20M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										WB	
JM38510/50601BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 50601BRA	Samples
JM38510/50604BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 50604BRA	Samples
M38510/50601BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 50601BRA	Samples
M38510/50604BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 50604BRA	Samples
TIBPAL16L8-20MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155012A TIBPAL16 L8-20MFKB	Samples
TIBPAL16L8-20MJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TIBPAL16L8-20M J	Samples
TIBPAL16L8-20MJB	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515501RA TIBPAL16L8-20M JB	Samples
TIBPAL16L8-20MWB	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515501SA TIBPAL16L8-20M WB	Samples
TIBPAL16R4-20MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155042A TIBPAL16 R4-20MFKB	Samples
TIBPAL16R4-20MJB	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515504RA TIBPAL16R4-20M JB	Samples
TIBPAL16R4-20MWB	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515504SA TIBPAL16R4-20M WB	Samples
TIBPAL16R6-20MFKB	NRND	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155032A TIBPAL16 R6-20MFKB	
TIBPAL16R6-20MJB	NRND	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515503RA TIBPAL16R6-20M	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										JB	
TIBPAL16R6-20MWB	NRND	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515503SA TIBPAL16R6-20M WB	
TIBPAL16R8-20MFKB	NRND	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 85155022A TIBPAL16 R8-20MFKB	
TIBPAL16R8-20MJB	NRND	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515502RA TIBPAL16R8-20M JB	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

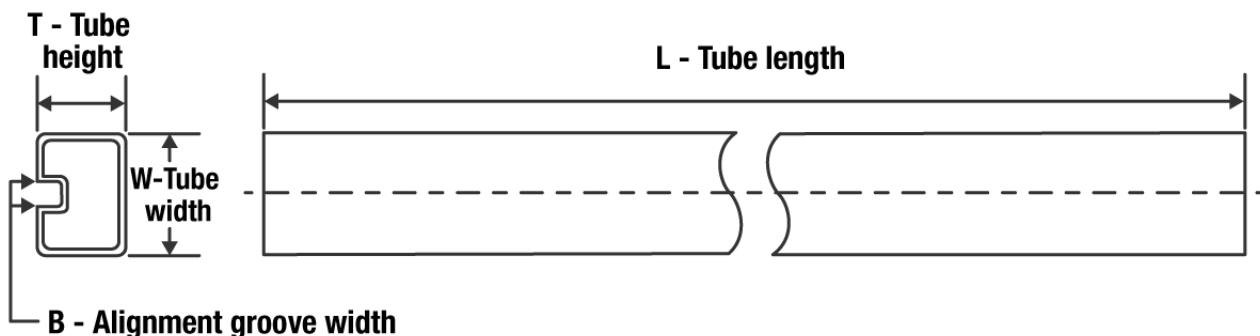
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


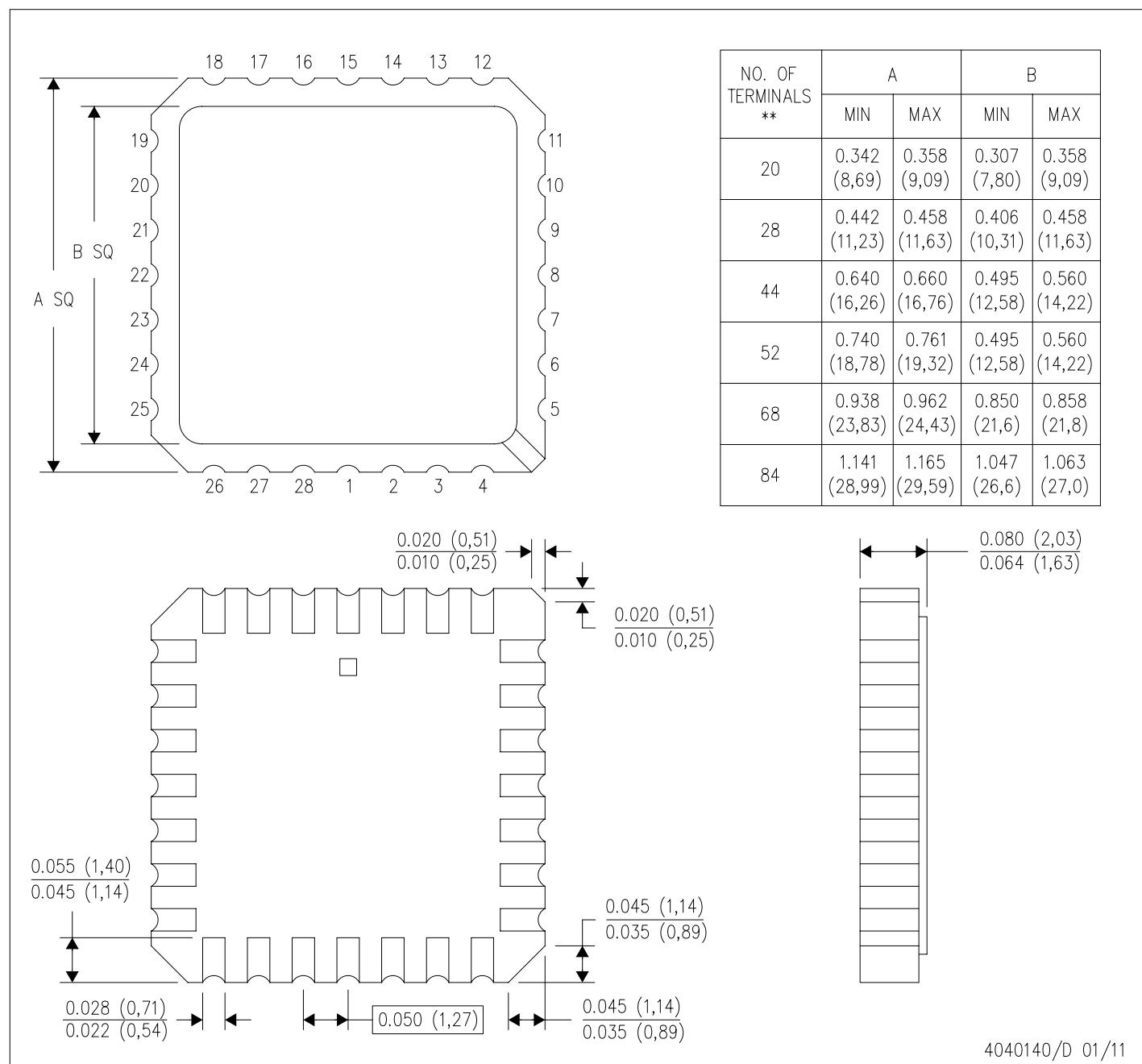
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-85155012A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-85155022A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-85155032A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-85155042A	FK	LCCC	20	1	506.98	12.06	2030	NA
TIBPAL16L8-20MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TIBPAL16R4-20MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TIBPAL16R6-20MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TIBPAL16R8-20MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



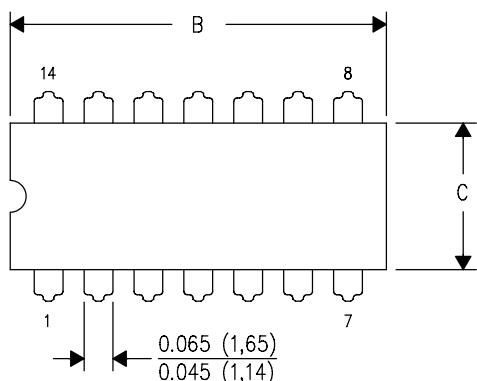
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. Falls within JEDEC MS-004

4040140/D 01/11

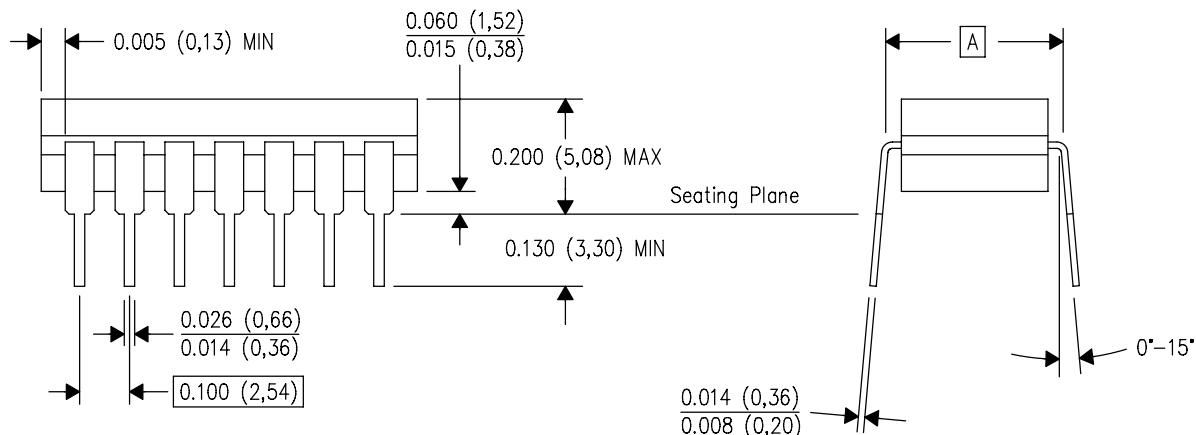
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

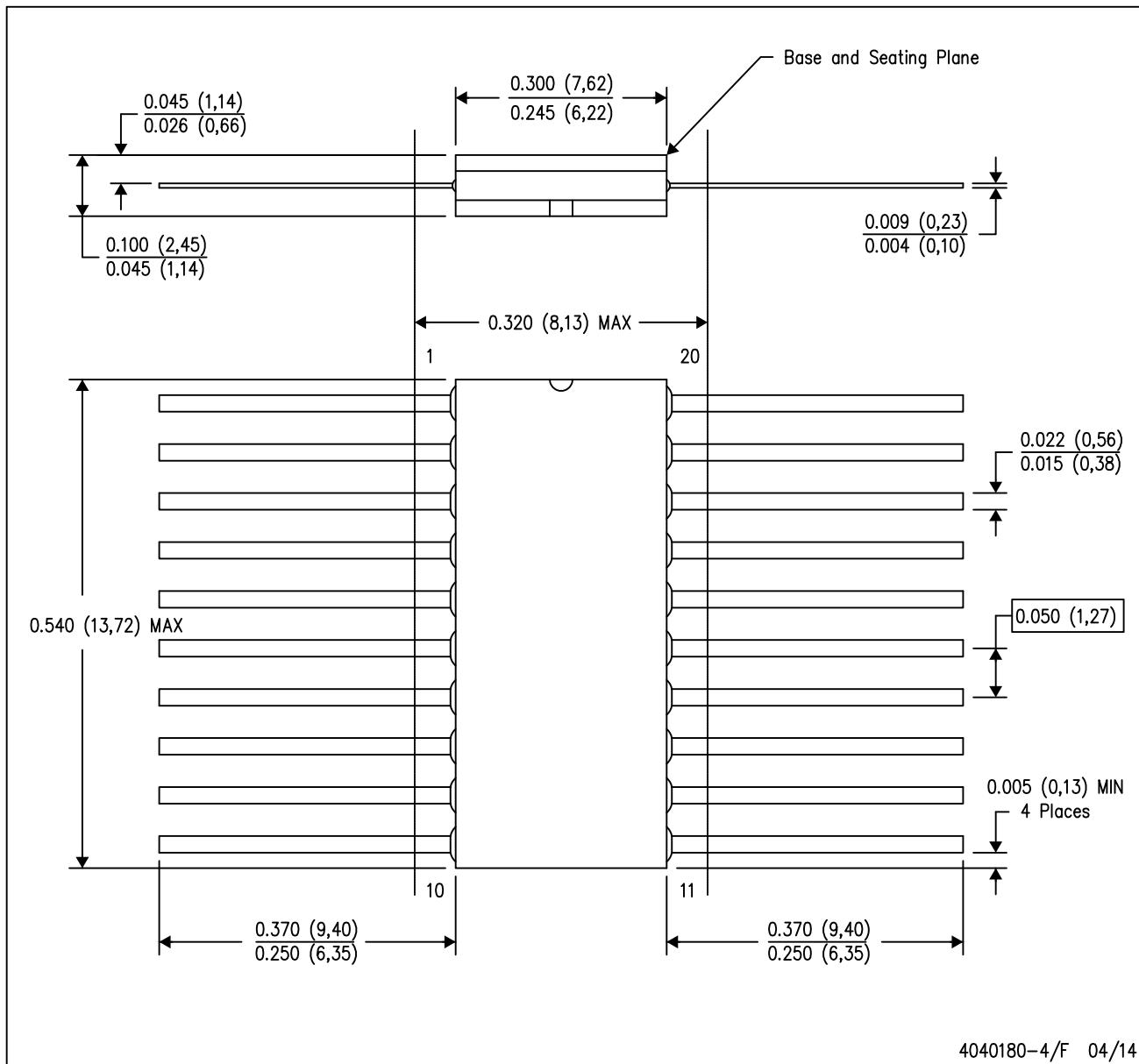


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

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