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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

## TFT Display Module

Part Number

E28RA-I-CW480-N

### Overview:

- 2.8-inch TFT (50.5x69.7 mm)
- 240 x 320
- 16-bit @ 180°
- 8/9/16/18-bit MCU Interface
- 3/4-wire SPI Interface
- All View
- Transmissive, IPS
- Wide Temperature
- No Touch Panel
- 480 nits
- TFT IC: ST7789V
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit and a backlight unit. The resolution of the 2.8" TFT LCD contains 240(RGB)x320 pixels and can display up to 262k colors.

## TFT Features

Low Input Voltage: 3.3V

Display Colors: 65k/262k

Interface: 8/9/16/18-bit MCU

16/18-bit RGB

3/4-wire Serial

| General Information Items | Specification                  | Unit    | Note |
|---------------------------|--------------------------------|---------|------|
|                           | Main Panel                     |         |      |
| TFT Display area (AA)     | 43.20(H) x 57.60(V) (2.8 inch) | mm      | -    |
| Driver Element            | TFT active matrix              | -       | -    |
| Display Colors            | 65k/262k                       | colors  | -    |
| Number of pixels          | 240(RGB)x320                   | dots    | -    |
| TFT Pixel arrangement     | RGB vertical stripe            | -       | -    |
| Pixel Pitch               | 0.18 (H)x0.18(V)               | mm      | -    |
| Viewing angle             | ALL                            | o'clock | -    |
| TFT Controller IC         | ST7789V                        | -       | -    |
| TFT Interface             | MCU, RGB, SPI                  | -       | -    |
| Display mode              | Transmissive/ Normally Black   | -       | -    |
| Operating temperature     | -20~+70                        | °C      | -    |
| Storage temperature       | -30~+80                        | °C      | -    |

## Mechanical Information

| Item        |                | Min | Typ.  | Max | Unit | Note |
|-------------|----------------|-----|-------|-----|------|------|
| Module Size | Horizontal (H) |     | 50.50 |     | mm   | -    |
|             | Vertical (V)   |     | 69.70 |     | mm   | -    |
|             | Depth (D)      |     | 2.60  |     | mm   | -    |
|             | Weight         |     | TBD   |     | g    |      |

**A**

**B**

**C**

**D**

**E**

**F**

**G**

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4

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NO.

PIN NAME

1 GND

2 XR

3 YD

4 XL

5 YU

6 IOVCC

7 IOVCC

8 VCI

9 VCI

10 IM2

11 IM1

12 IM0

13 RESET

14 CS

15 RS(SPI-SCL)

16 WR(SPI-RS)

17 RD

18 VSYNC

19 HSYNC

20 ENABLE

21 DOTCLK

22 SDA

23 DB0(B0)

24 DB01(B1)

25 DB02(B2)

26 DB03(B3)

27 DB04(B4)

28 DB05(B5)

29 DB06(G0)

30 DB07(G1)

31 DB08(G2)

32 DB09(G3)

33 DB10(G4)

34 DB11(G5)

35 DB12(R0)

36 DB13(R1)

37 DB14(R2)

38 DB15(R3)

39 DB16(R4)

40 DB17(R5)

41 SDO

42 GND

43 LEDA

44 LEDK1

45 LEDK2

46 LEDK3

47 LEDK4

48 LEDK5

49 LEDK6

50 GND

50,50±0.2 UP BEZEL

45,60±0.15 UP BEZEL OPEN

44,80±0.3 LCD POL

43,20LCD A.A

2.45

2.85

3.65

Remove Tape

FRONT

BACK

COMPNENT AREA

FPC

CONTACT SIDE

PI

2.8" TFT

240\*RGB\*320

IPS

69,70±0.2 UP BEZEL

61,05±0.15 UP BEZEL OPEN

60,25±0.3 LCD POL

57,60LCD A.A

2.61

16,27

29,12

3,50

50

W=0.3

P0.5\*49=24.50±0.05

25,50±0.1

R0,30

0,50

0,13±0.03

0,30±0.03

3,80±0.2

22,12

5,00

13,00

45,69±0.5

1,00 MAX

NOTE: MCU interface SET for IM PINS.

| DB0 | IM1 | IM0 | Interface type  | DB Pin in use |
|-----|-----|-----|---|---------------|
| 0   | 0   | 0   | DB1 Tyla 8-bit interface  | DB7-DB0       |
| 0   | 1   | 0   | DB1 Tyla 10-bit interface   | DB15-DB0      |
| 0   | 0   | 1   | DB1 Tyla 9-bit interface  | DB8-DB0       |
| 0   | 1   | 1   | DB1 Tyla 10-bit interface   | DB17-DB0      |
| 1   | 0   | 1   | 5-Wire I <sup>2</sup> C Data serial interface (I <sup>2</sup> C used) | SDA SCL CS    |
| 1   | 1   | 1   | 4-Wire I <sup>2</sup> C Data serial interface                         | SDA SCL CS RS |

NOTE:

If not use PINS fix to the GND , IOVCC or NC.

NOTES:

- DISPLAY TYPE: 2.8", TFT-LCD, 65K/262K COLORS
- DISPLAY MODE: IPS NORMALLY BLACK
- VIEWING DIRECTION: ALL
- DRIVER IC: ST7789V (COG)
- VCI: 3.3V
- OPERATING TEMP: -20° C TO 70° C  
STORAGE TEMP: -30° C TO 80° C
- BACK LIGHT: LED WHITE, 6 LED, 120mA, 3.2 ± 0.3V
- RoHS COMPLIANT.

K1(-)

K2(-)

K3(-)

K4(-)

K5(-)

K6(-)

A(+)

NOTE: RGB interface

| RGB Interface            | DB Pin in use                  |
|--------------------------|--------------------------------|
| 16 Bit 565 RGB interface | DB17-DB14, DB11-DB6<br>DB5-DB1 |
| 18 Bit 666 RGB interface | DB17-DB0                       |

NOTE: If used RGB mode must select serial interface!

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PARTS NO.

E28RA-I-CW480-N

TOLERANCE UNLESS OTHERWISE SPECIFIED

X.X±0.3

X.XX±0.2

Scale 1:1

Drawn

Checked

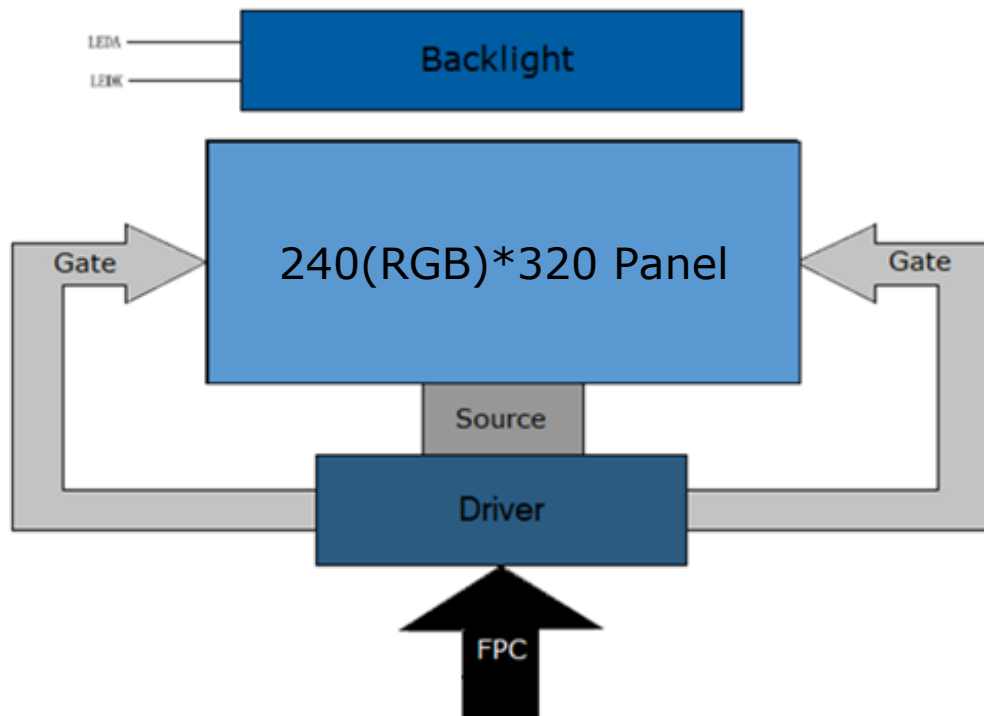
Approve

Unit

mm

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## 2. Block Diagram



### 3. Input Terminal Pin Assignment

Recommended Connector: FH12S-50S-0.5SH(55)

| NO.   | Symbol            | Description   |     |     |     |               | I/O |
|-------|-------------------|---|-----|-----|-----|---------------|-----|
| 1     | GND               | Ground  |     |     |     |               | P   |
| 2     | XR (NC)           | Touch panel right glass terminal  |     |     |     |               | A/D |
| 3     | YD (NC)           | Touch panel bottom film terminal  |     |     |     |               | A/D |
| 4     | XL (NC)           | Touch panel left glass terminal   |     |     |     |               | A/D |
| 5     | YU (NC)           | Touch panel top film terminal   |     |     |     |               | A/D |
| 6     | IOVCC             | Supply voltage (1.65-3.3V)  |     |     |     |               | P   |
| 7     | IOVCC             | Supply voltage (1.65-3.3V)  |     |     |     |               | P   |
| 8     | VCI               | Supply voltage (3.3V)   |     |     |     |               | P   |
| 9     | VCI               | Supply voltage (3.3V)   |     |     |     |               | P   |
| 10-12 | IM3<br>IM2<br>IM0 | Interface selection   | IM3 | IM2 | IM0 | Pins used     | I   |
|       |                   | DBI 8-bit   | 0   | 0   | 0   | DB7-DB0       |     |
|       |                   | DBI 16-bit  | 0   | 1   | 0   | DB15-DB0      |     |
|       |                   | DBI 9-bit   | 0   | 0   | 1   | DB8-DB0       |     |
|       |                   | DBI 18-bit  | 0   | 1   | 1   | DB17-DB0      |     |
|       |                   | 3-wire, 9-bit SPI   | 1   | 0   | 1   | SDA SCL CS    |     |
|       |                   | 4-wire, 8-bit SPI   | 1   | 1   | 1   | SDA SCL CS RS |     |
| 13    | RESET             | Reset signal of the device. Must be applied to properly initialize the device. Signal is active low.  |     |     |     |               | I   |
| 14    | CS                | Chip select pin. When not used this pin can be fixed low.   |     |     |     |               | I   |
| 15    | RS(SPI_SCL)       | Data or command signal for the parallel MCU interface. RS=1: data is selected, RS=0: command is selected. The clock for the serial interface. If not used, pin to VCI or GND. |     |     |     |               | I   |
| 16    | WR(SPI_RS)        | Write signal in the parallel MCU interface. Command or parameter select signal for the 4-wire serial interface. If not used, pin to VCI or GND.                               |     |     |     |               | I   |
| 17    | RD                | Read signal for the MCU parallel interface. If not used, pin to VCI or GND.   |     |     |     |               | O   |
| 18    | VSYNC             | Frame synchronizing signal for the RGB interface. If not used, pin to VCI or GND.   |     |     |     |               | I   |
| 19    | HSYNC             | Line synchronizing signal for the RGB interface. If not used, pin to VCI or GND.  |     |     |     |               | I   |
| 20    | ENABLE            | Data enable signal for the RGB interface. If not used, pin to VCI or GND.   |     |     |     |               | I   |
| 21    | DOTCLK            | Dot clock signal for the RGB interface. If not used, pin to VCI or GND.   |     |     |     |               | I   |
| 22    | SDA               | Serial input signal. The data is applied at the rising edge of the SCL signal. If not used, pin to VCI or GND.  |     |     |     |               | I   |
| 23-40 | DB0-DB17          | 18-bit parallel bi-directional data but for the RGB and MCU interfaces. Fix to GND when not used.   |     |     |     |               | I/O |
| 41    | SDO               | Serial data output for the SPI interface.   |     |     |     |               | I   |
| 42    | GND               | Ground  |     |     |     |               | P   |
| 43    | LEDA              | Anode pin of the backlight  |     |     |     |               | P   |
| 44    | LEDK1             | Cathode pin of the backlight  |     |     |     |               | P   |
| 45    | LEDK2             | Cathode pin of the backlight  |     |     |     |               | P   |
| 46    | LEDK3             | Cathode pin of the backlight  |     |     |     |               | P   |
| 47    | LEDK4             | Cathode pin of the backlight  |     |     |     |               | P   |
| 48    | LEDK5             | Cathode pin of the backlight  |     |     |     |               | P   |
| 49    | LEDK6             | Cathode pin of the backlight  |     |     |     |               | P   |
| 50    | GND               | Cathode pin of the backlight  |     |     |     |               | P   |

I: Input, O: Output, P: Power

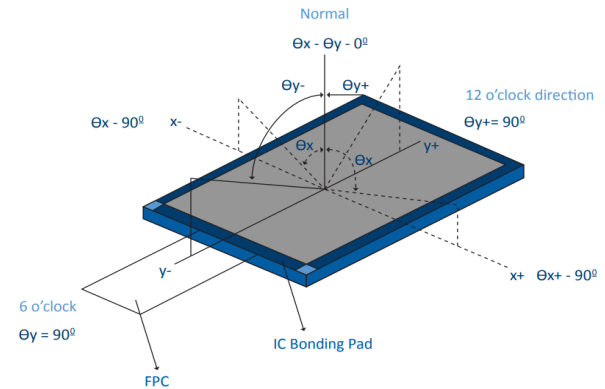
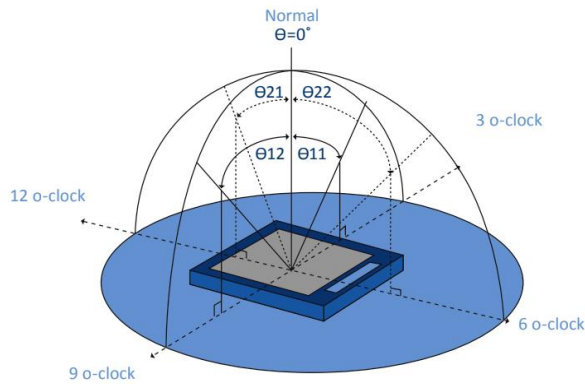
## 4. LCD Optical Characteristics

### 4.1 Optical Specifications

| Item                      |         | Symbol         | Condition                      | Min   | Typ.  | Max   | Unit    | Note   |
|---------------------------|---------|----------------|--------------------------------|-------|-------|-------|---------|--------|
| Color Gamut               |         | S%             | θ=0<br>Normal viewing<br>angle | --    | 60    | --    | %       | (3)    |
| Contrast Ratio            |         | CR             |                                | 600   | 800   | --    | %       | (2)    |
| Response Time             | Rising  | TR+TF          |                                | --    | 30    | 40    | ms      | (4)    |
|                           | Falling |                |                                |       |       |       |         |        |
| Color Filter Chromaticity | White   | W <sub>X</sub> |                                | 0.288 | 0.308 | 0.328 |         | (5)(6) |
|                           |         | W <sub>Y</sub> |                                | 0.310 | 0.330 | 0.350 |         |        |
|                           | Red     | R <sub>X</sub> |                                | 0.621 | 0.641 | 0.661 |         |        |
|                           |         | R <sub>Y</sub> |                                | 0.317 | 0.337 | 0.357 |         |        |
|                           | Green   | G <sub>X</sub> |                                | 0.254 | 0.274 | 0.294 |         |        |
|                           |         | G <sub>Y</sub> |                                | 0.540 | 0.560 | 0.580 |         |        |
|                           | Blue    | B <sub>X</sub> | 0.121                          | 0.141 | 0.161 |       |         |        |
|                           |         | B <sub>Y</sub> | 0.093                          | 0.113 | 0.133 |       |         |        |
| Viewing Angle             | Hor.    | Θ <sub>L</sub> | CR≥10                          | --    | 80    | --    | degrees | (1)(6) |
|                           |         | Θ <sub>R</sub> |                                | --    | 80    | --    |         |        |
|                           | Ver.    | Θ <sub>T</sub> |                                | --    | 80    | --    |         |        |
|                           |         | Θ <sub>B</sub> |                                | --    | 80    | --    |         |        |
| Option View Direction     |         | ALL            |                                |       |       |       |         | (1)    |

### Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

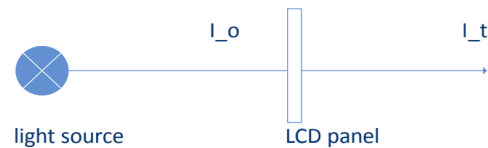


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

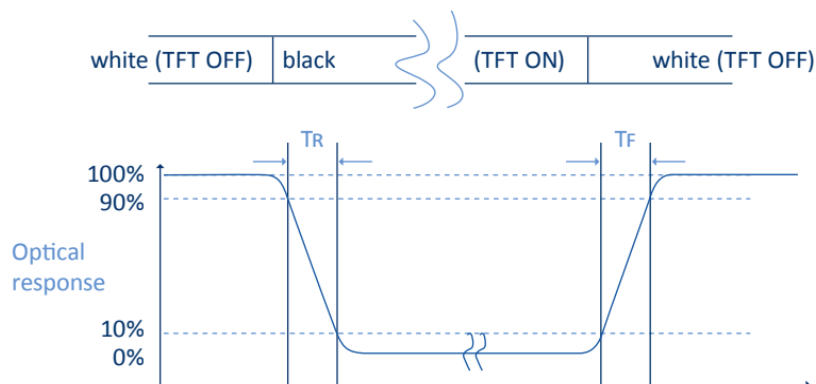
$$Tr = \frac{It}{Io} \times 100\%$$



Io = the brightness of the light source.

It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



##### (5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries:  $R(x,y,Y)$ ,  $G(x,y,Y)$ ,  $B(x,y,Y)$ . FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

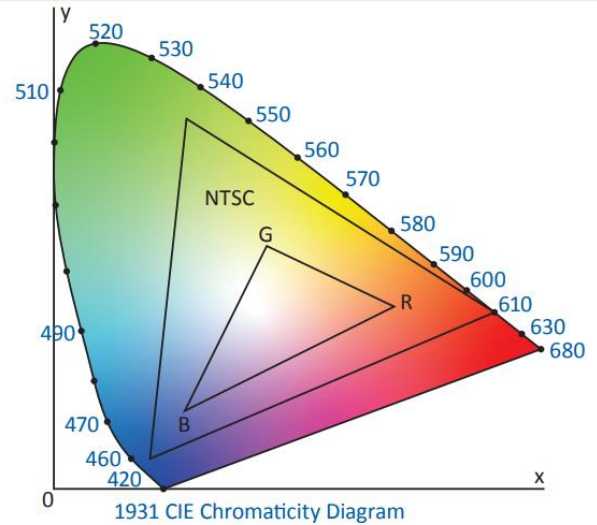
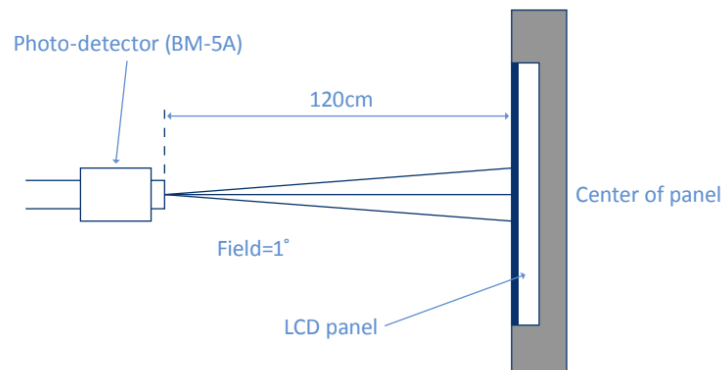
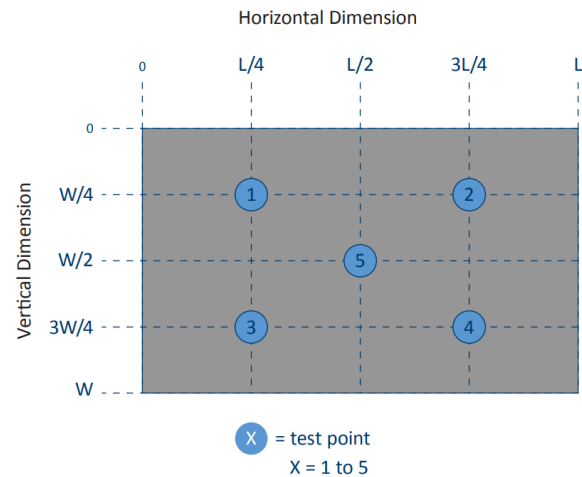
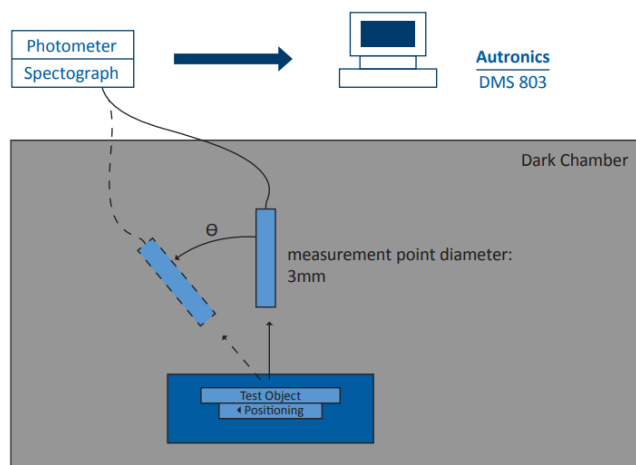


Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

##### (6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

| Characteristics                  | Symbol | Min  | Max | Unit |
|----------------------------------|--------|------|-----|------|
| Digital Supply Voltage           | VDD    | -0.3 | 4.6 | V    |
| Digital Interface Supply Voltage | IOVCC  | -0.3 | 4.6 |      |
| Operating Temperature            | TOP    | -20  | +70 | °C   |
| Storage Temperature              | TST    | -30  | +80 | °C   |

*NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.*

### 5.2 DC Electrical Characteristics

| Characteristics                  | Symbol | Min      | Typ. | Max      | Unit | Note |
|----------------------------------|--------|----------|------|----------|------|------|
| Digital Supply Voltage           | VCI    | 2.5      | 3.3  | 4.2      | V    |      |
| Digital Interface Supply Voltage | IOVCC  | 1.65     | 3.3  | 4.2      | V    |      |
| Normal Mode Current              | IDD    | --       | 8    | --       | mA   |      |
| Level Input Voltage              | VIH    | 0.7IOVCC | --   | IOVCC    | V    |      |
|                                  | VIL    | GND      | --   | 0.3IOVCC | V    |      |
| Level Output Voltage             | VOH    | 0.8IOVCC | --   | IOVCC    | V    |      |
|                                  | VOL    | GND      | --   | 0.2IOVCC | V    |      |

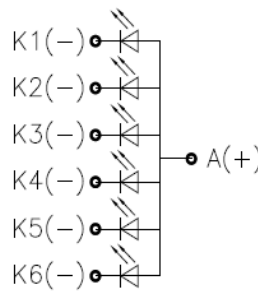
### 5.3 LED Backlight Characteristics

| Item            | Symbol | Min | Typ.  | Max | Unit  | Note         |
|-----------------|--------|-----|-------|-----|-------|--------------|
| Forward Current | IF     | 90  | 120   | --  | mA    |              |
| Forward Voltage | VF     | --  | 3.2   | --  | V     |              |
| LCM Luminance   | LV     | 430 | 480   | --  | cd/m2 | Note 3       |
| LED lifetime    | Hr     | --  | 50000 | --  | hour  | Note1<br>& 2 |
| Uniformity      | AVg    | 80  | --    | --  | %     | Note 3       |

The back-light system is edge-lighting type with 6 white LEDs.

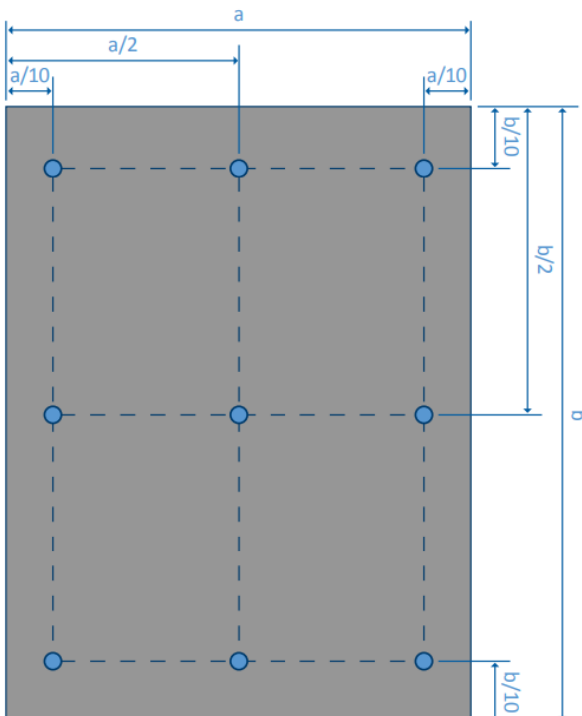
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm 3^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at  $T_a=25^{\circ}\text{C}$  and  $I_L=120\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 120mA. The constant current driving method is suggested.



### Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{(\text{Total Luminance of 9 points})}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

## 6. AC Characteristic

### 6.1 Parallel RGB Interface Characteristics

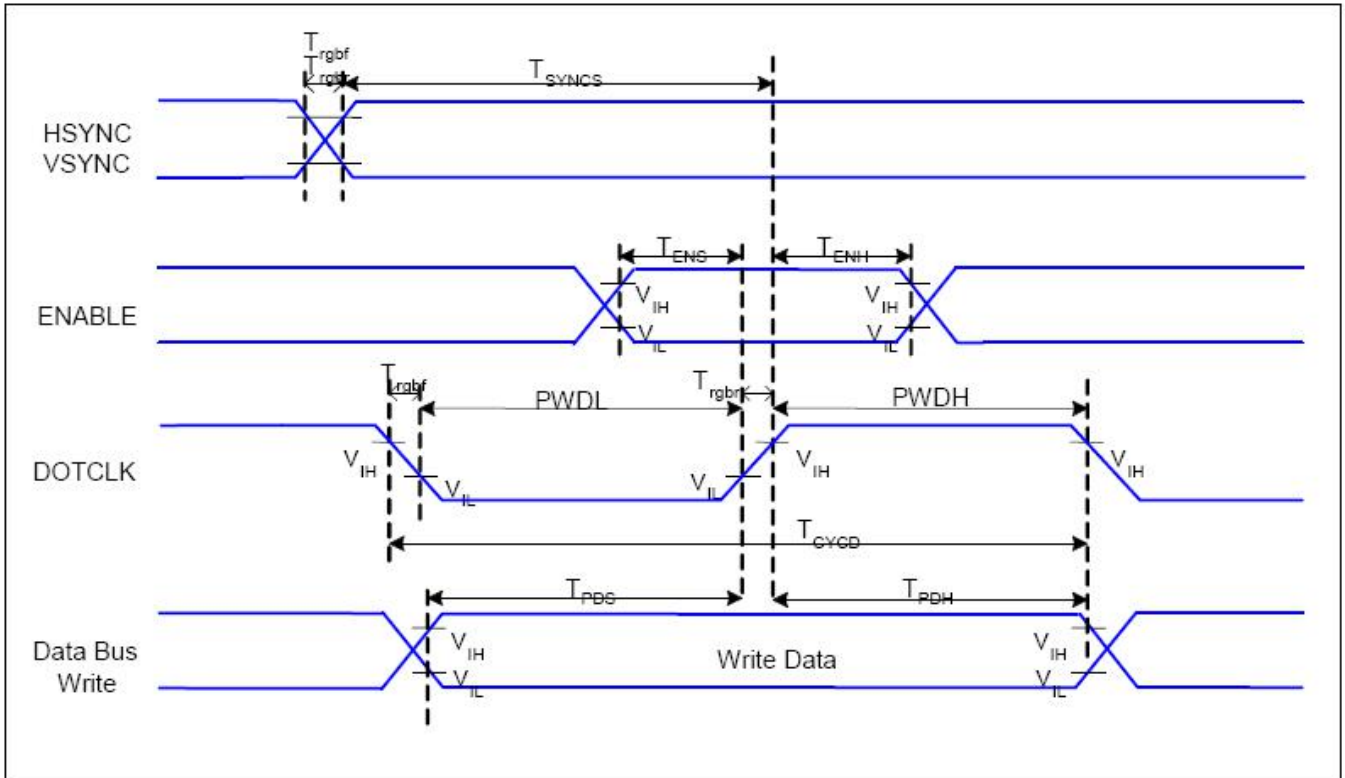


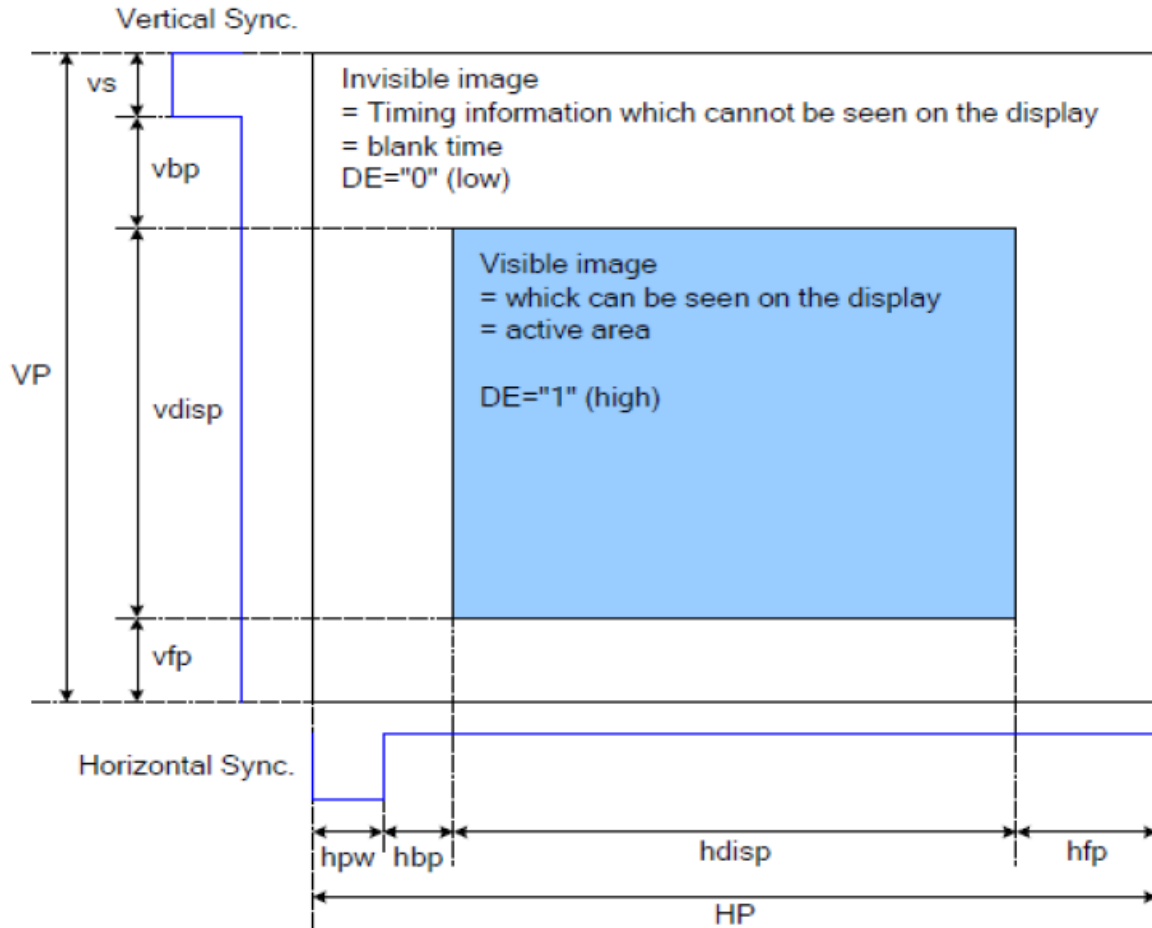
Figure 6.1: Parallel RGB Interface Timing Diagram

| Signal       | Symbol               | Parameter                     | Min | Max | Unit | Description |
|--------------|----------------------|-------------------------------|-----|-----|------|-------------|
| HSYNC, VSYNC | $T_{SYNCS}$          | VSYNC, HSYNC Setup Time       | 30  | -   | ns   |             |
| ENABLE       | $T_{ENS}$            | Enable Setup Time             | 25  | -   | ns   |             |
|              | $T_{ENH}$            | Enable Hold Time              | 25  | -   | ns   |             |
| DOTCLK       | PWDH                 | DOTCLK High-level Pulse Width | 60  | -   | ns   |             |
|              | PWDL                 | DOTCLK Low-level Pulse Width  | 60  | -   | ns   |             |
|              | $T_{CYCD}$           | DOTCLK Cycle Time             | 120 | -   | ns   |             |
|              | $T_{RGHR}, T_{RGHF}$ | DOTCLK Rise/Fall Time         | -   | 20  | ns   |             |
| DB           | $T_{DBS}$            | DB Data Setup Time            | 50  | -   | ns   |             |
|              | $T_{DBH}$            | DB Data Hold Time             | 50  | -   | ns   |             |

Table 6.1: Parallel RGB Interface Timing Characteristics

## 6.2 Timing Tables

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC and DOTCLK signals. The data can be written only within the specified area with low power consumption by using the window address function. The back porch and front porch are used to set the RGB interface timing signals.



| Parameter              | Symbol | Min | Typ | Max | Unit |
|------------------------|--------|-----|-----|-----|------|
| DCLK cycle time        | dclk   | 120 | -   | --  | ns   |
| Horizontal sync width  | hbw    | 2   | 10  | 16  | dclk |
| Horizontal back porch  | hbp    | 2   | 20  | 24  | dclk |
| Horizontal front porch | hfp    | 2   | 10  | 16  | dclk |
| Vertical sync width    | vs     | 1   | 2   | 4   | Line |
| Vertical back porch    | vbp    | 1   | 2   | --  | Line |
| Vertical front porch   | vfp    | 3   | 4   | --  | Line |

Table 6.2: RGB Interface Timing Table

### 6.3 Display Serial Interface Characteristics (3-line SPI system)

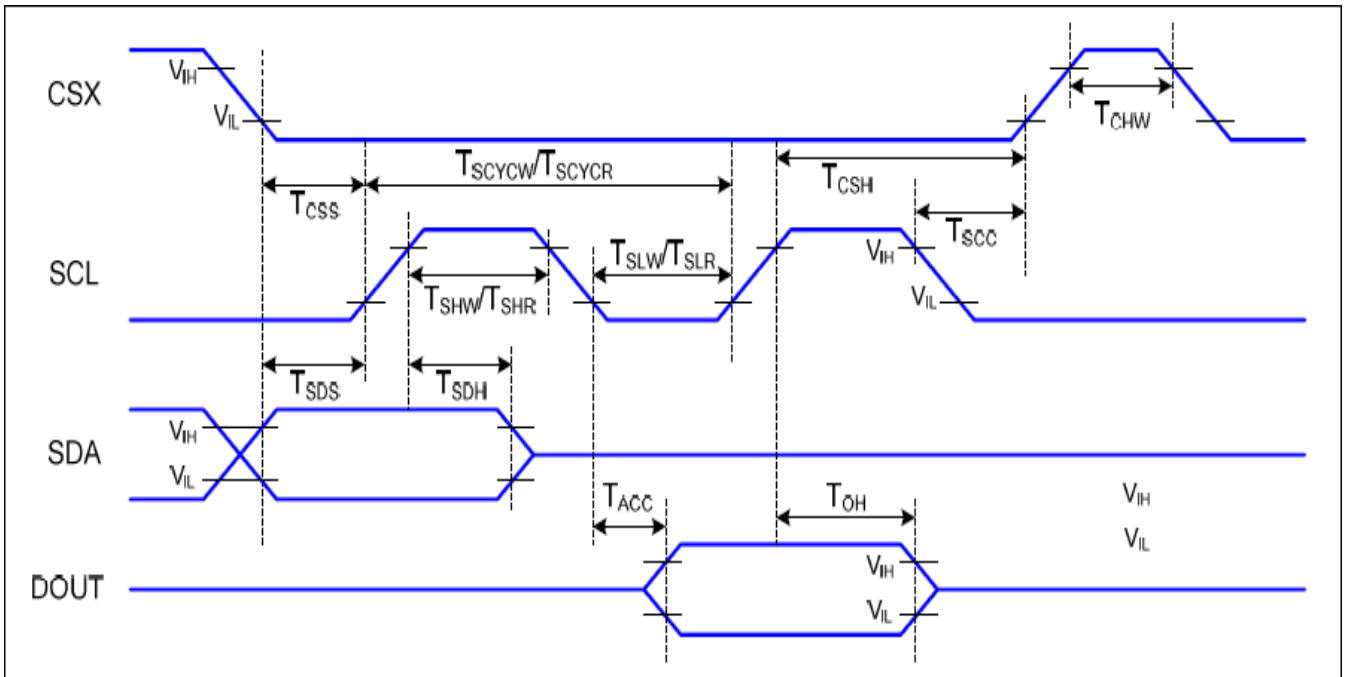


Figure 6.3: Serial Interface 3-SPI Timing Diagram

$V_{DDI} = 1.64 \text{ to } 3.3V$ ,  $V_{DD} = 2.4 \text{ to } 3.3V$ ,  $AGND=DGND=0V$ ,  $T_a = -30 \text{ to } 70^\circ C$

| Signal     | Symbol      | Parameter                      | Min | Max | Unit | Description                             |
|------------|-------------|--------------------------------|-----|-----|------|---|
| CSX        | $T_{CSS}$   | Chip select setup time (write) | 15  |     | ns   |   |
|            | $T_{CSH}$   | Chip select hold time (write)  | 15  |     | ns   |   |
|            | $T_{CSS}$   | Chip select setup time (read)  | 60  |     | ns   |   |
|            | $T_{SCC}$   | Chip select hold time (read)   | 65  |     | ns   |   |
|            | $T_{CHW}$   | Chip select "H" pulse width    | 40  |     | ns   |   |
| SCL        | $T_{SCYCW}$ | Serial clock cycle (write)     | 66  |     | ns   |   |
|            | $T_{SHW}$   | SCL "H" pulse width (write)    | 15  |     | ns   |   |
|            | $T_{SLW}$   | SCL "L" width (write)          | 15  |     | ns   |   |
|            | $T_{SCYCR}$ | Serial clock cycle (read)      | 150 |     | ns   |   |
|            | $T_{SHR}$   | SCL "H" pulse width (read)     | 60  |     | ns   |   |
|            | $T_{SLR}$   | SCL "L" pulse width (read)     | 60  |     | ns   |   |
| SDA (DIN)  | $T_{SDS}$   | Data setup time                | 30  |     | ns   |   |
|            | $T_{SDH}$   | Data hold time                 | 30  |     | ns   |   |
| SDA (DOUT) | $T_{ACC}$   | Access time                    | 10  | 50  | ns   | For max<br>CL=30pF<br>For min<br>CL=8pF |
|            | $T_{OH}$    | Output disable time            | 15  | 50  |      |   |

Table 6.3: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of  $V_{DDI}$  for Input signals

## 6.4 Display Serial Interface Characteristics (4-line SPI serial)

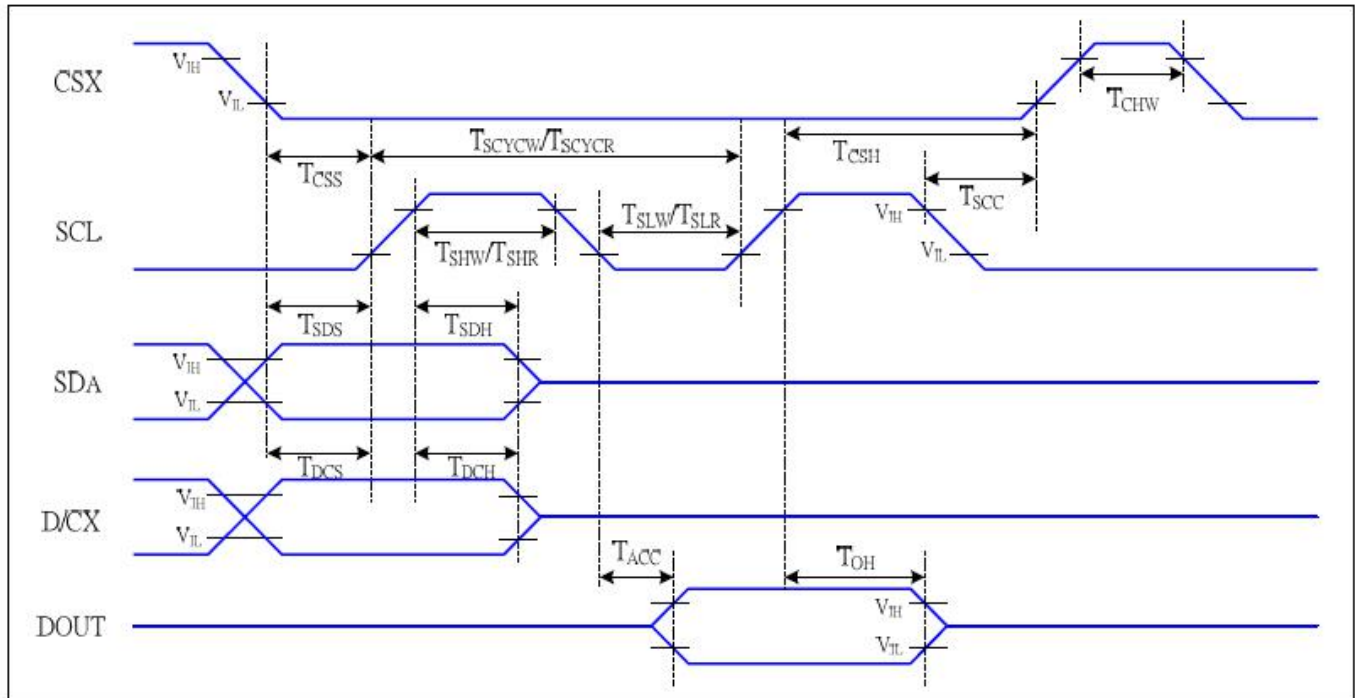


Figure 6.4: Serial Interface 4-SPI Timing Diagram

| Signal    | Symbol      | Parameter                      | Min | Max | Unit | Description                          |
|-----------|-------------|--------------------------------|-----|-----|------|--------------------------------------|
| CSX       | $T_{CSS}$   | Chip select setup time (write) | 15  |     | ns   |                                      |
|           | $T_{CSH}$   | Chip select hold time (write)  | 15  |     | ns   |                                      |
|           | $T_{CSS}$   | Chip select setup time (read)  | 60  |     | ns   |                                      |
|           | $T_{SCC}$   | Chip select hold time (read)   | 65  |     | ns   |                                      |
|           | $T_{CHW}$   | Chip select "H" pulse width    | 40  |     | ns   |                                      |
| SCL       | $T_{SCYCW}$ | Serial clock cycle (write)     | 66  |     | ns   | write command & data ram             |
|           | $T_{SHW}$   | SCL "H" pulse width (write)    | 15  |     | ns   |                                      |
|           | $T_{SLW}$   | SCL "L" width (write)          | 15  |     | ns   |                                      |
|           | $T_{SCYCR}$ | Serial clock cycle (read)      | 150 |     | ns   | read command & data ram              |
|           | $T_{SHR}$   | SCL "H" pulse width (read)     | 60  |     | ns   |                                      |
|           | $T_{SLR}$   | SCL "L" pulse width (read)     | 60  |     | ns   |                                      |
| D/CX      | $T_{DCS}$   | D/CX setup time                | 10  |     | ns   |                                      |
|           | $T_{DCH}$   | D/CX hold time                 | 10  |     | ns   |                                      |
| SDA (DIN) | $T_{SDS}$   | Data setup time                | 10  |     | ns   |                                      |
|           | $T_{SDH}$   | Data hold time                 | 10  |     | ns   |                                      |
| DOUT      | $T_{ACC}$   | Access time                    | 10  | 50  | ns   | For max<br>CL=30pF For<br>min CL=8pF |
|           | $T_{OH}$    | Output disable time            | 15  | 50  | ns   |                                      |

Table 6.5: 4-line Serial Interface Timing Characteristics

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of  $V_{DDI}$  for Input signals.

## 6.5 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

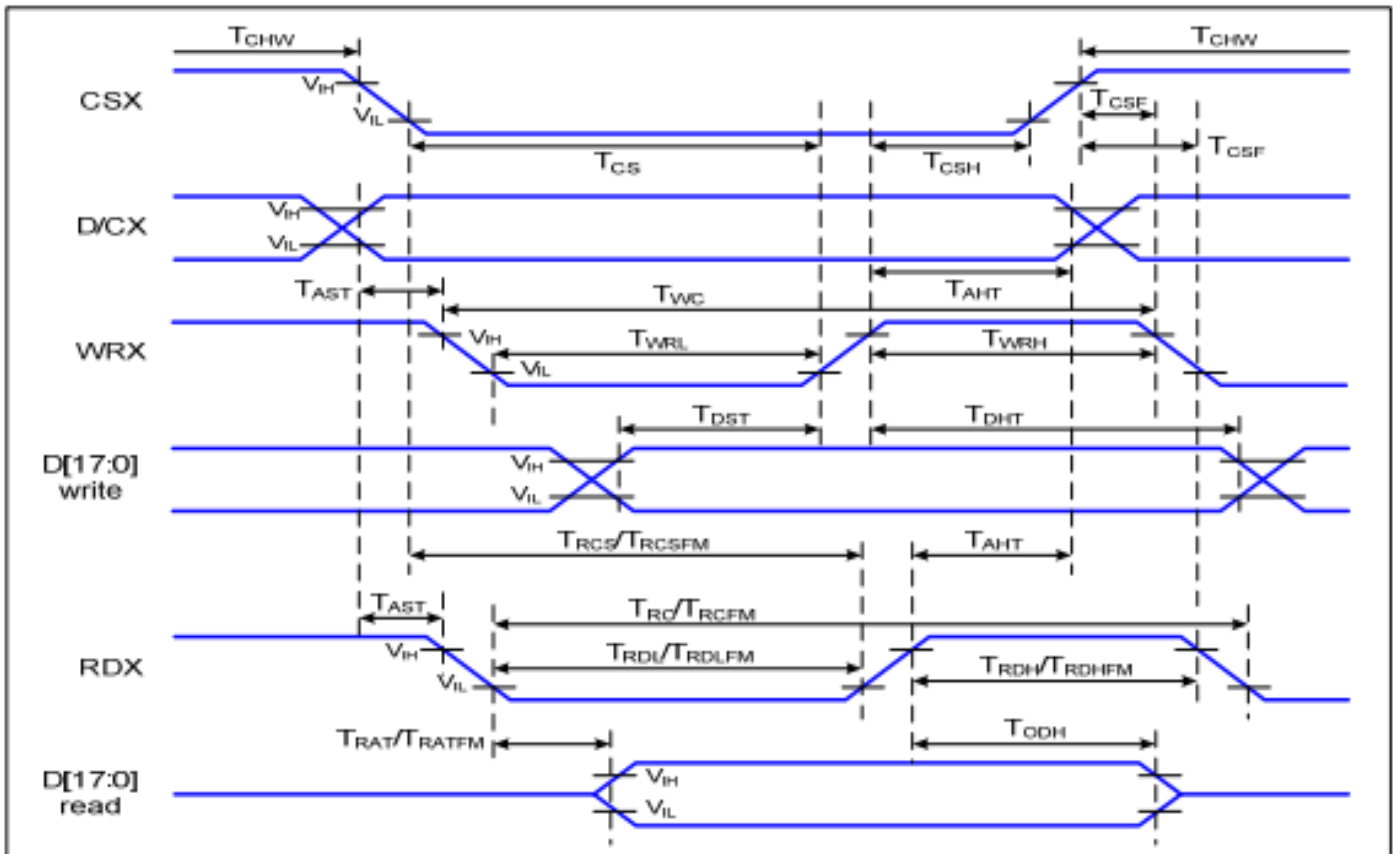


Figure 6.5: Parallel Interface Timing Characteristics (8080-Series MCU Interface)

| Signal                                   | Symbol      | Parameter                          | Min | Max | Unit | Description                           |
|--|-------------|------------------------------------|-----|-----|------|---------------------------------------|
| D/CX                                     | $T_{AST}$   | Address setup time                 | 0   | -   | ns   |                                       |
|  | $T_{AHT}$   | Address hold time (Write/Read)     | 10  | -   | ns   |                                       |
| CSX                                      | $T_{CHW}$   | Chip select “H” pulse width        | 0   | -   | ns   |                                       |
|  | $T_{CS}$    | Chip select setup time (Write)     | 15  | -   | ns   |                                       |
|  | $T_{RCS}$   | Chip select setup time (Read ID)   | 45  | -   | ns   |                                       |
|  | $T_{RCSFM}$ | Chip select setup time (Read FM)   | 355 | -   | ns   |                                       |
|  | $T_{CSF}$   | Chip select wait time (Write/Read) | 10  | -   | ns   |                                       |
|  | $T_{CSH}$   | Chip select hold time              | 10  | -   | ns   |                                       |
| WRX                                      | $T_{WC}$    | Write cycle                        | 66  | -   | ns   |                                       |
|  | $T_{WRH}$   | Control pulse “H” duration         | 15  | -   | ns   |                                       |
|  | $T_{WRL}$   | Control pulse “L” duration         | 15  | -   | ns   |                                       |
| RDX (ID)                                 | $T_{RC}$    | Read cycle (ID)                    | 160 | -   | ns   |                                       |
|  | $T_{RDH}$   | Control pulse “H” duration (ID)    | 90  | -   | ns   |                                       |
|  | $T_{RDHL}$  | Control pulse “L” duration         | 45  | -   | ns   |                                       |
| RDX (FM)                                 | $T_{RCFM}$  | Read cycle (FM)                    | 450 | -   | ns   |                                       |
|  | $T_{RDHFM}$ | Control pulse “H” duration (FM)    | 90  | -   | ns   |                                       |
|  | $T_{RDLFM}$ | Control pulse “L” duration (FM)    | 355 | -   | ns   |                                       |
| D[17:0]<br>D[15:0],<br>D[8:0],<br>D[7:0] | $T_{DST}$   | Write data setup time              | 10  | -   | ns   | For max CL=30pF<br><br>For min CL=8pF |
|  | $T_{DHT}$   | Write data hold time               | 10  | -   | ns   |                                       |
|  | $T_{RAT}$   | Read access time (ID)              | -   | 40  | ns   |                                       |
|  | $T_{RATFM}$ | Read access time (FM)              | -   | 340 | ns   |                                       |
|  | $T_{ROD}$   | Output disable time                | 20  | 80  | ns   |                                       |

Table 6.5: 8080 Series MCU Parallel Timing Characteristics

### 6.3 Reset Timing

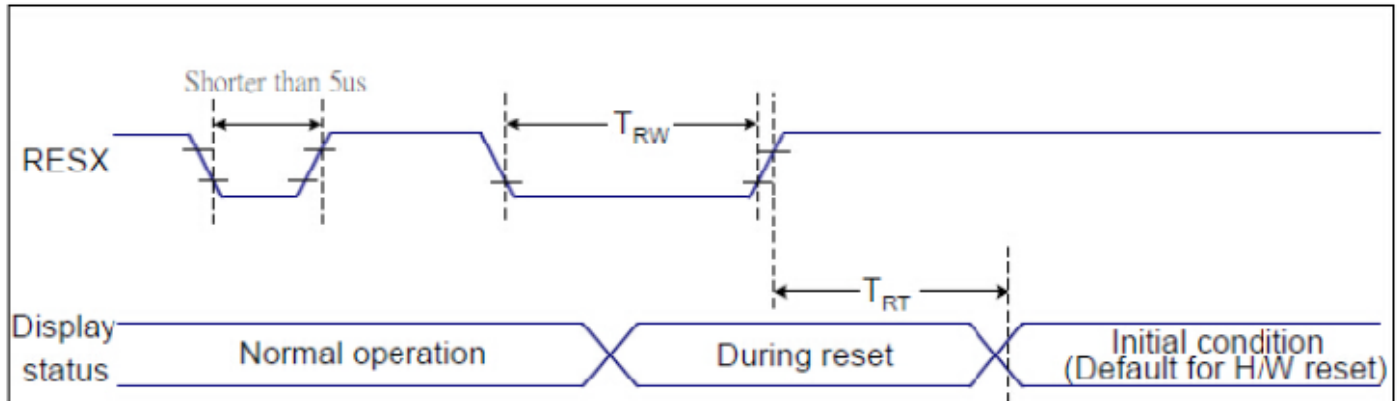


Figure 6.6: Reset Timing Diagram

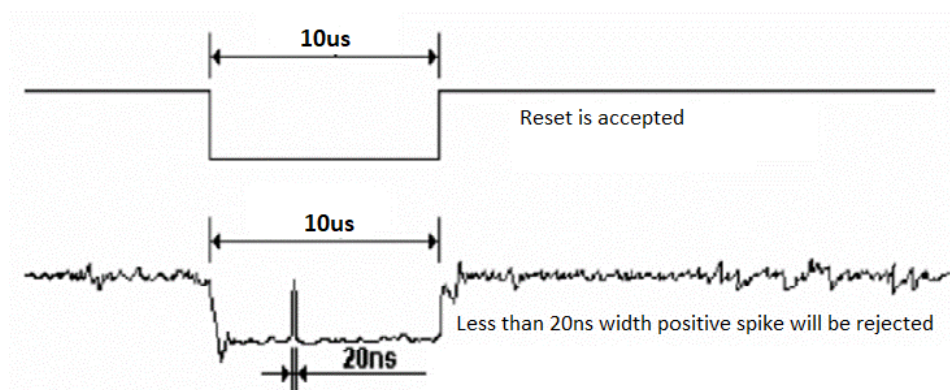
| Related Pins | Symbol | Parameter            | Min | Max                | Unit |
|--------------|--------|----------------------|-----|--------------------|------|
| RESX         | TRW    | Reset pulse duration | 10  | -                  | us   |
|              | TRT    | Reset cancel         | -   | 5 (Note 1,5)       | ms   |
|              |        |                      |     | 120 (Note 1, 6, 7) | ms   |

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

| RESX Pulse           | Action         |
|----------------------|----------------|
| Shorter than 5us     | Reset Rejected |
| Longer than 9us      | Reset          |
| Between 5us and 9 us | Reset starts   |

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.



## **7. Cautions and Handling Precautions**

### **7.1 Handling and Operating the Module**

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

### **7.2 Storage and Transportation**

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.