

SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

SDAS227A – JUNE 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
 - SN74ALS666 . . . True Outputs
 - SN74ALS667 . . . Inverted Outputs
- Preset and Clear Inputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

description

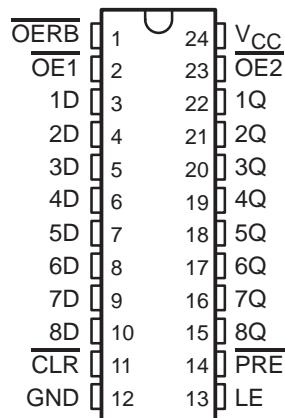
These 8-bit D-type transparent latches are designed specifically for storing the contents of the input data bus, plus reading back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily utilized in bus-structured applications.

While the latch enable (LE) is high, the Q outputs of the SN74ALS666 follow the data (D) inputs. The \bar{Q} outputs of the SN74ALS667 provide the inverse of the data applied to its D inputs. The Q or \bar{Q} output of both devices is in the high-impedance state if either output-enable (\bar{OE}_1 or \bar{OE}_2) input is at a high logic level.

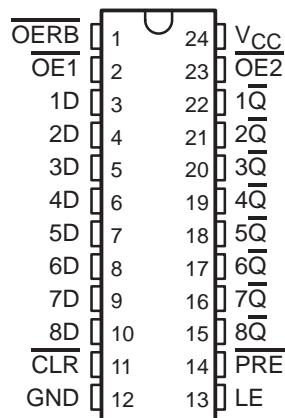
Read back is provided through the read-back control (\bar{OER}_B) input. When \bar{OER}_B is taken low, the data present at the output of the data latches passes back onto the input data bus. When \bar{OER}_B is taken high, the output of the data latches is isolated from the D inputs. \bar{OER}_B does not affect the internal operation of the latches; however, caution should be exercised to avoid a bus conflict.

The SN74ALS666 and SN74ALS667 are characterized for operation from 0°C to 70°C.

SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)



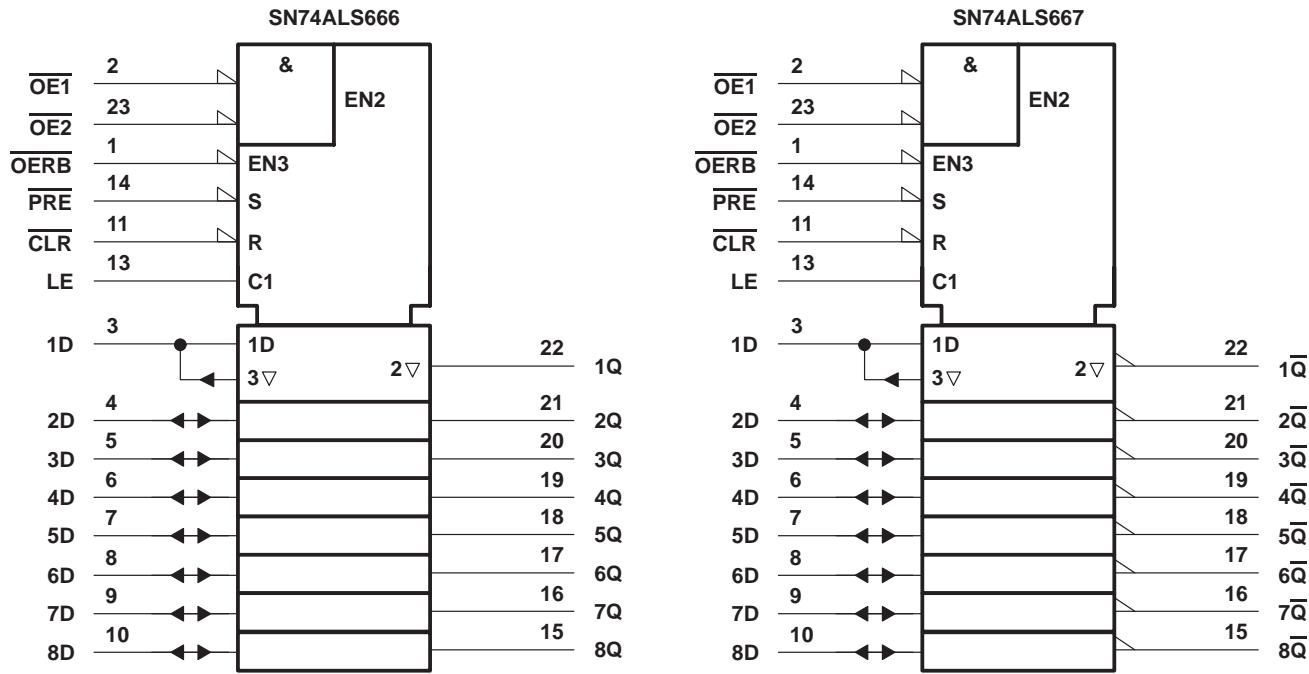
SN74ALS667 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

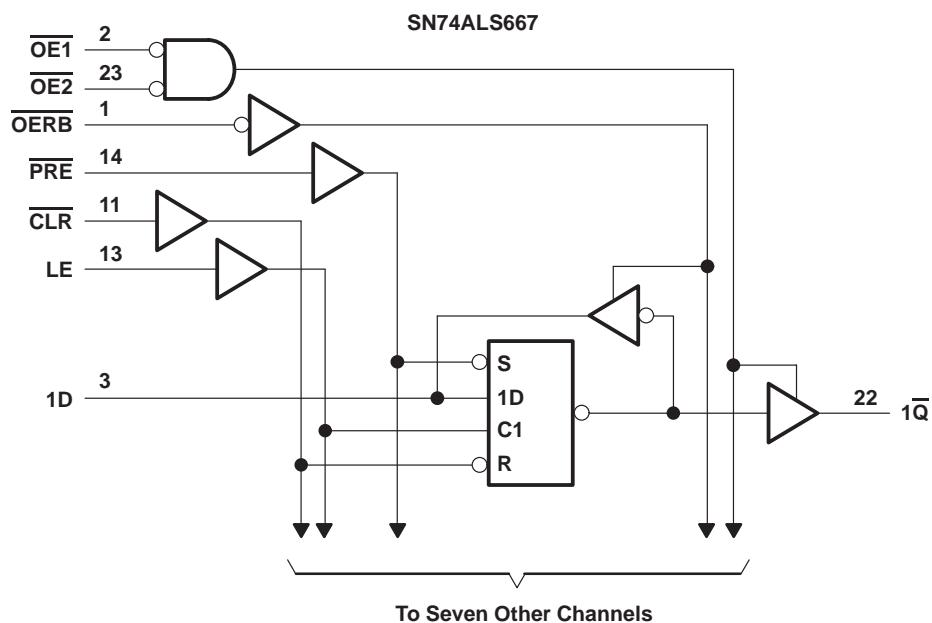
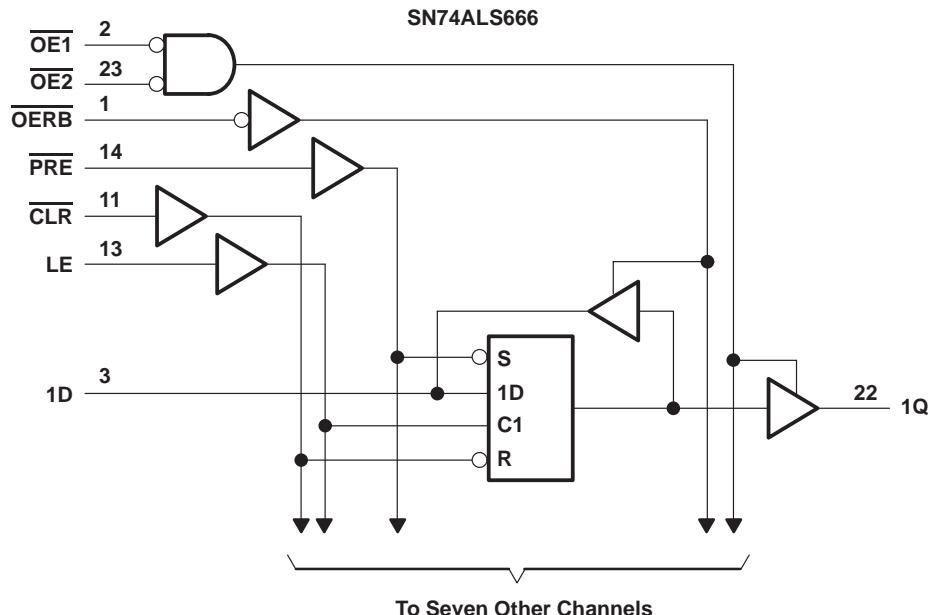
SDAS227A – JUNE 1984 – REVISED JANUARY 1995

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



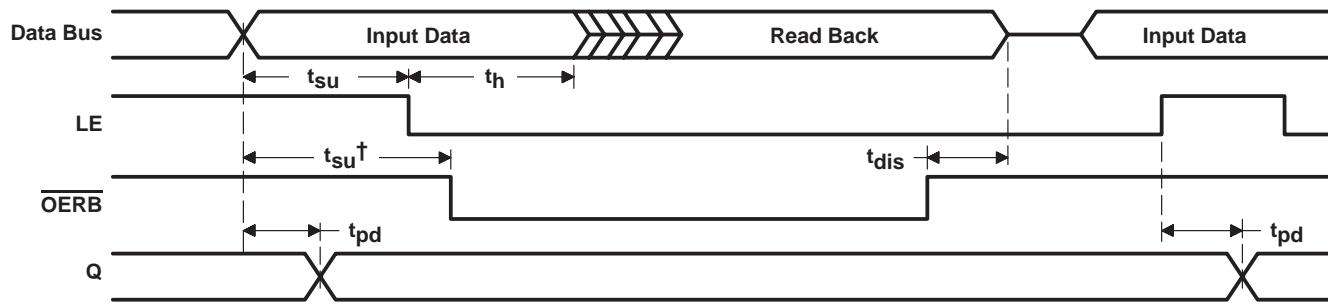
SN74ALS666, SN74ALS667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

WITH 3-STATE OUTPUTS

SDAS227A – JUNE 1984 – REVISED JANUARY 1995

timing diagram



$\overline{CLR} = H$, $\overline{PRE} = H$, $\overline{OE1} = L$, $\overline{OE2} = L$.

† This setup time ensures the read-back circuit does not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I (all inputs except D inputs)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range, T_A : SN74ALS666, SN74ALS667	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS666 SN74ALS667			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q		24	mA
		D		8	
t_w	Pulse duration	LE high	10		ns
		\overline{CLR} low	10		
		\overline{PRE} low	10		
t_{su}	Setup time	Data before $LE \downarrow$	10		ns
		Data before $\overline{OERB} \downarrow$	10		
t_h	Hold time, data after $LE \downarrow$		5		ns
T_A	Operating free-air temperature		0	70	°C

SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

SDAS227A – JUNE 1984 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS666 SN74ALS667			UNIT
		MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	All outputs	$V_{CC} = 4.5 \text{ V}$ to 5.5 V , $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		V
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -2.6 \text{ mA}$	2.4	3.2	
V_{OL}	D inputs	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4
			$I_{OL} = 8 \text{ mA}$	0.35	0.5
	Q or \bar{Q}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4
			$I_{OL} = 24 \text{ mA}$	0.35	0.5
I_{OZH}	Q or \bar{Q}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$		20	μA
I_{OZL}	Q or \bar{Q}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$		-20	μA
I_I	D inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 5.5 \text{ V}$	0.1	mA
	All others		$V_I = 7 \text{ V}$	0.1	
I_{IH}	D inputs‡	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20	μA
	All others			20	
I_{IL}	D inputs‡	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.1	mA
	All others			-0.1	
$I_O\$$		$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	mA
I_{CC}	SN74ALS666	$V_{CC} = 5.5 \text{ V}$, OERB high	Q outputs high	25	50
			Q outputs low	40	73
			Q outputs disabled	30	55
	SN74ALS667	$V_{CC} = 5.5 \text{ V}$, OERB high	\bar{Q} outputs high	25	50
			\bar{Q} outputs low	45	79
			\bar{Q} outputs disabled	30	60

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES
WITH 3-STATE OUTPUTS

SDAS227A – JUNE 1984 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $TA = \text{MIN to MAX}^\dagger$		UNIT	
			SN74ALS666			
			MIN	MAX		
t_{PLH}	D	Q	3	14	ns	
t_{PHL}			4	18		
t_{PLH}	LE	Q	6	21	ns	
t_{PHL}			8	27		
t_{PHL}	$\overline{\text{CLR}}$	Q	9	29	ns	
		D	11	32		
t_{PLH}	$\overline{\text{PRE}}$	Q	7	22	ns	
t_{PHL}		D	9	28		
t_{en}^\ddagger	$\overline{\text{OERB}}$	D	4	21	ns	
	$\overline{\text{OE1}}, \overline{\text{OE2}}$	Q	4	21		
$t_{dis}^\$$	$\overline{\text{OERB}}$	D	1	14	ns	
	$\overline{\text{OE1}}, \overline{\text{OE2}}$	Q	1	14		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] $t_{en} = t_{PZH}$ or t_{PZL}

[§] $t_{dis} = t_{PHZ}$ or t_{PLZ}

switching characteristics (see Figure 1)

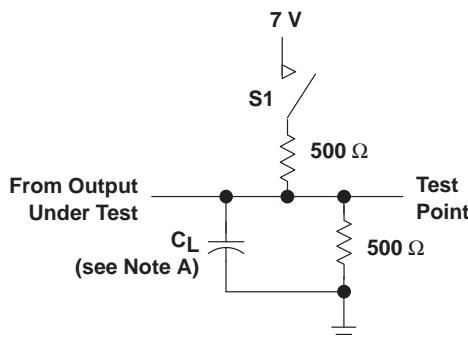
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $TA = \text{MIN to MAX}^\dagger$		UNIT	
			SN74ALS667			
			MIN	MAX		
t_{PLH}	D	\overline{Q}	6	20	ns	
t_{PHL}			4	15		
t_{PLH}	LE	\overline{Q}	9	28	ns	
t_{PHL}			7	22		
t_{PHL}	$\overline{\text{CLR}}$	\overline{Q}	7	24	ns	
		D	8	26		
t_{PLH}	$\overline{\text{PRE}}$	\overline{Q}	8	25	ns	
t_{PHL}		D	9	28		
t_{en}^\ddagger	$\overline{\text{OERB}}$	D	4	21	ns	
	$\overline{\text{OE1}}, \overline{\text{OE2}}$	\overline{Q}	4	21		
$t_{dis}^\$$	$\overline{\text{OERB}}$	D	1	14	ns	
	$\overline{\text{OE1}}, \overline{\text{OE2}}$	\overline{Q}	1	14		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

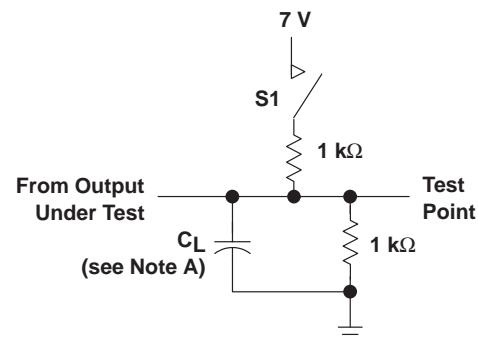
[‡] $t_{en} = t_{PZH}$ or t_{PZL}

[§] $t_{dis} = t_{PHZ}$ or t_{PLZ}

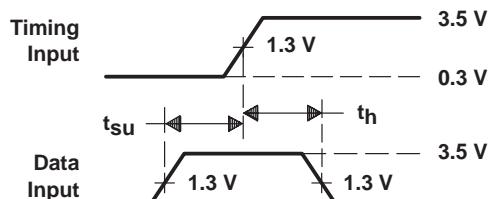
PARAMETER MEASUREMENT INFORMATION



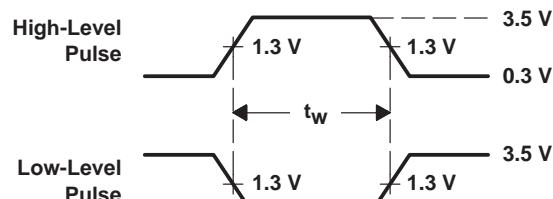
LOAD CIRCUIT FOR Q OR \bar{Q} OUTPUTS



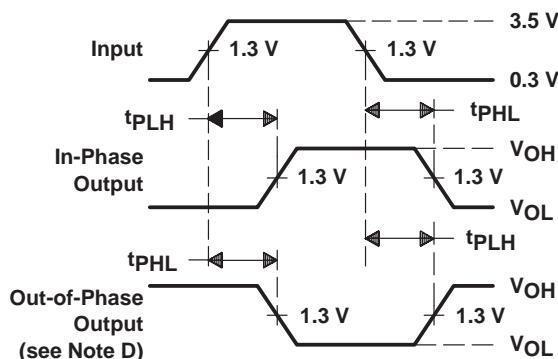
LOAD CIRCUIT FOR D OUTPUTS



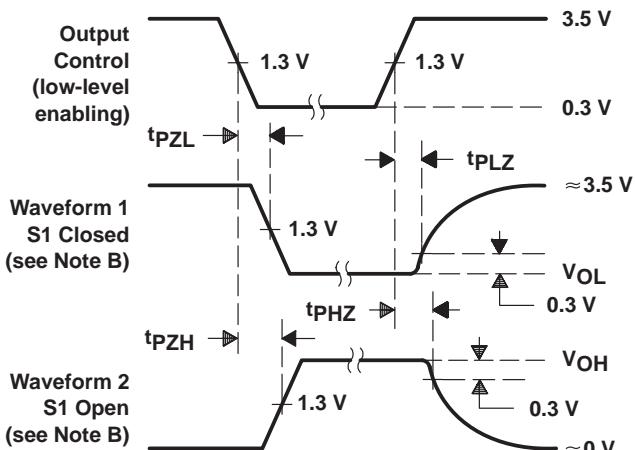
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PULSE DURATIONS



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS666DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS666	Samples
SN74ALS666DWE4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS666	Samples
SN74ALS666DWG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS666	Samples
SN74ALS667DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS667	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

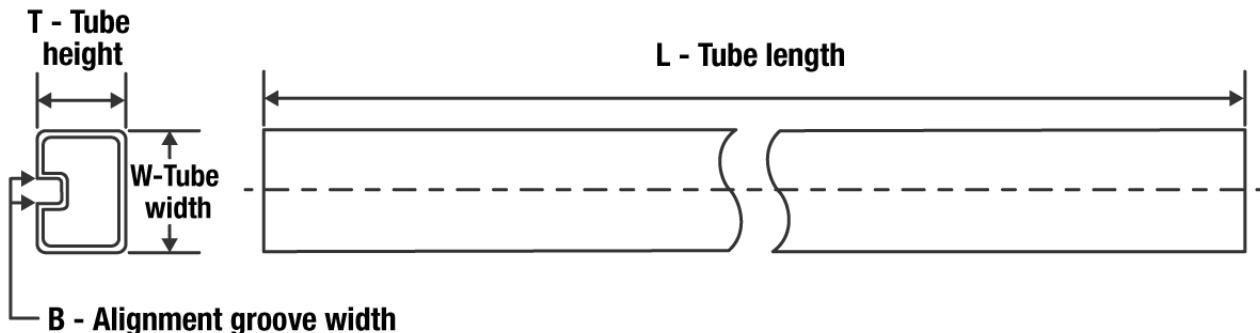
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

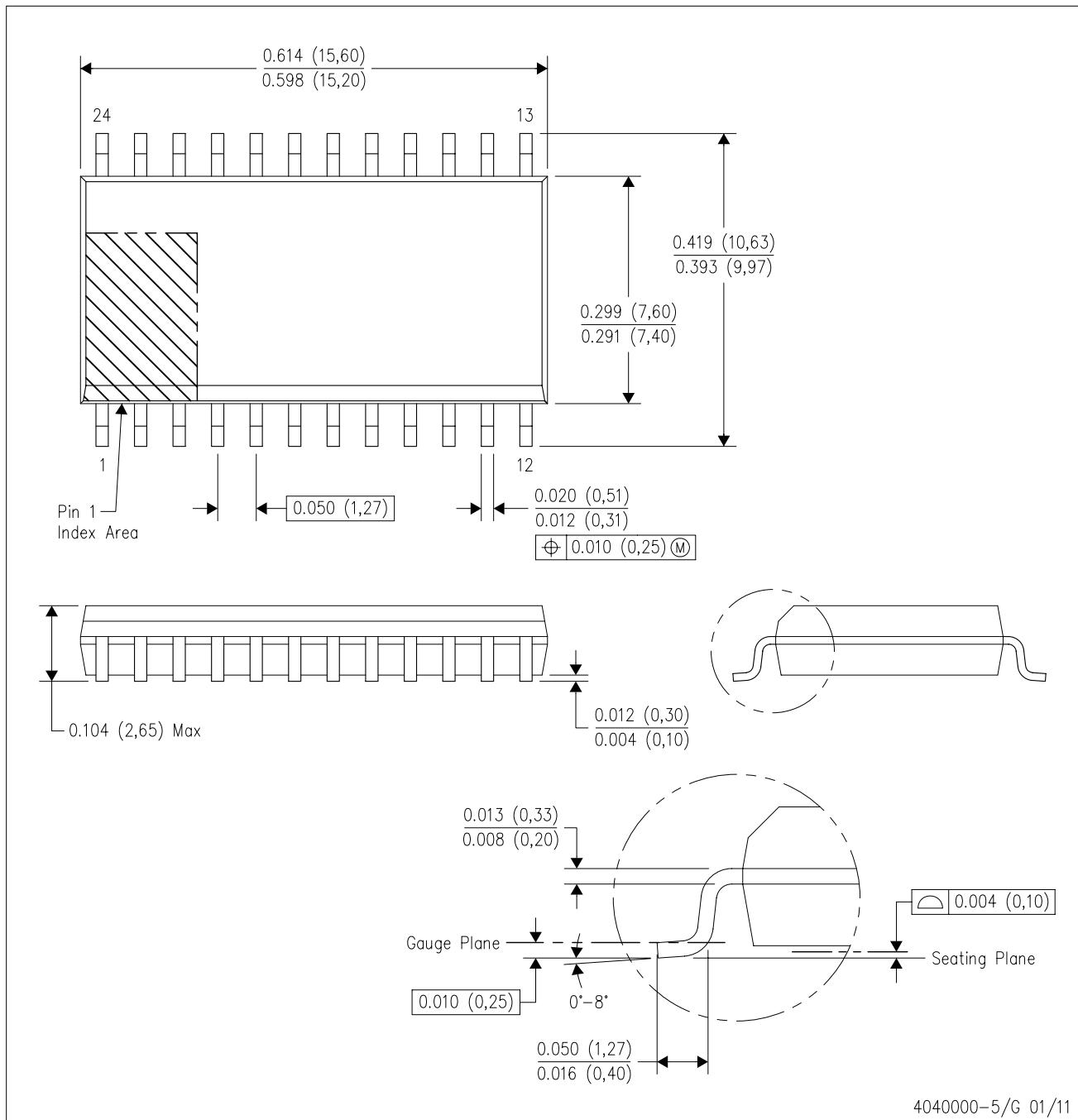
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS666DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS666DWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS666DWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS667DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated