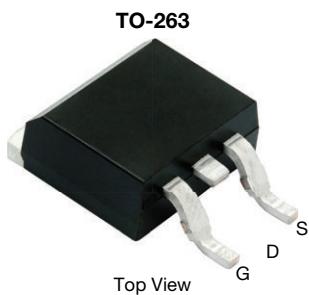


N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A) ^c	Q_g (TYP.)
100	0.0089 at $V_{GS} = 10$ V	50	33 nC
	0.0093 at $V_{GS} = 7.5$ V	50	


Ordering Information:

SUM70090E-GE3 (lead (Pb)-free and halogen-free)

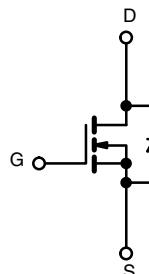
FEATURES

- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- Q_{gd} / Q_{gs} ratio < 1 optimizes switching characteristics
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power supply
 - Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$I_C = 25$ °C	50 °C	A
	$T_C = 70$ °C	50 °C	
Pulsed Drain Current ($t = 100$ µs)	I_{DM}	120	
Avalanche Current	I_{AS}	40	
Single Avalanche Energy ^a	E_{AS}	80	mJ
Maximum Power Dissipation ^a	$T_C = 25$ °C	125	W
	$T_C = 70$ °C ^b	87.5	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) ^b	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.2	

Notes

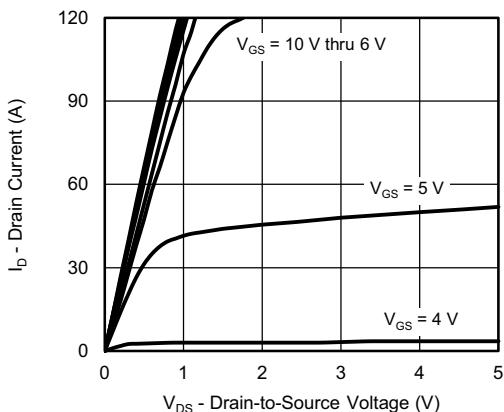
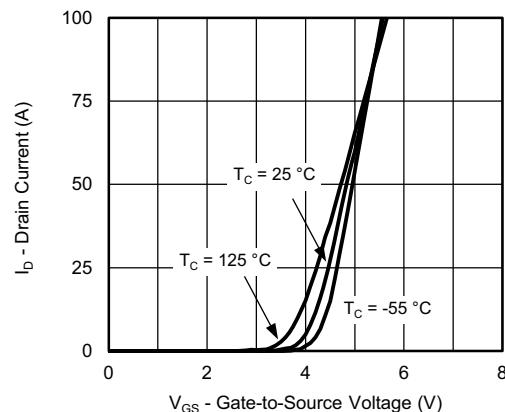
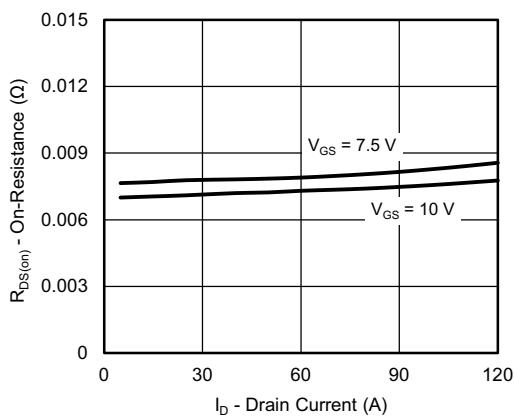
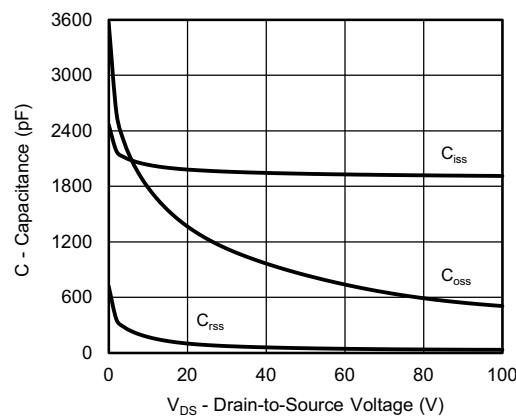
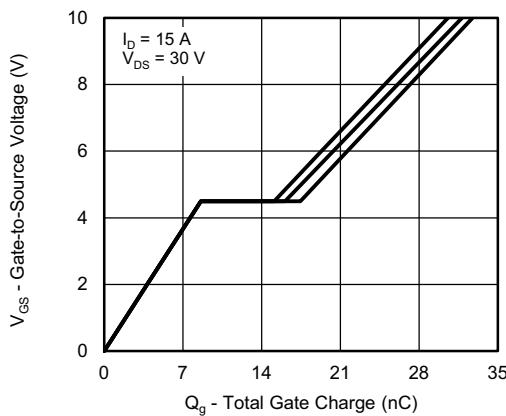
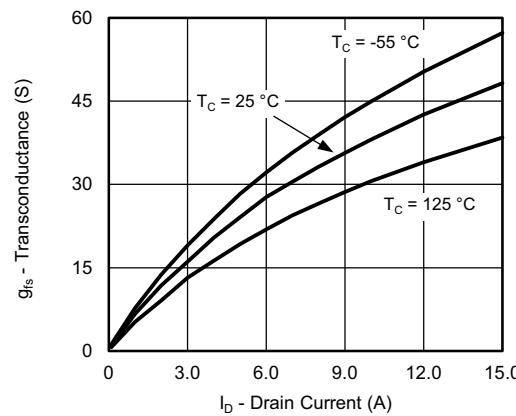
- Duty cycle ≤ 1 %.
- When mounted on 1" square PCB (FR4 material).
- Package limited.

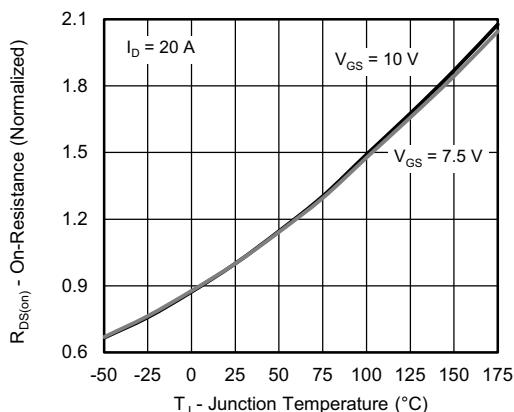
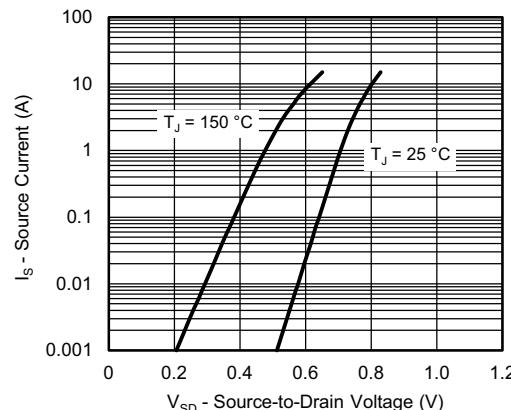
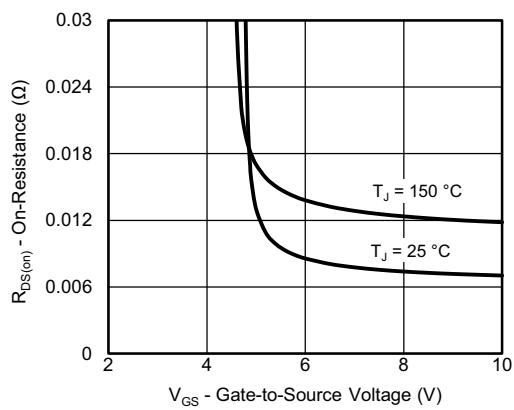
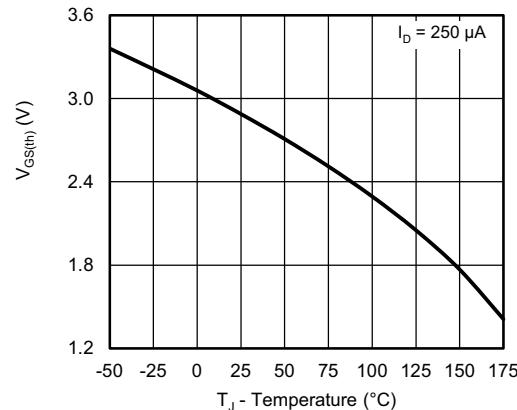
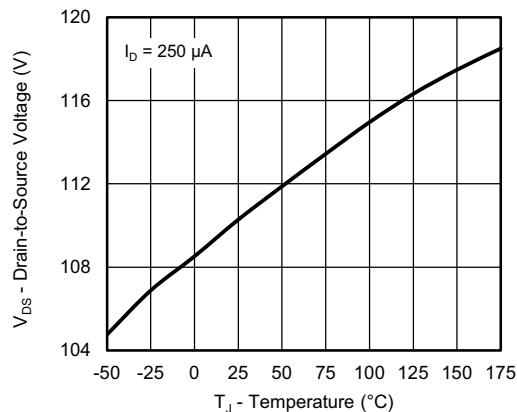
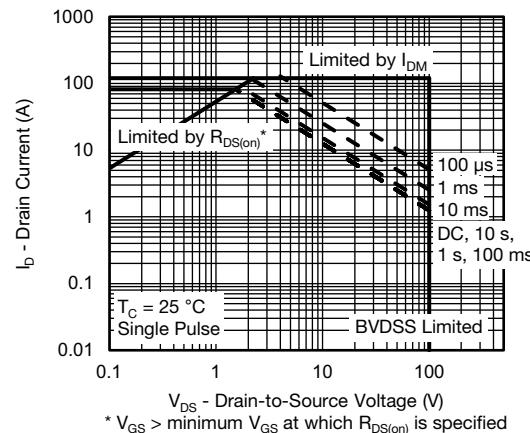
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100	-	-	V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	-	4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	150	
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	5	mA
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 10 \text{ V}$, $V_{GS} = 10 \text{ V}$	50	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	-	0.0074	0.0089	Ω
		$V_{GS} = 7.5 \text{ V}$, $I_D = 15 \text{ A}$	-	0.0077	0.0093	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 10 \text{ A}$	-	38	-	S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$	-	1950	-	pF
Output Capacitance	C_{oss}		-	845	-	
Reverse Transfer Capacitance	C_{rss}		-	54	-	
Total Gate Charge ^c	Q_g	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	-	33	50	nC
Gate-Source Charge ^c	Q_{gs}		-	8.8	-	
Gate-Drain Charge ^c	Q_{gd}		-	7.5	-	
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.7	3.5	7	Ω
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 5 \Omega$ $I_D \equiv 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$	-	15	30	ns
Rise Time ^c	t_r		-	27	54	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$		-	36	72	
Fall Time ^c	t_f		-	45	90	
Drain-Source Body Diode Ratings and Characteristics ^b ($T_C = 25^\circ\text{C}$)						
Pulsed Current ($t = 100 \mu\text{s}$)	I_{SM}		-	-	120	A
Forward Voltage ^a	V_{SD}	$I_F = 10 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	0.8	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = -10 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$	-	77	116	ns
Peak Reverse Recovery Charge	$I_{RM(\text{REC})}$		-	4.2	6.3	A
Reverse Recovery Charge	Q_{rr}		-	145	365	nC

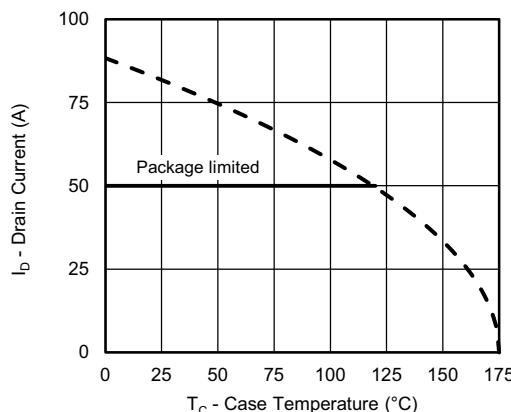
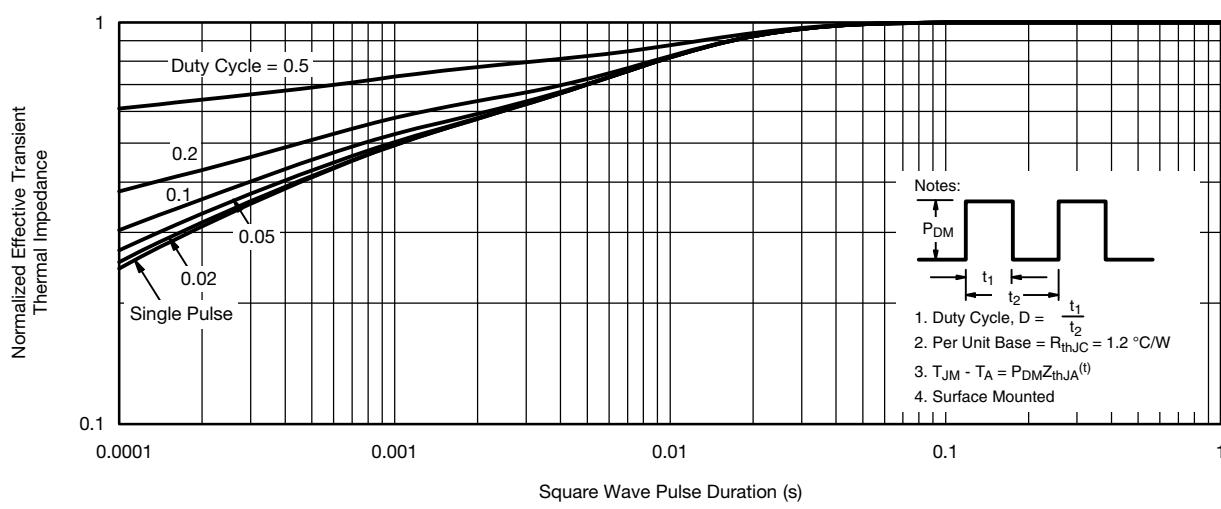
Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

Transconductance

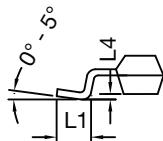
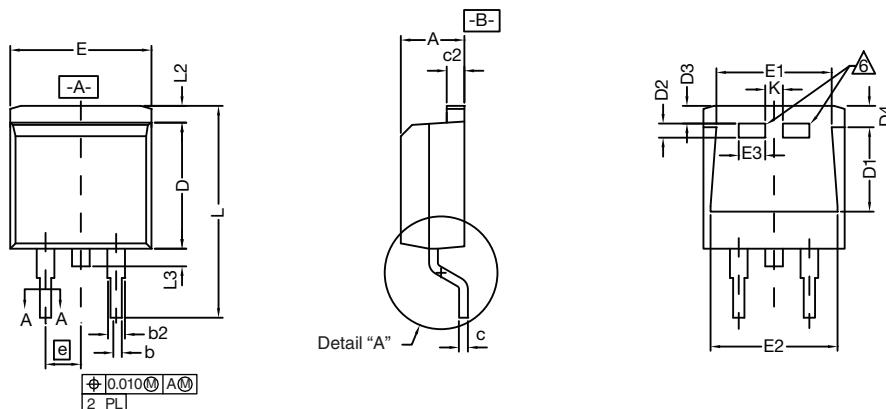
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Voltage vs. Junction Temperature

Safe Operating Area

THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Current De-Rating

Normalized Thermal Transient Impedance, Junction-to-Case
Note

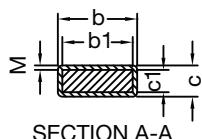
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25°C)
 - Normalized Transient Thermal Impedance Junction to Case (25°C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



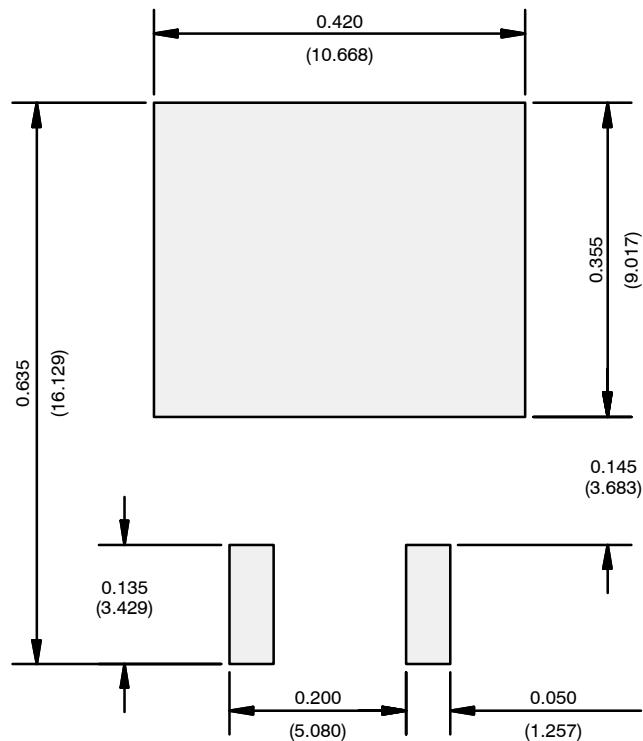
SECTION A-A

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.

 This feature is for thick lead.

DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)

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