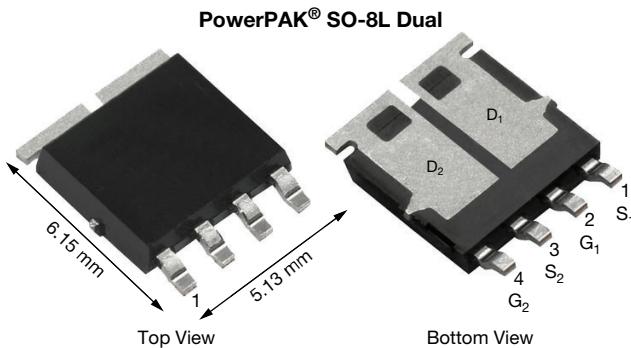


Automotive Dual P-Channel 30 V (D-S) 175 °C MOSFET

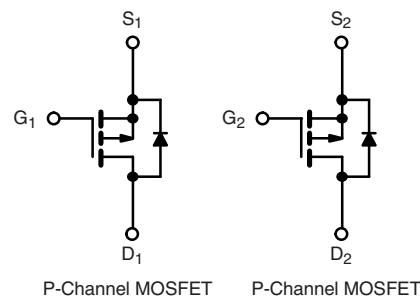


FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc/99912



PRODUCT SUMMARY	
V_{DS} (V)	- 30
$R_{DS(on)}$ (Ω) at $V_{GS} = - 10$ V	0.017
$R_{DS(on)}$ (Ω) at $V_{GS} = - 4.5$ V	0.036
I_D (A)	- 30
Configuration	Dual



ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ951EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	- 30	
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	$T_C = 25 \text{ }^\circ\text{C}^a$	I_D	A
	$T_C = 125 \text{ }^\circ\text{C}$		
Continuous source current (diode conduction) ^a		I_S	
Pulsed drain current ^b		I_{DM}	
Single pulse avalanche current	$L = 0.1 \text{ mH}$	I_{AS}	mJ
Single pulse avalanche energy		E_{AS}	
Maximum power dissipation ^b	$T_C = 25 \text{ }^\circ\text{C}$	P_D	W
	$T_C = 125 \text{ }^\circ\text{C}$		
Operating junction and storage temperature range		T_J, T_{stg}	
Soldering recommendations (peak temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	85	°C/W
Junction-to-case (drain)	R_{thJC}	2.7	

Notes

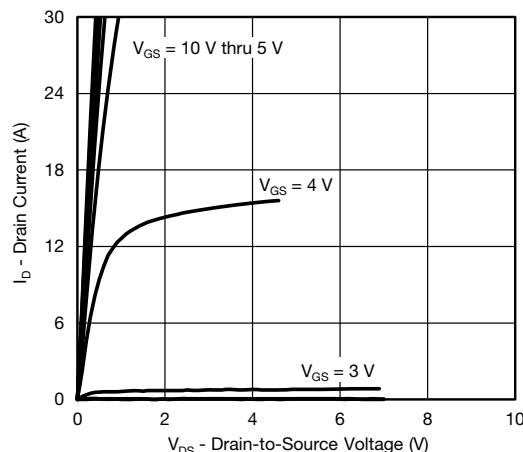
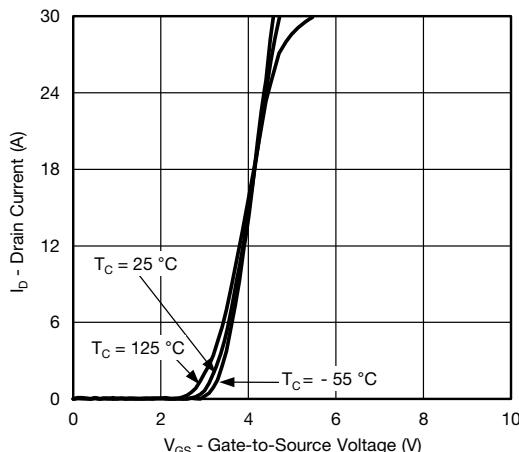
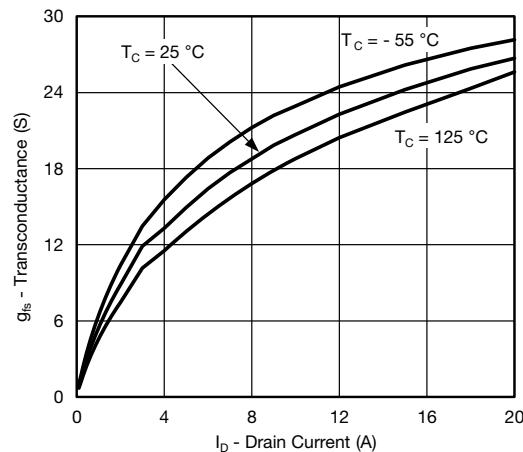
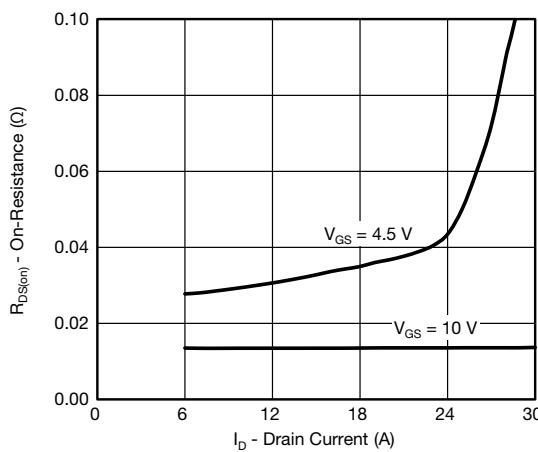
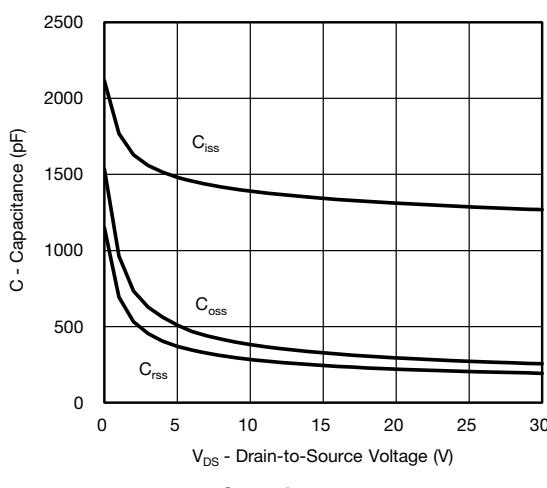
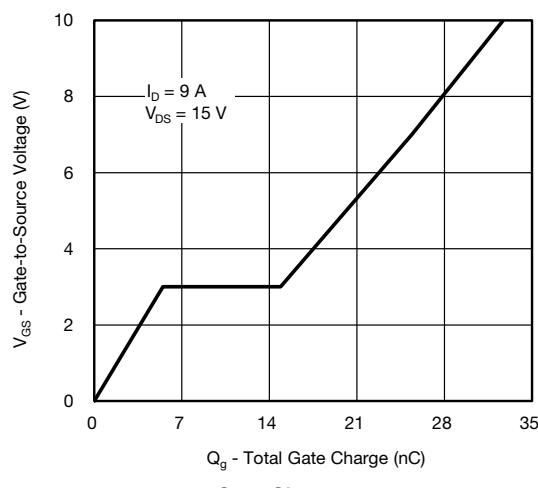
- a. Package limited
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$
- c. When mounted on 1" square PCB (FR4 material)
- d. Parametric verification ongoing
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

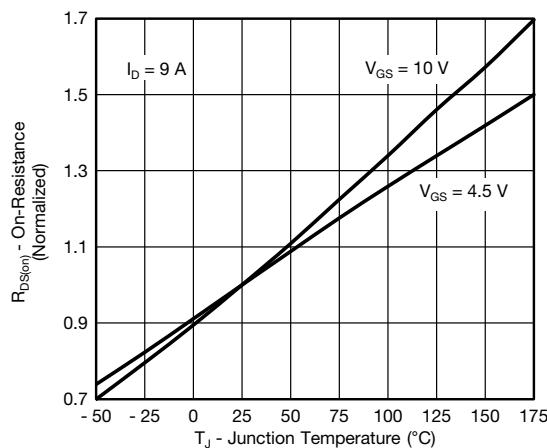
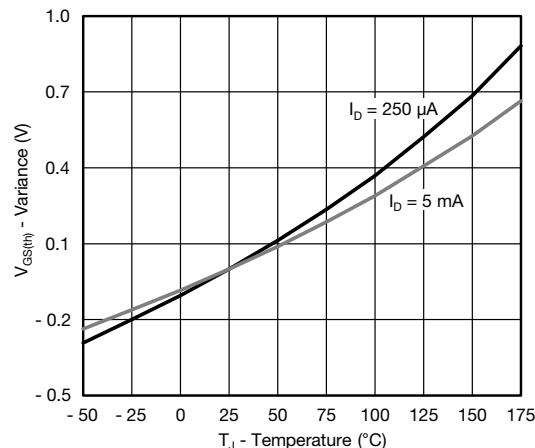
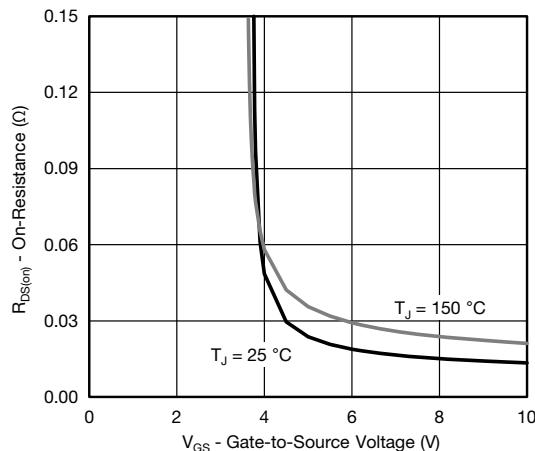
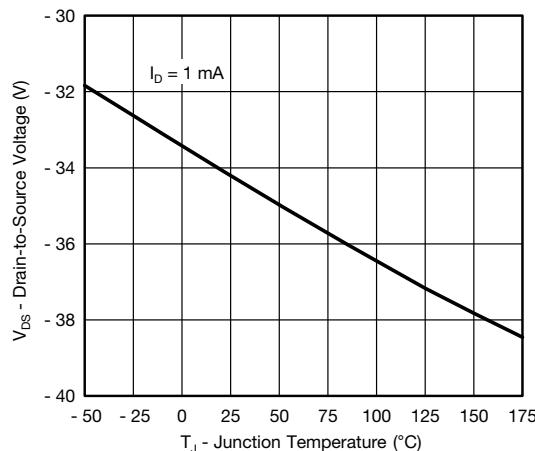
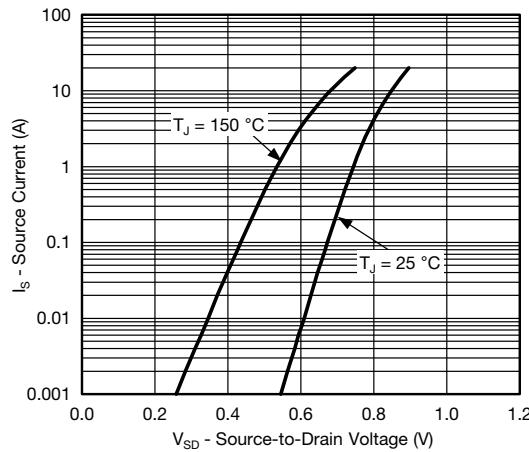
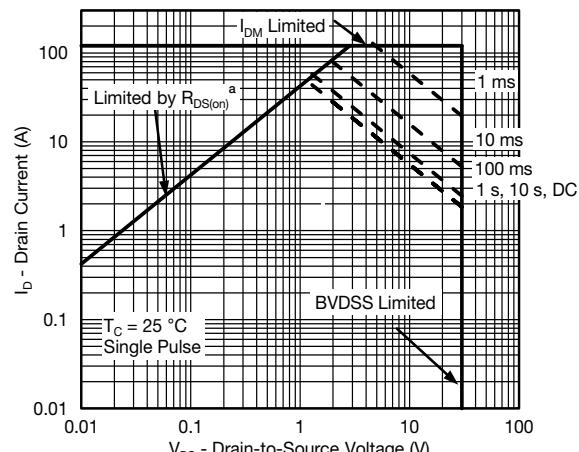
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$, $I_D = -250\ \mu\text{A}$		- 30	-	-	V	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$		- 1.5	- 2.0	- 2.5		
Gate-source leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$		-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\ \text{V}$	$V_{DS} = -30\ \text{V}$	-	-	- 1	μA	
		$V_{GS} = 0\ \text{V}$	$V_{DS} = -30\ \text{V}$, $T_J = 125^\circ\text{C}$	-	-	- 50		
		$V_{GS} = 0\ \text{V}$	$V_{DS} = -30\ \text{V}$, $T_J = 175^\circ\text{C}$	-	-	- 150		
On-state drain current ^a	$I_{D(\text{on})}$	$V_{GS} = -10\ \text{V}$	$V_{DS} = -5\ \text{V}$	- 30	-	-	A	
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10\ \text{V}$	$I_D = -7.5\ \text{A}$	-	0.014	0.017	Ω	
		$V_{GS} = -10\ \text{V}$	$I_D = -7.5\ \text{A}$, $T_J = 125^\circ\text{C}$	-	-	0.034		
		$V_{GS} = -10\ \text{V}$	$I_D = -7.5\ \text{A}$, $T_J = 175^\circ\text{C}$	-	-	0.039		
		$V_{GS} = -4.5\ \text{V}$	$I_D = -5\ \text{A}$	-	0.030	0.036		
Forward transconductance ^b	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -7.5\ \text{A}$		-	18	-	S	
Dynamic ^b								
Input capacitance	C_{iss}	$V_{GS} = 0\ \text{V}$	$V_{DS} = -10\ \text{V}$, $f = 1\ \text{MHz}$	-	1345	1680	pF	
Output capacitance	C_{oss}			-	330	415		
Reverse transfer capacitance	C_{rss}			-	245	305		
Total gate charge ^c	Q_g	$V_{GS} = -10\ \text{V}$	$V_{DS} = -15\ \text{V}$, $I_D = -9\ \text{A}$	-	33	50	nC	
Gate-source charge ^c	Q_{gs}			-	5.5	-		
Gate-drain charge ^c	Q_{gd}			-	9.4	-		
Gate resistance	R_g	$f = 1\ \text{MHz}$		3	6.31	10.5	Ω	
Turn-on delay time ^c	$t_{d(\text{on})}$	$V_{DD} = -15\ \text{V}$, $R_L = 1.66\ \Omega$ $I_D \approx -9\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_g = 6\ \Omega$		-	12	18	ns	
Rise time ^c	t_r			-	12	18		
Turn-off delay time ^c	$t_{d(\text{off})}$			-	39	59		
Fall time ^c	t_f			-	28	42		
Source-Drain Diode Ratings and Characteristics ^b								
Pulsed current ^a	I_{SM}			-	-	- 120	A	
Forward voltage	V_{SD}	$I_F = -4.5\ \text{A}$, $V_{GS} = 0$		-	- 0.8	- 1.2	V	

Notes

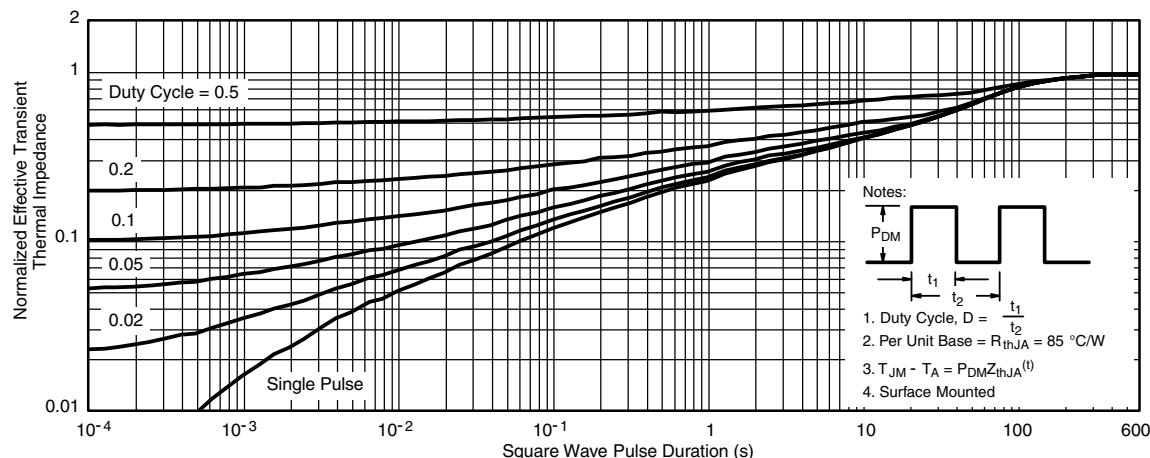
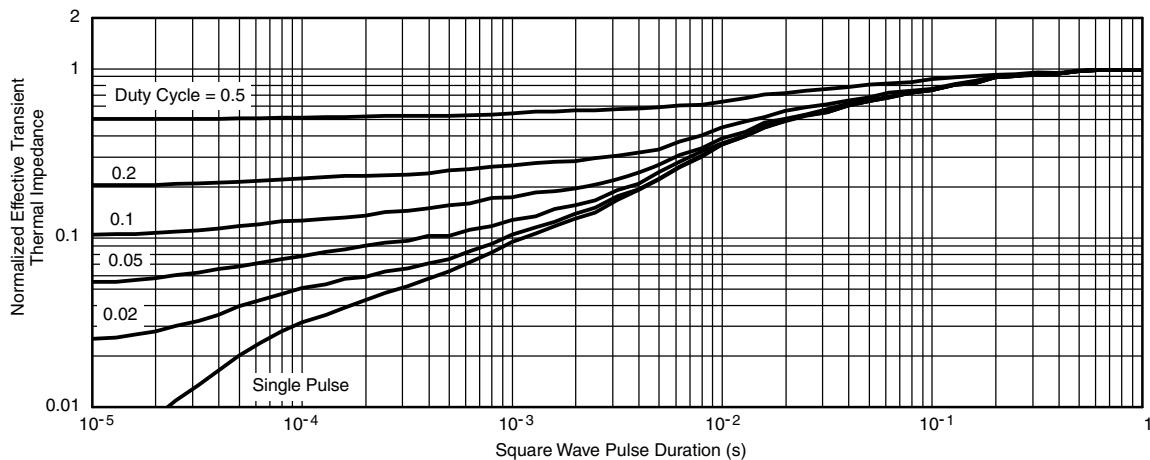
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ %$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

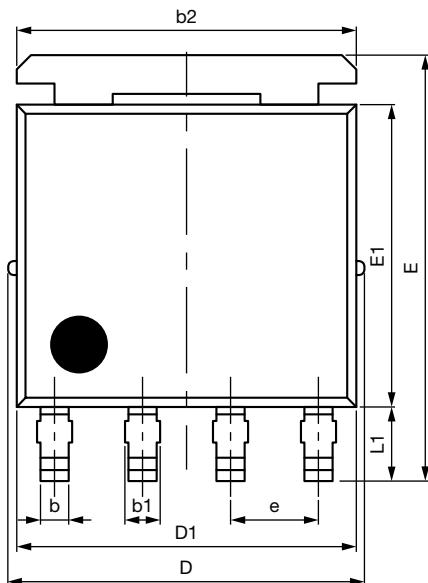
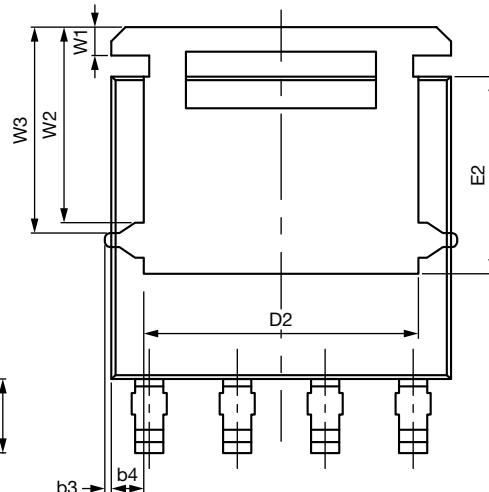
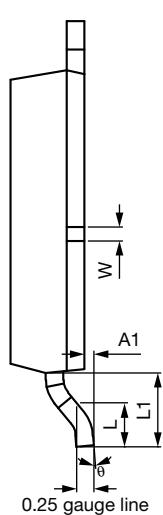
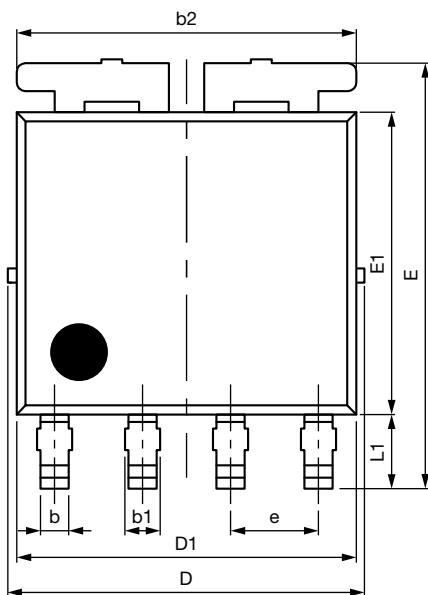
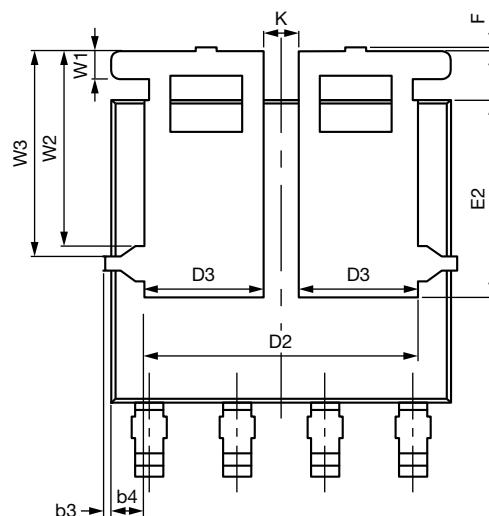
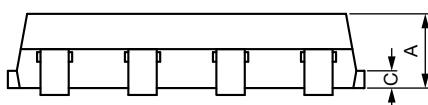

On-Resistance vs. Junction Temperature

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

BVDSS vs. Junction Temperature

Source Drain Diode Forward Voltage

Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63658.

PowerPAK® SO-8L Case Outline 2


Topside view (single)

Backside view (single)

Topside view (dual)

Backside view (dual)




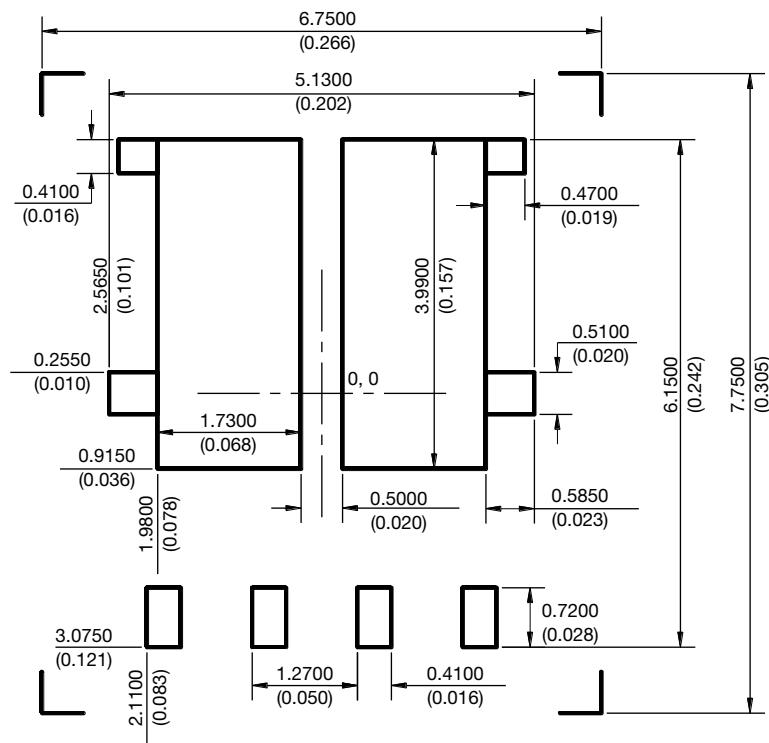
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°

ECN: C21-1498-Rev. C, 01-Nov-2021

DWG: 6044

Note

- Millimeters will govern

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL


Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)

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